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# Simple Digital to Analog Converter

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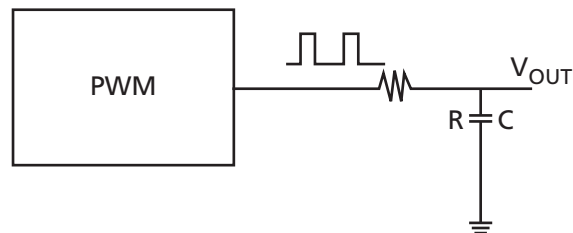
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## Introduction

Methods for implementing a digital to analog converter (DAC) differ depending on the required resolution, speed, and cost. For many applications that do not have high resolution or speed requirements, a simple and cost-effective approach to converting digital to analog is to use a pulse width modulation (PWM) function together with a RC low-pass filter (LPF), as shown in [Figure 1](#). The RC LPF is one of the simplest analog electronic filters that passes low frequencies well but attenuates (reduces) the unwanted higher frequencies. By varying the duty cycle, usually controlled by a state machine or microcontroller, the LPF charges while the PWM signal is **ON** and discharges while the PWM signal is **OFF**, generating an analog output voltage. This application brief describes the techniques of PWM control (using the Microsemi Core8051 microcontroller) as well as design criteria for the RC filter.

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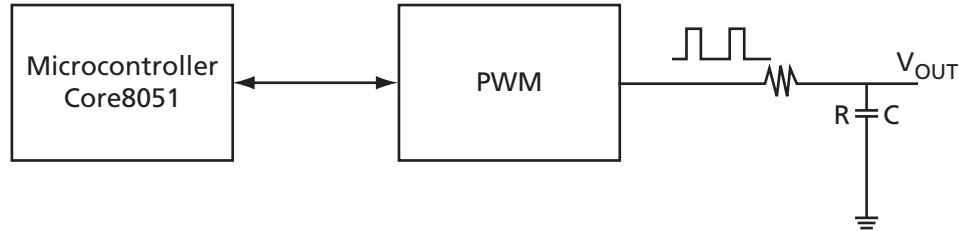


**Figure 1 • Simple DAC Concept Diagram**

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## Application Implementation

Microsemi Core8051 and CorePWM are designed with integration in mind. Core8051 and CorePWM can be implemented in various Microsemi device families to accomplish a simple DAC application with some external circuitry, as shown in [Figure 2](#).



**Figure 2 • Simple DAC Implementation with Core8051 and CorePWM**

## CorePWM Control

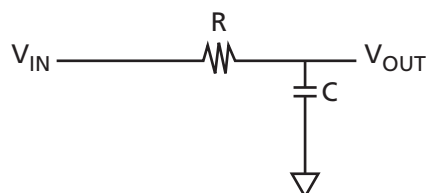
In order to convert different digital voltages to analog voltages, the user must generate different PWM duty cycles.

The CorePWM duty cycle is controlled by both the positive edge value and the negative edge value for a given duty cycle. The edge values are registered in the PWM\_POSEDGE and PWM\_NEGEDGE registers separately. A CorePWM duty cycle calculator provided on the Microsemi website can be used to assist in calculating the PWM\_POSEDGE and PWM\_NEGEDGE register values, given a requested duty cycle.

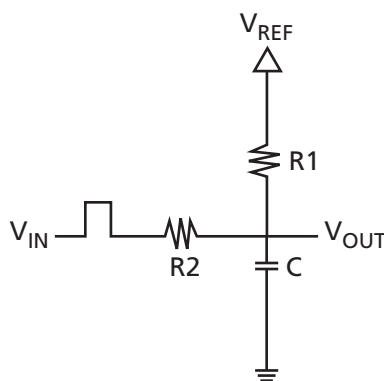
Applying the PWM\_POSEDGE and PWM\_NEGEDGE register values in the software implementation of Core8051, the user can control the CorePWM duty cycle. For more information about CorePWM, refer to the [CorePWM Datasheet](#).

## External Circuitry

A Fourier analysis of a typical PWM signal shows that there is a strong peak at frequency  $F_n = 1/T$ . Other strong harmonics also exist at  $F = K/T$ , where  $K$  is an integer. These peaks are unwanted noise and must be eliminated. This requires that the PWM signal be LPF, therefore eliminating these inherent noise components. [Figure 3](#) and [Figure 4](#) shows different LPF circuitries.



**Figure 3 • First Order Passive LPF**

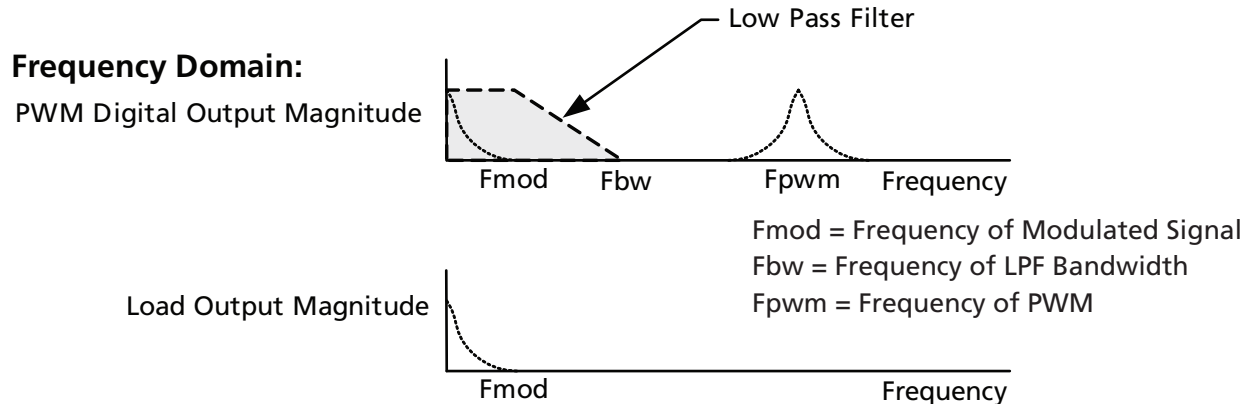


**Figure 4 • Modified First Order Passive LPF**

First order passive LPFs are used for low cost and low resolution requirement applications, as shown in [Figure 3](#) and [Figure 4](#). The circuit in [Figure 3](#) can be driven by OUTBUF and the  $V_{OUT}$  can swing from almost 0 to  $V_{OH}$ , but the  $V_{OUTMAX}$  is limited by the  $V_{CCI}$ . The circuit in [Figure 4](#) drives a higher voltage than the devices 3.3 V limit and can be driven by TRIBUF or an open collector. Its  $V_{OUTMAX}$  can swing almost to  $V_{REF}$ , not limited by the  $V_{CCI}$ . However, its  $V_{OUTMIN}$  cannot reach 0 V because of the  $R1/R2$  voltage divider.

For an application that requires  $V_{OUTMAX} > V_{CCI}$ , the open collector solution is desired, as shown in [Figure 4 on page 3](#). If  $R = R1 \parallel R2$ , then RC defines the cutoff frequency or bandwidth (Fbw) of the LPF. Decreasing the value of R2 in order to get lower  $V_{OUTMIN}$  can increase the LPF cutoff frequency, which can let more noise pass through. The LPF must allow the modulated digital signal to pass through but filter out the higher PWM frequency (Fpwm), as shown in [Figure 5](#).

The desired signal must follow a pattern similar to the one shown in [Figure 5](#).



*Note:*  $Fbw \ll Fpwm$  or  $Fpwm \gg Fbw$ , implies  $Fpwm = K \times Fbw$ , where  $K \gg 1$ .

**Figure 5 • First Order Low Pass Filter Frequency Domain**

## Conclusion

Many embedded applications require the generation of analog signals. Although separate DAC ICs exist on the market today, Fusion with a PWM, such as CorePWM, can integrate these components and reduce cost and circuit board space while improving reliability in embedded control applications that need a PWM. A low cost, simple DAC can be implemented with Fusion, ProASIC<sup>®</sup>3/E, ProASIC<sup>PLUS</sup><sup>®</sup>, Axcelerator<sup>®</sup>, or RTAX-S FPGAs using Microsemi Core8051 and CorePWM plus a few external components.

These techniques can be used to generate dual-tone multiplexed frequencies (DTMF) for telephone dialing, controlling the speed of a motor, generating sound, complex waveforms, generating variable voltages, and performing voltage trimming in a power management system.

## List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Pages
Revision 1 (January 2016)	Non-technical updates.	NA
Revision 0 (August 2006)	Initial release.	NA

*\*The part number is located on the last page of the document.*



**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo,  
CA 92656 USA

**Within the USA:** +1 (800) 713-4113  
**Outside the USA:** +1 (949) 380-6100  
**Sales:** +1 (949) 380-6136  
**Fax:** +1 (949) 215-4996

**E-mail:** [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

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