A CONCEPTUALLY NEW QUAD POWER FAULT MONITOR CIRCUIT

Abstract

SG1548 is a comprehensive fault monitoring system in a single 16-pin IC. The new circuit provides overvoltage and undervoltage supervision of four DC power supplies simultaneously. In addition a uniquely flexible pin-out permits AC line voltage monitoring, real-time line clock generation, or programmable switching supply undervoltage lockout protection. All fault thresholds are adjustable to a high degree of accuracy using a minimum of external passive components. A number of typical application examples are given to clarify the concepts discussed.

Introduction

As the complexity of modern electronic systems grows, the number of supply voltages necessary to support the circuitry has also increased. Even the simplest home computer typically requires +5 V for the logic, 12 or 15 V for the analog circuits, and perhaps +24 V or +28 V for the printer or disk drive. The task of supervising these multiple voltages for proper tolerance has traditionally required a substantial number of precision components: a voltage reference, resistors, timing capacitors, op-amps, comparators, and logic gates.

An additional penalty was paid in board space consumption. Consequently, in an attempt to shave costs, the supervisory function was often eliminated entirely. While this action resulted in meeting budget for the supply, the money saved was often given out again many times over when a system malfunction occurred in the field and a service engineer had to tediously check each supply voltage.

The availability of a new integrated circuit which can monitor four DC supplies and the AC line simultaneously now allows the power systems designer to implement fault monitoring at lower cost and with much reduced board space. This new device utilizes the strengths of monolithic linear technology to create precisely matched components at high density on a silicon chip, the SG1548 Quad Power Fault Monitor. Functional block diagram is shown in Figure 1.

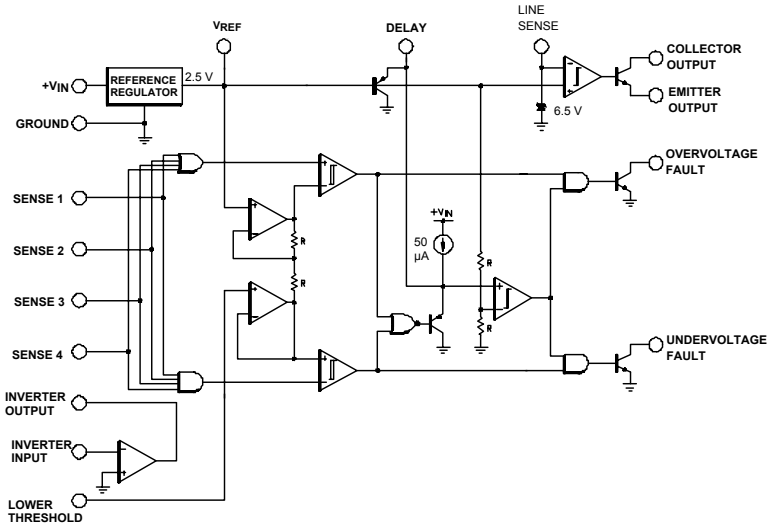


Figure 1. Block Diagram of the SG1548 Quad Power Fault Monitor

Functional Description

The circuit consists of a precision reference regulator, a fault window generator, analog OR and AND circuitry for selecting most positive and most negative voltages, threshold comparators, delay logic, open-collector output drivers, an inverting amplifier, and a multipurpose line sense comparator with uncommitted collector and emitter outputs.

The most positive voltage at the four Sense inputs is compared with the upper or overvoltage threshold, and the most negative input is routed to the undervoltage comparator. The comparator outputs are connected to their respective output drivers and two AND logic gates. The drivers are inhibited by the delay logic, which requires that either an overvoltage fault or undervoltage fault persists for a pre-set time interval. A single capacitor at the Delay pin sets the time interval, which is C x 2.5 x 10^4 s. If a negative voltage must be monitored, it can be mirrored into a positive voltage using the inverter amplifier. Special clamp circuitry inside the SG1548 prevents the amplifier from locking up if Pin 15 is pulled below ground. Now let's look at the operation of each subset in detail.

Voltage Reference

The reference circuit is a low-drift bandgap design which generates a precise +2.50 V ±1% at Pin 3. It is fully functional at input voltages as low as +4.5 V, and provides up to 10 mA of output current. Special β-compensation circuitry provides immunity to process variations and achieves typical 1 mV line and 3 mV load regulation. Internal current limiting protects the IC against accidental shorts to ground.

Fault Window Generator

The fault window generator is the heart of the Quad Power Fault Monitor. This section generates an upper overvoltage and lower undervoltage threshold centered about the +2.5 V reference. A precision tracking regulator utilizing two operational amplifiers and a pair of ratioed resistors produce the tracking action, as shown in Figure 2.

An external voltage derived from the reference is applied to Pin 1. This voltage represents the lower boundary of the tolerance window. Op-amp A1 is connected as a unity-gain buffer, providing a low input bias current and a low impedance output for driving the remaining circuitry. The transfer function through A1 is simply:

$$V_{LOWER} = V_{REF} - \Delta V \pm V_{OS1} \quad [1]$$

where V_{OS1} is the input offset voltage of A1, and ΔV is some small percentage of V_{REF}. Op-amp A2 is connected as an inverter working at a common mode voltage equal to V_{REF}. Its transfer function is given by:

$$V_{UPPER} = \frac{R_2}{R_1} \{\Delta V \pm V_{OS1} \pm V_{OS2}\} + V_{REF} \pm V_{OS2} \quad [2]$$

where V_{OS2} is the input offset voltage of A2, and bias current errors are assumed to be very small.

If $\frac{R_2}{R_1}$ is nearly 1, then

$$V_{UPPER} = V_{REF} + \Delta V \pm V_{OS1} \pm 2V_{OS2} \quad [3]$$

Since R1 = R2 = 2 k and the resistor match very well over the temperature, then the above assumptions about bias current error and resistor ratio are correct. Therefore the limit as to how small ΔV can be is approximately 3 times the offset voltage, neglecting comparator offsets. If a worst case value of 8 mV is assumed, the smallest value of ΔV is 24 mV, corresponding to a fault tolerance of ±1%. Since this is the same order as the initial accuracy of the reference, ±2% is recommended as the tightest setting for the tolerance window.

Dual Channel Delay with a Single Capacitor

In supervisory circuits, delay is frequently required to reject false fault reports which could result from switching supply spikes or transients due to step load changes. The delay circuit in the SG1548 requires only one capacitor to implement the delay function for both the overvoltage and undervoltage channels.

The circuit depends on two factors for low false alarm rates:

1. Reports due to noise are of short duration compared to the program delay.

2. Noise causing false threshold crossings in each channel is essentially uncorrelated.

When all four voltages at the Sense pins fall within the set fault tolerance band, the output of each fault comparator is LOW.

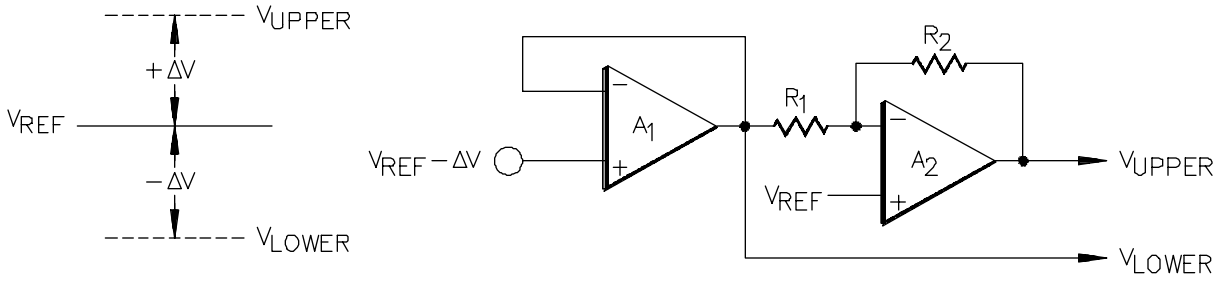


Figure 2. Generating a Precision Fault Tolerance Window

The output of the 2-input NOR gate is HIGH, turning on the discharge transistor Q1. The Delay pin is held at ground. This is below the +1.25 V trip threshold of the delay comparator, resulting in a LOW logic level to each of the output AND gates. Since both inputs must be HIGH to turn on the output drivers, no fault indication is possible.

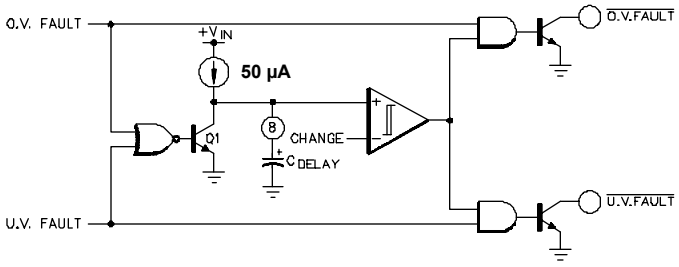


Figure 3. False Alarm Rejection Using a Single Capacitor

When one of the sensed voltages crosses a fault threshold, the fault comparator switches HIGH, turning off Q1. The delay pin voltage rises linearly from 0 V as the 50 µA current source charges the daily capacitor. If the fault condition persists long enough, the capacitor will charge to +1.25 V, tripping the delay comparator, which has hysteresis to eliminate jitter due to the slow ramp. The HIGH output level from the comparator enables both output drivers, permitting an overvoltage and/or undervoltage indication as appropriate.

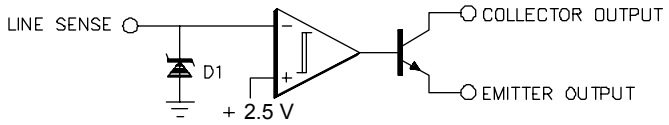


Figure 4. Block Diagram of the AC Line Sense Circuit

AC Line Sense Comparator

The line Sense section of the SG1548 is a high-gain comparator with 25 mV of hysteresis referenced to the precision +2.5 V threshold voltage. The output transistor is rated at 40 V and 10 mA, and has uncommitted collector and emitter connections for either inverting or non-inverting operation. A unique clamp diode structure (D1) on the input adds to the versatility of this section, since it is specified for both forward and reverse conduction at 1 mA. (Most junction-isolated integrated circuits can behave strangely or self-destruct if any pin is driven negative with respect to the substrate. The AC Line Sense pin was specifically designed to operate in this mode, thereby eliminating the need for an external clamp diode).

On-Chip Inverting Amplifier

The operational amplifier provided for converting a negative voltage to a positive one is optimized for inverter operation with the summing node at ground. The amplifier has a minimum open loop gain of 72dB, and is internally compensated for unity gain stability.

Like the AC line Sense input pin, the Inverting Input pin can be pulled below ground by nature of the external circuitry. To prevent the possibility of latch-up under these conditions, clamp circuitry as illustrated in Figure 5 exists at the pin. These protective components clamp negative excursions to -0.5V_{BE} or approximately -0.3 V at +25°C. This prevents the substrate diode from conducting and activating any parasitic SCRs in the IC. An additional diode limits the maximum positive input voltage to 1 V_{BE} to eliminate the possibility of latch up in the direction.

Input offset characteristics are further improved with a special Kelvin grounding scheme for the non-inverting input. Separate bounding pads exist at the periphery of the chip for power ground and the op-amp input. The bond wires become common only at the IC package pin itself, eliminating the errors due to ground drops in the circuit metallization.

A performance factor called “inversion error” can be defined from the amplifier’s electrical parameters which quantizes the total deviation from ideal inversion. It includes the effects of input offset voltage, input bias current, input offset current, and finite open-loop voltage gain. For unity-gain operation with perfect 10 k/10 k gain setting resistors, the maximum inversion error for the SG1548 is 26.5 mV or 1.06% referred to the +2.5 V fault window center. In most applications the error will be less. For example, if -15 V is converted to +2.5 V, the closed loop gain will be -1/6. The output stage can source at least 5 mA, so 6 k/1 k gain resistors can be used. With these values the maximum inversion error falls to 13.5 mV or 0.5%. The actual resistor tolerances will, of course, degrade this further.

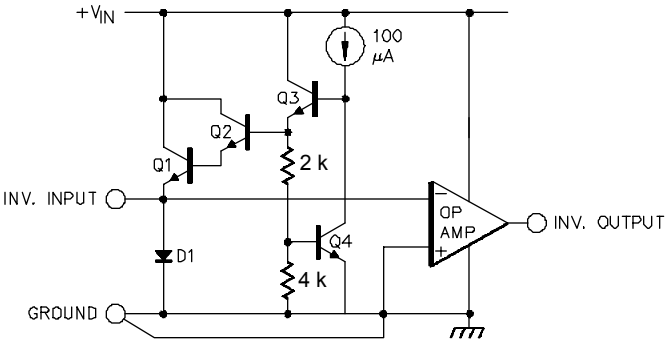


Figure 5. Protective Circuitry at the Inverter Input Terminals

Setting the Fault Tolerance

The fault tolerance window is set by applying a voltage slightly less than the +2.50 V reference to the Lower Threshold pin.

In the example shown in Figure 6, a ±2% window is programmed with the divider network formed by R_A and R_B. The maximum input bias current at Pin 1 is 1.0 µA, so the divider current is chosen to be three orders of magnitude greater to minimize threshold shifts. With the resistor values shown, +2.450 V is applied to Pin 1, setting up nominal ±50 mV threshold values about the +2.500 reference. Resistors should be of the same type so that temperature coefficients will track, maintaining a constant divider ratio. The allowable voltage range on the adjustment pin is +2.45 V to +1.50 V, corresponding to ±2% and ±40% fault tolerance bands.

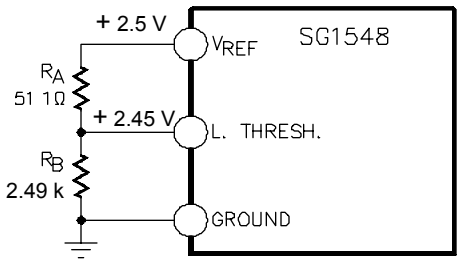


Figure 6. Programming the Fault Tolerance Window

Implementing Multiple Tolerances

In actual practice, some power supply tolerances may be more critical than others. For example, most +5 V logic can withstand ±10% variations without malfunction, whereas the analog circuitry might require ±5% accuracy. Multiple tolerances can easily be obtained with the SG1548 using the technique shown in Figure 7.

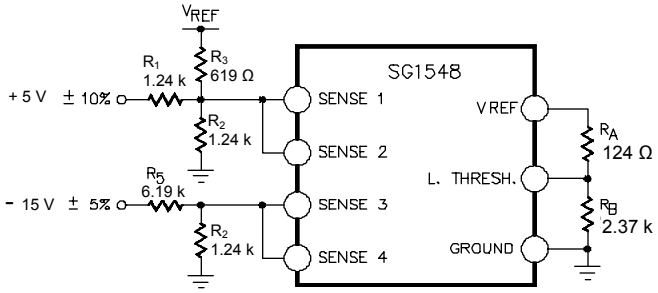


Figure 7. Implementing Multiple Tolerances

The Quad Power Fault Monitor is first programmed for the tightest tolerance required. In this case the +15 V supply must be held within ±5% of its nominal value, so R_A and R_B are chosen such that ±125 mV window edges are set at Pin 1, and pin 13 is set at 2.5 V by R4 and R5 divider network. Next, the required tolerance of ±10% for the +5 V input is set by adding a resistor R3 from the sense pin to the 2.5 V reference. In this section a set of formulas are derived to calculate R1, R2, and R3 considering the effect of the sink current capability of the reference voltage.

Given: 1. Nominal Input Voltage - V_{NOM}
2. A programmed window tolerance - X%
3. A desired fault tolerance - Y%

1. Calculate: $P = (V_{NOM} - 2.5)/2.5$

2. Choose R_2 such that:

$$R_2 \geq (5)\ (Y\text{-}X)\ \left(\frac{P+1}{P}\right)$$

3. Calculate R_1 and R_3 by:

$$R_1 = PR_2$$

$$R_3 = \left(\frac{X}{Y - X}\right)\left(\frac{PR_2}{P + 1}\right)$$

4. Calculate reference sink current:

$$I_{SINK} = \frac{(2.5)(X)}{R_3}$$

I_{SINK} calculated should be less than 500 µA.

5. Check your calculation by calculating fault tolerance Y:

$$Y = \left(1 + \frac{R_1/R_3}{R_1/R_2}\right)(X) \quad [\%]$$

This value should be very close to your desired value of Y.

EXAMPLE:
Given: 1. V_{NOM} = 5 V
2. X = 5%
3. Y = 10%

1. Calculate P:

$$P = \frac{5 - 2.5}{25} = 1$$

2. Choose R_2:

$$R_2 \geq (5)\left(\frac{10 - 5}{100}\right)(2) = .50\ k\Omega$$

Choose R_2 = 1.24 k

3. Calculate R_1 and R_3:

$$R_1 = R_2 = 1.24\ k$$

$$R_3 = \left(\frac{5}{10 - 5}\right)\left(\frac{1.24}{2}\right) = 620\ \Omega$$

Choose R_3 = 619 Ω

4. Calculate reference sink current:

$$I_{SINK} = \frac{(2.5 \times 0.05)}{619} = 202\ \mu A$$

5. Check Calculation:

$$Y = \left(1 + \frac{1.24 / 0.619}{1 + 1.24 / 1.24}\right)(5) = 10.008\%$$

Inverting a Negative Supply

Conversion of a negative source to +2.50 V is straightforward, as shown in Figure 8. The op-amp is operated at a closed loop gain less than unity. However, since the amplifier is internally compensated for unity gain, it is possible to monitor voltages less than 2.5 V (gain greater then unity) without additional components for stability.

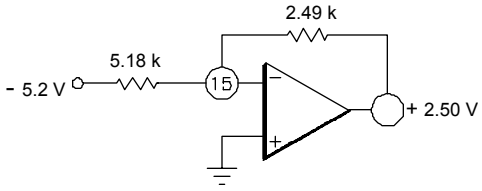


FIGURE 8. Inverting and Scaling a Negative Voltage

Determining Fault Delay

Fault delay as a function of delay capacitor on Pin 8 is given by the graph in Figure 9. The line reflects the time required to charge a given capacitor to +1.25 V with a nominal 50 µA current source. Delays beyond several hundred milliseconds can be obtained, but for capacitor values beyond 5 µF, the surge limiting circuit shown in Figure 10 is recommended. The 100 Ω resistor limits the peak discharge current into the SG1548, while the external PNP transistor provides a high peak-current discharge path for the delay capacitor.

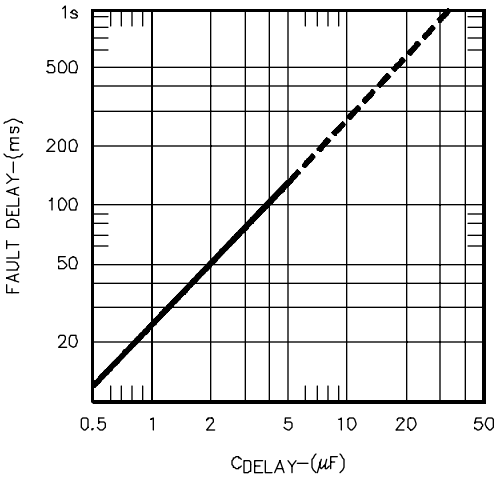


FIGURE 9. Graph of Fault Delay vs. Delay Capacitor

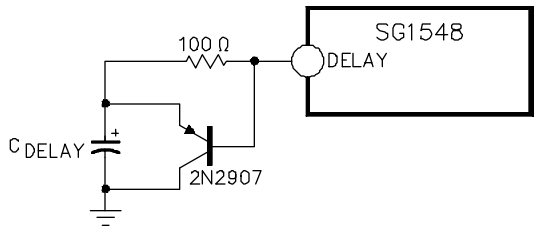
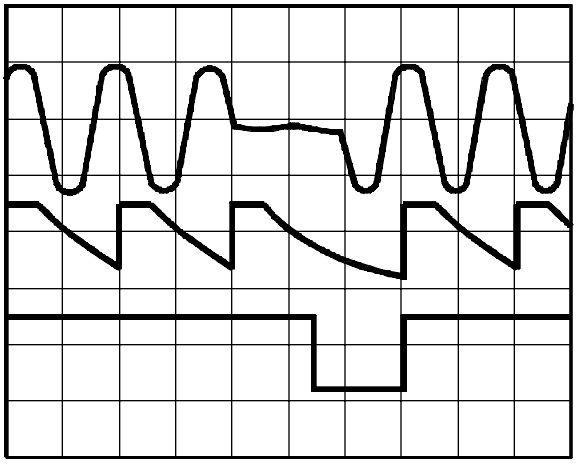


FIGURE 10. Surge Limit Circuit for Large Delay Capacitors

Monitoring the AC Line

Single-cycle AC line dropouts can be detected with the circuit shown in Figure 11. A positive half cycle is clipped to a precise level using the internal Zener and a 3 k source resistor. The discharge circuit consisting of 180 k and the 0.1 µF capacitor control the voltage decay so that the +2.5 V trip point is not reached with normal sinusoidal line conditions. A single-cycle dropout will provide an extra 16.7 ms discharge time, as shown in Figure 12, causing the Line Fault output to switch LOW.



HORIZONTAL: 10 ms/DIV
UPPER TRACE: AC LINE
MIDDLE TRACE: PIN 5 AT 5V/DIV.
LOWER TRACE: LINE SENSE OUTPUT AT 5V/DIV.

FIGURE 12. Response to a Single-Cycle Line Dropout

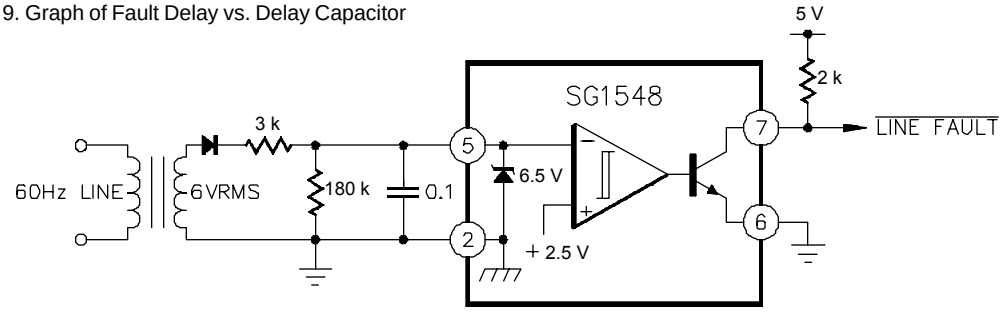


FIGURE 11. Monitoring the AC Line for Single-Cycle Dropout

Line Clock Generation

A logic clock derived from the line frequency can be obtained with a minimal number of components, as illustrated in Figure 13. The internal clamp diode is used in both forward and reverse conduction modes, with the 10 k input resistor limiting peak input current to less than 1 mA. Waveforms obtained with this circuit are shown in Figure 14.

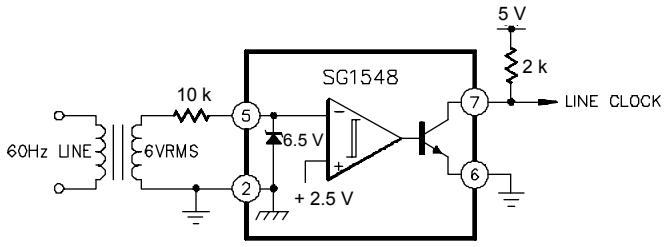


FIGURE 13. Generating an AC Line Clock

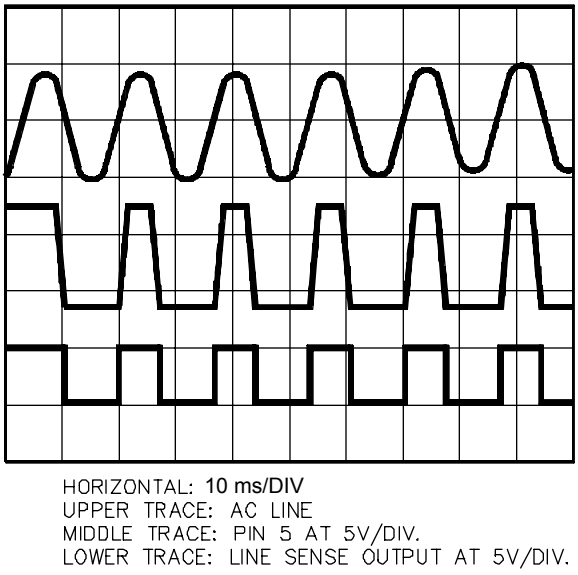


FIGURE 14. Waveforms Produced by the Line Clock

Undervoltage Lockout

Figure 15A and B shows two methods of using the Line Sense comparator for inhibiting power supply start-up until some minimum supply voltage has been reached. In the first case a HIGH-going shutdown signal to the PWM control is generated until V_{IN} causes the voltage at Pin 5 to exceed +2.5 V. If the PWM is on the primary side of the power transformer, the Line Sense Output can directly drive an optocoupler. In the second case the line sense comparator is used to gate a bias supply ON when the proper working voltage has been reached.

Expanding the Quad Power Fault Monitor

The SG1548 is readily expandable to include additional positive and negative supplies. One half of an inexpensive quad comparator IC is required for each supply, as shown in Figure 16.

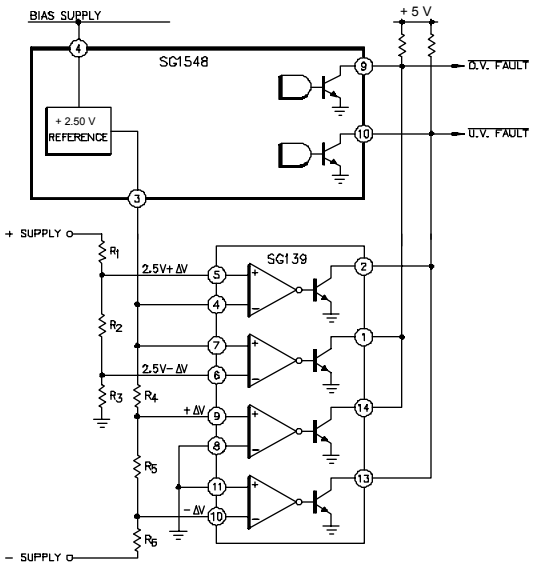
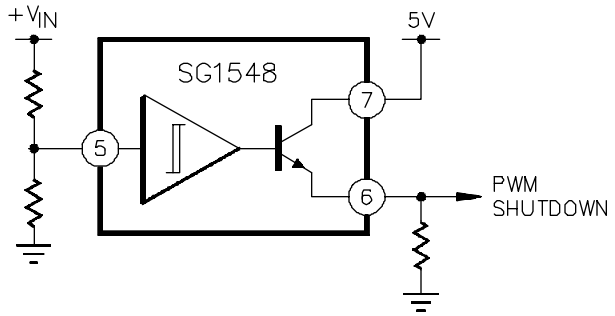


FIGURE 16. Expanding the SG1548 to Monitor Additional Supplies



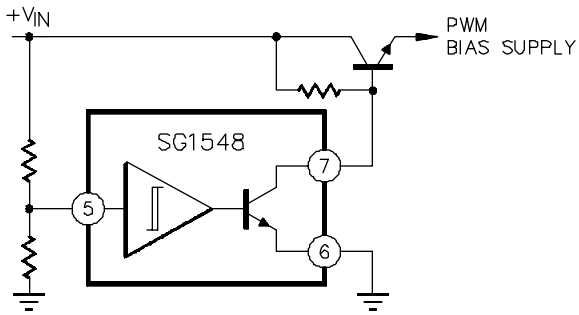


FIGURE 15A & 15B. Using the Line Sense for Undervoltage Lockout

For an additional positive supply, the comparators are referenced to the +2.5 V regulator of the SG1548. The monitored supply is divided down by resistors R1 through R3. When the supply drops a given percent, the upper comparator switches LOW. Since the fault outputs of the SG1548 are active LOW, the indication from the quad comparator can be wire-ORed to the undervoltage fault output line. Similarly, if the supply voltage increases beyond a preset limit, the overvoltage fault line will be pulled LOW by the second comparator.

The negative supply is handled similarly, except that the comparators are referenced to ground, and the resistive divider R4 through R6 is returned to the +2.5 V reference. The 139 quad comparator will work correctly as long as the inputs are not pulled below -0.3 V. If this possibility exists, a Schottky clamp diode should be used at Pin 10 to preserve the overvoltage indication in case of a massive negative overdrive at the divider input.

A Comprehensive Example

Each section of the SG1548 Quad Power Fault Monitor has been described in detail. Now it is time to put all the pieces together and show power supply supervision in an actual system. For our example we will use the hypothetical personal computer mentioned at the beginning of this paper. Figure 17 shows all the components required.

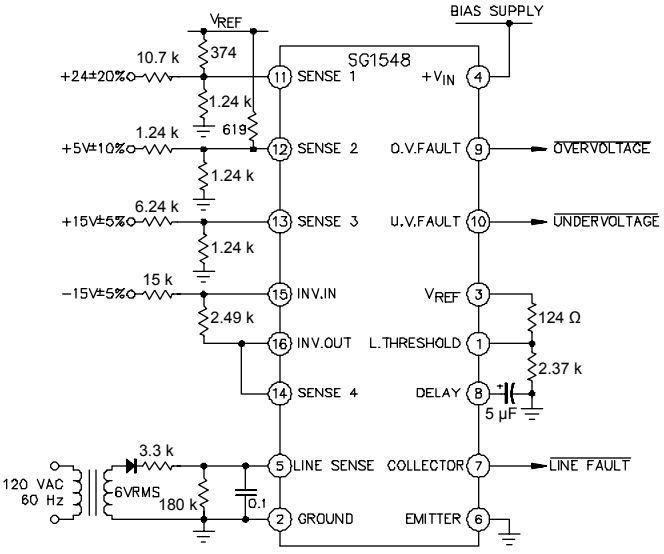


FIGURE 17. Monitoring Four DC Supplies and the AC Line

In this case, four DC voltages are monitored: three positive and one negative. Three different fault tolerances are mechanized, and the AC line is checked for single-cycle dropout.

The ±15 V supplies are the most critical, requiring ±5% accuracy. The 124 Ω/2.37 k divider from the reference sets this tolerance in the fault window generator. The -15 V supply is converted to +2.50 V with the inversion amplifier on the chip and applied to one of the Sense inputs. The +5 and +24 V supplies are not as critical, requiring ±10% and ±20% respectively. Divider resistors to the reference are used to scale the effective windows accordingly. The single 5 µF capacitor provides 125 ms of delay before an out-of-tolerance fault is reported.

All this is accomplished with one 16-pin integrated circuit and 14 resistors, 2 capacitors, a low-current diode, and a line isolation transformer, which can be part of the bias supply.

Conclusion

The opportunity to realize comprehensive power supply fault monitoring with low component count is a reality with the introduction of the SG1548 Quad Power Fault Monitor. A combination of flexible architecture combined with innovative circuit design techniques has resulted in a supervisory function with excellent accuracy and repeatability over the full military temperature range of -55°C to +125°C.

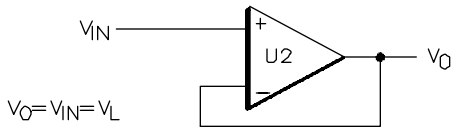
Appendix - A

Derivation of over voltage trip in terms of R_1, R_2, R_3, R_4, R_5
Looking at Figure 1:
Lower Threshold voltage is calculated by:

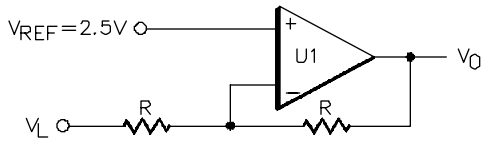
$$V_L = \frac{R_B}{R_B + R_A} V_{REF} = V_{REF} - \Delta V \quad (1)$$

$$\text{where } \Delta V = \frac{R_A}{R_A + R_B} V_{REF} \quad (2)$$

Op-amp (U2) is configured as a unity gain follower, therefore:



Upper threshold is calculated as:



$$V_O = (1 + \frac{R}{R}) V_{REF} - \frac{R}{R} V_L = 2V_{REF} - V_L$$

But V_L was calculated to be:

$$V_L = V_{REF} - \Delta V \quad (2\text{-a})$$

$$V_O = 2 V_{REF} - (V_{REF} - \Delta V) = V_{REF} + \Delta V$$

We will call the output of U1 op-amp upper threshold UMIT and designate it by V_U, so:

$$V_U = V_{REF} + \Delta V \quad (3)$$

Next we will analyze the circuitry associate with O.V sensing circuit. We also assume, it is required to have higher threshold voltage setting than the one being programmed by R_4, R_5 divider.

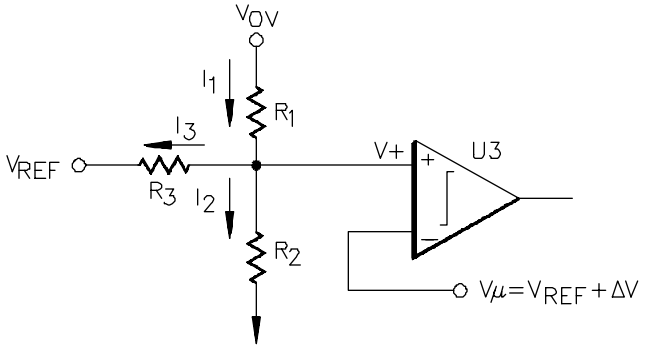


Figure 2

From the schematic of figure 2, we have:

$$V_T = V_U = V_{REF} + \Delta V$$

and writing K.C.L. for V_T node, we get:

$$I_1 = I_2 + I_3$$

$$\frac{V_{OV} - V_T}{R_1} = \frac{V_T}{R_2} + \frac{V_T - V_{REF}}{R_3}$$

$$\text{or : } V_{OV} = (1 + \frac{R_1}{R_2})(V_{REF} + \Delta V) + \frac{R_1}{R_3} \Delta V \quad (4)$$

$$\text{where } \Delta V = \frac{R_A}{R_A + R_B} V_{REF}$$

Equation (4) can only hold if the following is true:

(4-a) $I_2 >> I_{BIAS}$ where: I_{BIAS} is the bias current of U_3 comparator

and

(4-b) $I_3 < I_{SINK\ MAX}$ where: $I_{SINK\ MAX}$ is the maximum sink current capability of the reference voltage.

Derivation of equation for R_3:

Assumption:

V_{OV1} ≅ O.V trip point set by R_4, R_5 (lower threshold)
V_{OV2} ≅ O.V trip point desired ($V_{OV2} > V_{OV1}$)
x ≅ percent voltage above nominal for V_{OV1}
y ≅ percent voltage above nominal for V_{OV2}

From the definitions of x and y we get:

$$V_{OV1} = (x + 1) V_{NOM} \quad (7)$$
$$V_{OV2} = (y + 1) V_{NOM} \quad (8)$$

We also know that:

$$V_{OV1} = (V_{REF} + \Delta V)(1 + \frac{R_1}{R_2}) \quad (9)$$

and from equation (4)

$$V_{OV2} = (V_{REF} + \Delta V)(1 + \frac{R_1}{R_2}) + \frac{R_1}{R_3} DV \quad (10)$$

Replacing (7) and (8) into (9) and (10) and subtracting (9) from (10) we get:

$$(y - x) V_{NOM} = \frac{R_1}{R_3} \Delta V \quad (11)$$

or

$$R3 = \frac{R_1 R_2}{R_1 + R_2} \times \frac{1}{y - x} \times \frac{\Delta V}{V_{REF}} \quad (12)$$

We also know that the relation between V_L and V_{REF} is:

$$V_L = (1 - x)\, V_{REF} \qquad (13)$$

Since VL is x percentage lower than VREF by R3, R4 divider, putting (13) into equation (2-a) we get:

$$\Delta V = xV_{REF} \qquad (14)$$

Replacing (14) into (12) we get the result:

$$R3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)\left(\frac{1}{y - x}\right) \qquad (15)$$

Deriving a set of formulas for R_1, R_2, R_3 calculation:

From the inequality of 4-b we get:

$$R_3 >= \frac{\Delta V}{10^{-3}}\ \Delta V\ (KR) \qquad (16)$$

I_{BIAS} maximum for SG1548 comparator is 1 mA.

we know that:

$$V_{NOM} = \frac{R_2}{R_1 + R_2} \qquad (16\text{-a})$$

$$R1 = \left(\frac{V_{NOM} - V_{REF}}{V_{REF}}\right) R_2 = PR_2 \qquad (17)$$

$$\text{if} \quad P \cong \frac{V_{NOM} - V_{REF}}{V_{REF}}$$

From equation (15), (16) and (17) we get:

$$\left(\frac{x}{y - x}\right)\left(\frac{PR_2}{P + 1}\right) > \Delta V$$

$$\text{or } R_2 > (\Delta V)\left(\frac{P + 1}{P}\right)\left(\frac{y - x}{x}\right) \text{ where } R_2 \text{ [KR]} \qquad (18)$$

From equation (14) we have:

$$\Delta V = xV_{REF}$$

and replacing V_{REF} by 2.5 in equation 18) we get:

$$R2 > (2.5)(y - x)\left(\frac{P + 1}{P}\right) \qquad (19)$$

Using equations (17), (19) and (15) we can calculate R1, R2, and R3 values.

To calculate the reference sink current we use:

$$I_{SINK} = \frac{\Delta V}{R_3} = \frac{x\, V_{REF}}{R_3} = \frac{2.5x}{R_3}$$

To derive the equation for checking we start by equation (4):

$$V_{OV} = (V_{REF} + \Delta V)\left(1 + \frac{R_1}{R_2}\right) + \frac{R_1}{R_3}\Delta V$$

or

$$V_{OV} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) + \Delta V\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (20)$$

putting equation (8) in (20) we get:

$$V_{NOM} + yV_{NOM} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) + \Delta V\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (21)$$

Replacing (16-a) into (21) we get :

$$y = \frac{\Delta V}{V_{NOM}}\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right) \qquad (22)$$

Replacing (14) and (16-a) into (22) we get:

$$y = \frac{x}{\left(1 + \frac{R_1}{R_2}\right)}\left(1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}\right)$$

or

$$y = \left(1 + \frac{\frac{R_1}{R_3}}{\left(1 + \frac{R_1}{R_2}\right)}\right)$$

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at www.microsemi.com.