



Applications of the MT90502 Implementing I.366.1 SSCS on the MT90502 AAL2 SAR

Application Note

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1.0 Related Documents

Zarlink Semiconductor, "MT90502 Datasheet", DS5420, Issue 1, November 2001

ITU-T, "I.366.1 Segmentation and Reassembly Service Specific Convergence Sublayer for the AAL2 type 2", June 1998

ITU-T, "I.363.2 B-ISDN ATM Adaptation layer specification: Type 2 AAL", September 1997

Simpson, W., Editor, RFC 1662, STD.51. "The Point-to-Point Protocol (PPP)"

Motorola Inc, "MP8260 User's Manual", MPC8260UM/D

2.0 Overview

This document will discuss how to implement support for ITU-T standard I.366.1, framed mode data services, using the MT90502 SAR and HDLC encapsulation on the TDM bus.

3.0 MT90502 Introduction

The MT90502 is an AAL2 SAR (Segmentation and Reassembly) offering a highly integrated solution for interfacing telecom bus-based systems with an ATM network. It integrates a SAR engine that can process 1023 VCs (Virtual Circuits), a CPS (Common Part Sublayer) engine that can process 1023 CPS-packets, and two SSCS (Service Specific Convergence Sublayer) engines that can handle PCM and ADPCM voice respectively.

3.1 TDM Bus

The telecom bus implemented on MT90502 is an ECTF H.100 or H.110 compatible TDM bus consisting of 32 serial data streams running at 8Mbps. See Figure 1.

A block diagram of MT90502 is shown in MT90502 Block Diagram. PCM and ADPCM data are directly transported on the TDM bus. Each PCM or ADPCM channel occupies one entire timeslot, although ADPCM samples don't use all of the eight bits. Once the SSCS engines accumulate sufficient PCM or ADPCM samples from TDM bus, they will assemble those samples into the payload of a CPS-packet. The CPS engine will then complete the whole CPS-packet by adding a CPS-packet header that includes the CID, UII and LI fields. All completed CPS-packets are given to the SAR engine where they will be segmented and assembled into AAL2 cells. Finally, all AAL2 cells are transmitted out through one of the three UTOPIA ports.

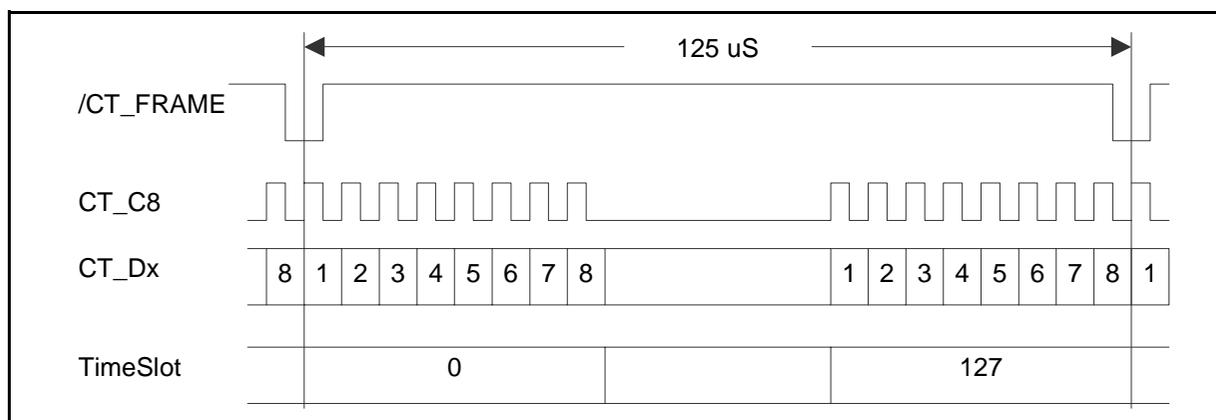


Figure 1 - H.100/H.110 TDM Bus Structure

The receive path performs the reverse process, with the AAL2 cells being reassembled into CPS-packets and the payload within the CPS-packets driven out onto the TDM bus.

As shown in the block diagram (MT90502 Block Diagram), the MT90502 can also send/receive CPS-packets (with or without a CPS-packet header) directly through the TDM bus. This is meant for those applications where other compression technologies (e.g. G.729 CS-ACELP or G.728 LD-CELP) are employed or for framed mode data services (ITU-T standard I.366.1). External compressors are responsible to generate CPS-packets (with or without a header) that will be handed over to MT90502 through the TDM bus. To enable the transportation of packets over a synchronous TDM bus like H.100, High Level Data Link Control (HDLC) protocol is supported by the MT90502.

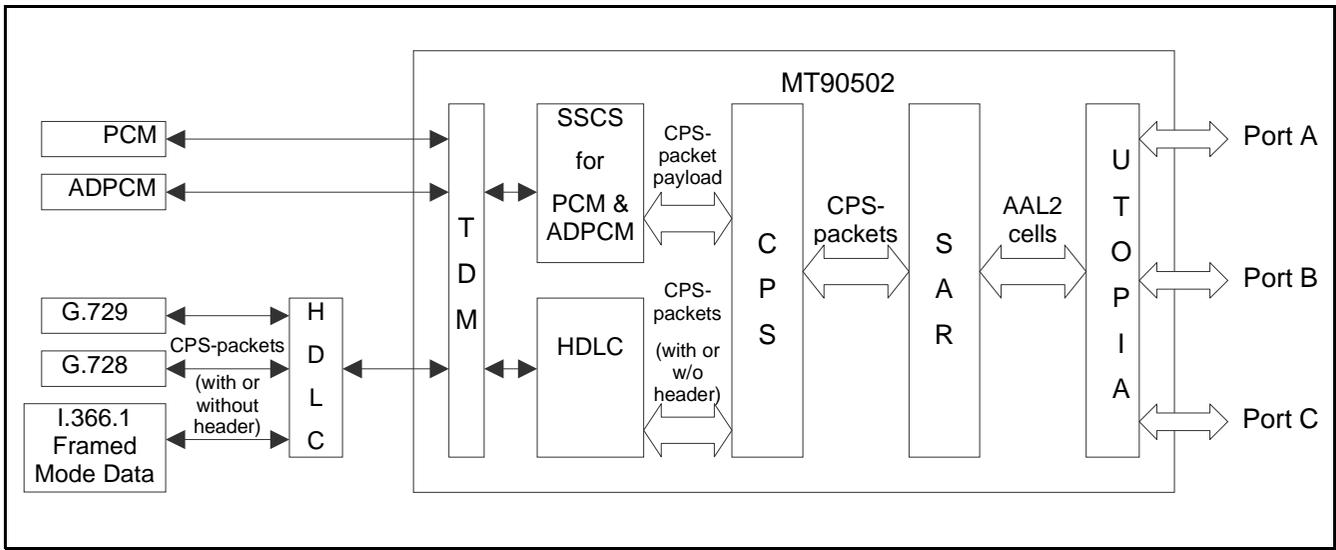


Figure 2 - MT90502 Block Diagram

Any consecutive TDM timeslots on a single data stream can be grouped as a single HDLC stream, over which one or more HDLC channels can be transported. An HDLC channel will carry CPS-packets destined to the same AAL2 channel. CPS-packets carried on the HDLC channel may or may not contain a header. The CPS-packet header can be appended in the CPS engine of the MT90502.

The MT90502 HDLC controller allows for two methods of transferring per-channel UUI information in an HDLC channel. First, the UUI can be embedded as the five MSB bits in the Control field of an HDLC frame. Second, the UUI can be included in the HDLC frame payload as part of a complete AAL2 CPS-Packet header. The HDLC protocol is discussed in greater detail in section 1.2.

1023 HDLC engines are implemented in MT90502 enabling the SAR to process 1023 HDLC channels simultaneously. To establish an HDLC channel with external device the exact same HDLC function implemented in the MT90502 shall be implemented on the external device. This HDLC approach brings us two main benefits. First, the TDM bus can be used for both CBR traffic like PCM/ADPCM, VBR traffic like G.729/G.728 and framed mode data services (I.366.1). Second, there is a wide range of flexibility in allocating bandwidth to HDLC channels (up to 8.192Mbps).

3.2 HDLC

HDLC methodology is widely used in telecommunication to facilitate transportation of asynchronous data through a synchronous serial bus. One example is T1/E1 Common Channel Signalling (CCS) where signalling packets are HDLC encapsulated before being inserted into T1/E1 channels. A generic HDLC format is shown in Generic HDLC format. A typical HDLC frame will contain a starting and an ending flag, one or two address bytes, one control byte, and two CRC bytes, in addition to the data (or payload) field. The payload data between a start flag and an end flag represents one complete CPS-packet.

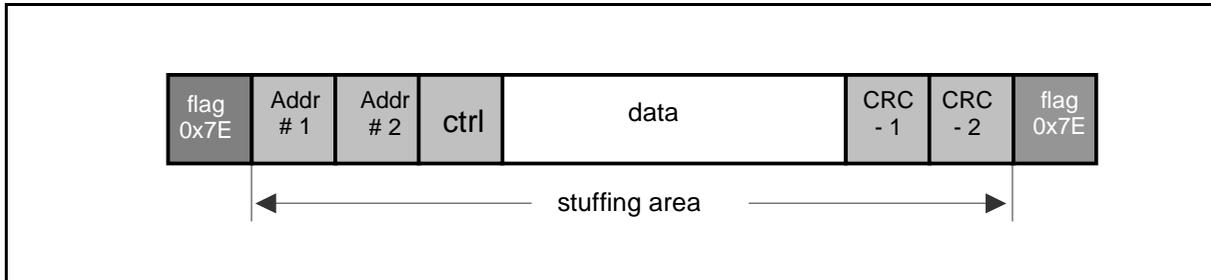


Figure 3 - Generic HDLC format

In order to eliminate any mimics of flags, data between the starting and ending flags are subject to stuffing. Two stuffing methods, bit stuffing and byte stuffing, are widely accepted. In bit stuffing, the whole stuffing area is scanned bit by bit while a zero is inserted after every 5 ones. Byte stuffing, however, is based on the assumption that the whole HDLC frame is byte aligned. It replaces any 0x7E within stuffing area with 0x7D5E, and replaces any 0x7D with 0x7D5D. Byte stuffing is more favourable than bit stuffing in terms of computation, because it searches for each byte individually instead of each bit.

When included, CRC bytes are calculated over the address bytes, the control byte and the data field by using CRC-16 (polynomial $x^{16}+x^{12}+x^5+1$) scheme. The initial CRC value at reset is FFFFh and it is XORed with F0B8h before being sent.

The HDLC controller on MT90502 has the flexibility to support various HDLC formats, whether it is bit stuffing or byte stuffing. The presence of address byte(s), control byte and CRC bytes are all optional. The simplest formats will be similar to The simplest HDLC format supported by MT90502.

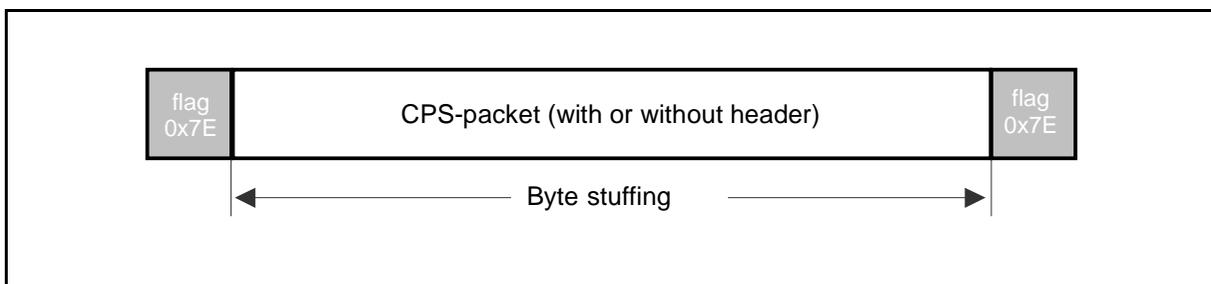


Figure 4 - The simplest HDLC format supported by MT90502

3.3 Framed Mode Data

ITU-T standard I.366.1 specifies a Segmentation and Reassembly SSCS (SEG-SSCS) protocol for AAL2 that allows for support of signalling and data packets. These packets may exceed the maximum length of 64 bytes for an AAL2 CPS-packet specified in ITU-T standard I.363.2. This type of traffic is referred to as framed mode data. One popular usage of I.366.1 framed mode data is to carry PSTN signalling packets over AAL2 cells in voice gateway or 3G wireless applications.

3.4 Protocol Stack

The AAL2 protocol stack consists of both the SEG-SSCS layer and the CPS layer. Example CCS Protocol Stack shows an example protocol stack for V5 CCS over AAL2. The AAL2 layer is below the application layers and above the ATM layer. The SEG-SSCS layer consists of the Service Specific Assured Data Transfer sublayer (SSADT), the Service Specific Segmentation and Reassembly sublayer (SSSAR), and the Service Specific Transmission Error Detection sublayer (SSTED).

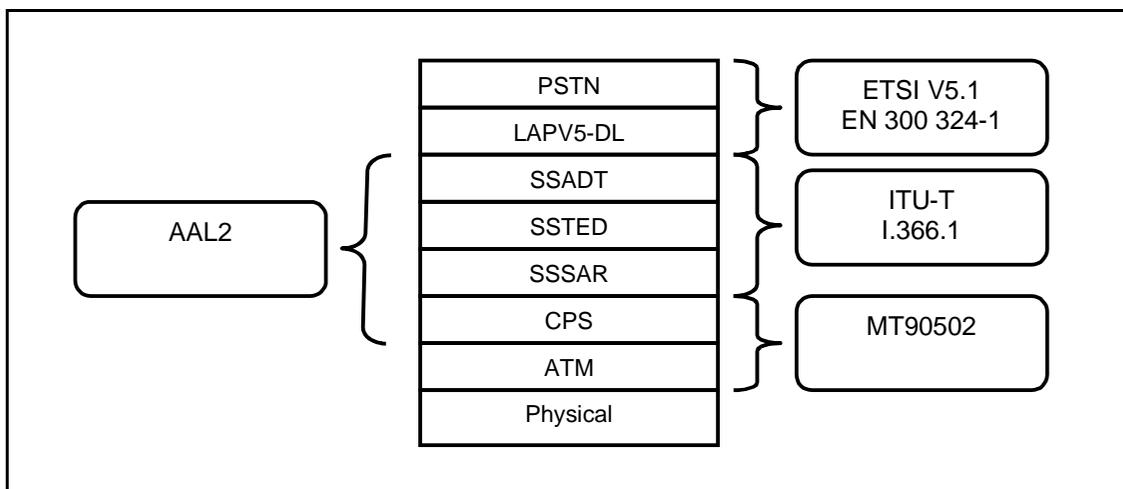


Figure 5 - Example CCS Protocol Stack

As indicated in the figure, the MT90502 will perform the CPS portion of the AAL2 protocol as well as the ATM protocol. The MT90502 exchanges from the SSSAR a CPS-packet payload (maximum 64 bytes in length) as well as the UUI codepoint value. If multiple UUI codepoints are not required by the SSSAR, a value of 26 is used to indicate that the CPS-packet is the last packet in the SSSAR-SDU and a value of 27 is used to indicate there are more CPS-packets to complete the SSSAR-SDU.

3.5 CPS Interface

The TDM interface can be thought of as a physical Service Access Point (SAP) between the SSSAR sublayer and the CPS layer. HDLC Interface between MPC8260 and MT90502 AAL2 SAR shows a block diagram of a Motorola MPC8260 processor interfacing the MT90502 via the TDM bus. The data on the bus is HDLC encapsulated. The encapsulated data may either be the complete CPS-packet (as shown in The simplest HDLC format supported by MT90502) or the CPS-packet payload with the UUI value encoded into the 5 MSB bits of the Control Field (example packet shown in Generic HDLC format).

3.6 Microprocessor

Any SAR processing board usually has a microprocessor to control the SAR device, such as the MT90502, and other components on the board. The microprocessor is also responsible for the high layer software stack. Motorola's MPC860 or MPC8260 are popular choices as the microprocessor. The MPC8260 has a serial TDM port that can be gluelessly connected to the H.110 bus on the MT90502. HDLC encapsulation can be easily implemented on the processor. Additionally, some commercial packages are available to implement I.366.1 on an MPC8260. The flexibility of the local interface and the high density of MT90502's voice capacity make HDLC Interface between MPC8260 and MT90502 AAL2 SAR an attractive solution for high-bandwidth voice and framed mode data over AAL2.

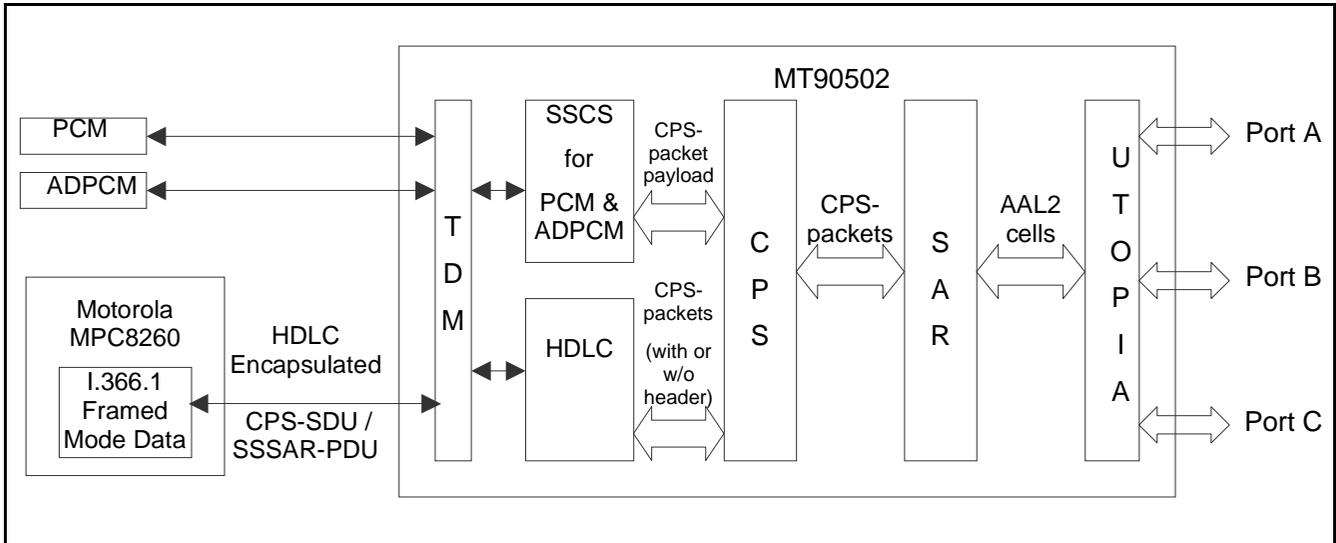


Figure 6 - HDLC Interface between MPC8260 and MT90502 AAL2 SAR

4.0 Conclusion

Through the flexible TDM interface the MT90502 is able to communicate with either DSPs or microprocessors to transfer variable bit rate channels or data, while still allowing for PCM and ADPCM voice to be handled directly from the TDM bus. The HDLC interface as described in the preceding sections has proven to be an effective way of transferring CPS-packets created using a variety of SSSCS engines. A solution to meet the ITU-T I.366.1 framed mode data specification can be achieved using an external agent to implement the SSSCS portion of the standard while using the MT90502 to implement the CPS portion of the standard.



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