ZLAN-72

Applications of the MT90502 CPS-Packet Switching

Application Note

November 2003

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1.0 Introduction

This technical note explores the possibility of using Zarlink's MT90502 AAL2 SAR device to switch CPS-packets. Some key performance indicators like throughput delay and capacity are also discussed.

2.0 Implementation

We are trying to build an exchange that can switch ATM traffic on an OC-3 link at both the cell level and the CPS-packet level.

Figure 1 shows the block diagram of our implementation using two MT90502 chips.

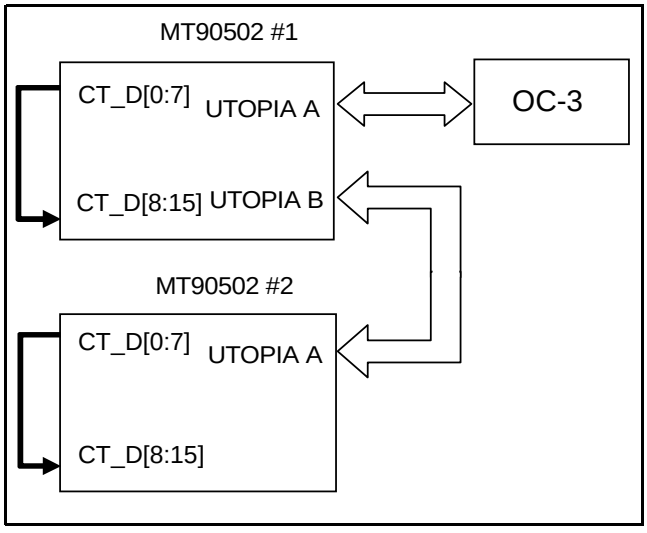

Figure 1 - Block Diagram

2.1 Cell Switching

The MT90502 has a built-in feature to allow cell switching at its UTOPIA ports. Any ATM cell received at a UTOPIA input port can be routed back to any UTOPIA output port according to its VPI/VCI. Moreover, its VPI/VCI could be over-written by a new value. In Figure 1, any cell that enters UTOPIA port A of MT90502 #1 from the OC-3 PHY can be:

- received by MT90502 #1 as an AAL2 VC,
- switched back to the OC-3 PHY with VPI/VCI changed or unchanged, or
- switched to MT90502 #2 through port B.

2.2 CPS-Packet Switching

The AAL2 SAR engine inside the MT90502 can process 1023 VCs simultaneously. CPS-packets reassembled from VCs will be processed by a Rx CPS engine, where a total of 1023 CIDs can be handled. The Rx CPS engine will put a CPS-packet onto the TDM bus with HDLC encapsulation. The format of the HDLC encapsulation is shown in Figure 2. Address bytes are used to indicate HDLC channels. One HDLC channel carries one CID. Byte stuffing is performed over the CPS-packet and HDLC address bytes to eliminate any mimic of the HDLC flag.

The TDM bus on the MT90502 contains 32 high speed streams (CT_D[0:31]) running at 8.192 Mbps. This gives as many as 4096 timeslots. However, the MT90502 can only access 2046 of them - 1023 Tx timeslots and 1023 Rx timeslots. In our implementation, the first eight (CT_D[0:7]) streams are configured as output (Rx) streams, and the second eight (CT_D[8:15]) are input (Tx) streams. Each output stream is physically connected to an input stream, so that all CPS-packets on TDM bus get looped back. The remaining streams (CT_D[16:31]) are unused.

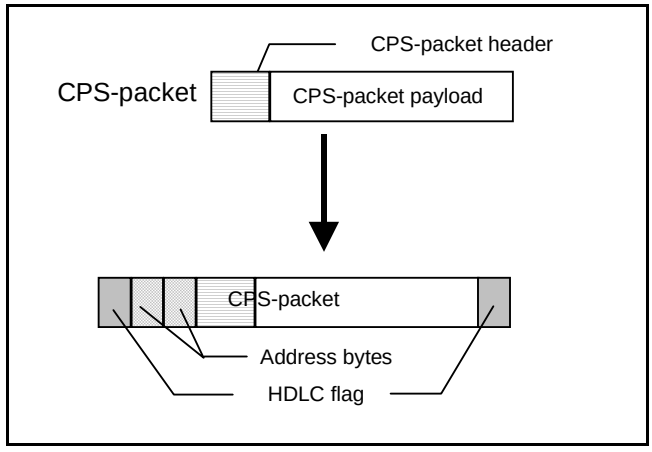

Figure 2 - HDLC Packet

There are 128 available timeslots on each stream. One or more consecutive timeslots can be assigned to a single HDLC stream in which multiple HDLC channels or CIDs are transported. Again, HDLC channels or CIDs in the same HDLC stream are distinguished by the address bytes in the HDLC frame.

In our implementation, only one HDLC stream is created on each TDM stream. Each HDLC stream will cover all the available timeslots on that stream. Because there are 1023 usable timeslots per direction, the first seven HDLC streams on CT_D[0:6] will each have 128 timeslots, and the last HDLC stream on CT_D[7] has 127 timeslots. In other words, there are 8 HDLC streams on TDM bus, each has bandwidth of 128 timeslots or 8.192 Mbps except for the last one.

On the TDM input (Tx) side, 1023 HDLC engines are available to receive all HDLC channels from the 8 HDLC streams. CPS-packets will be retrieved from HDLC encapsulation and passed over to the proper Tx CPS engine according to the HDLC stream number and the HDLC address bytes.

In the Tx CPS engines, both the CID and UUI fields of the CPS-packets can be modified by the user, if desired, before the packets are sent to the Tx SAR engine. In the Tx SAR engine the CPS-packets are segmented into AAL2 cells. Again, the VPI/VCI are user programmable.

Figure 3 shows a complete data flow from UTOPIA to TDM back to UTOPIA. By changing the CID/VPI/VCI on the Tx side the CPS-packets are switched among VCs.

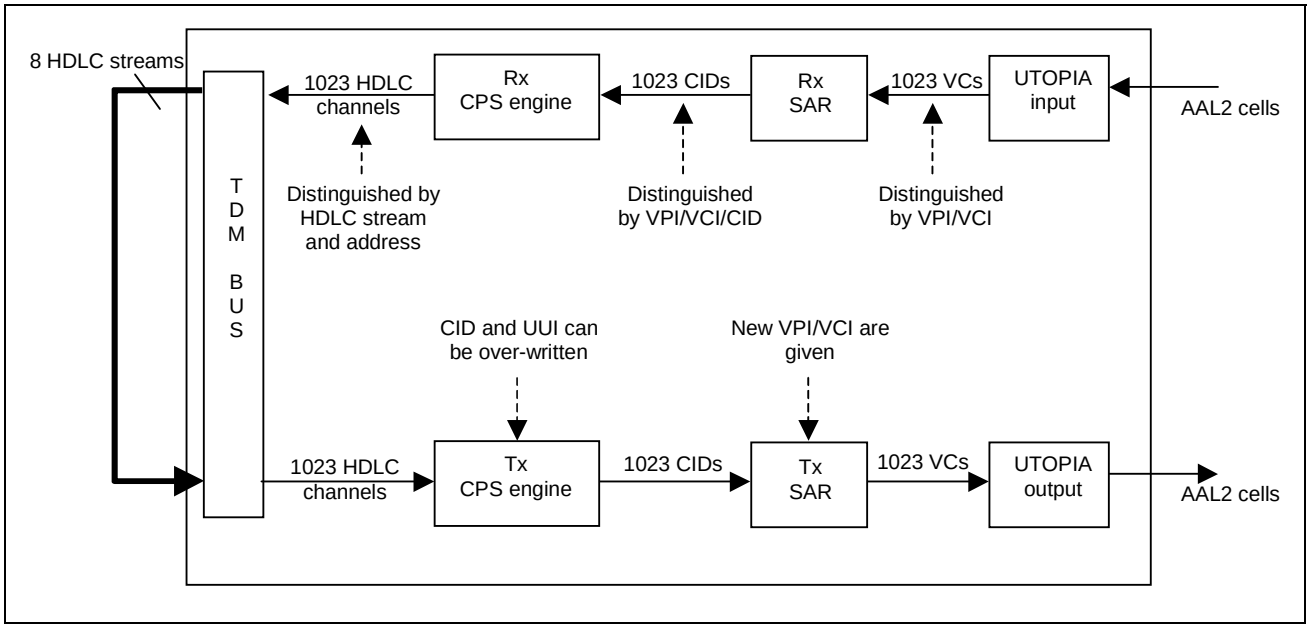

Figure 3 - Data Flow of CPS-Packet Switching

3.0 Delay and Capacity

3.1 Throughput delay

On the MT90502, the total throughput delay from UTOPIA input to UTOPIA output comprises:

- Process delay from the UTOPIA input to the TDM interface, totalling 250us.
- Transportation delay on the TDM bus. The TDM bus is running at 8.192 Mbps or 122ns per bit. Since multiple HDLC channels may share a single HDLC stream, the transportation delay of a HDLC packet depends on the number of HDLC channels (N) in this stream as well as the CPS-packet length (L). The delay is N*(L*1.1+3)*8*122ns. Here, we have a multiplier of 1.1 as a result of byte stuffing and we add 3 bytes for the HDLC flag and address.
- Process delay from the TDM interface to the UTOPIA output, which is 125us.

3.2 Capacity

Although the MT90502 supports 1023 HDLC CIDs or HDLC channels, the bottleneck of our implementation is on the TDM bus. The number of HDLC channels that can be carried by an HDLC stream (which has 8.192 Mbps bandwidth) depends on the packet size and the packet rate. If the average CPS-packet length is L bytes, the average packet rate is R packets/s, and the number of HDLC channels in a single HDLC stream is N, we will have the total traffic of N*R*(L*1.1+3)*8 bits/s that will appear on the TDM bus. Obviously, this traffic cannot exceed the 8.192 Mbps bandwidth limitation. Therefore, we have

$$N \le \frac{1024000}{R \times (L \times 1.1 + 3)}$$

Since the above N is the capacity of a single HDLC steam, multiply it by 8 to get the total capacity of a single chip. Again, multiply it by 2 to get the total capacity of our implementation as shown in Figure 1.

Table 1 summarizes the results of capacity and delay for some PCM and ADPCM profiles.

Profile	L (byte)	R (packet/s)	Capacity	Delay (ms)
40 byte PCM	43	200	1616	5.3
			1024	3.5
			512	1.9
			256	1.2
32K ADPCM	23	200	2046	3.9
			1024	2.1
			512	1.3
			256	0.8
44 byte PCM	47	181.2	1648	5.9
			1024	3.8
			512	2.1
			256	1.2

Table 1 - Delay vs. Capacity

4.0 Conclusion

An AAL2 switch is proposed by using two MT90502 SAR devices. The CPS-packet capacity and throughput delay are discussed. The smaller the capacity used on the MT90502, the smaller the round trip delay. However, by using compressed data like ADPCM or CELP, we can achieve both high capacity and low delay.

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