ZLAN-71

Applications of the Digital PLLs
Design Guidelines for Using Oscillators

Application Note

December 2003

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1.0 Introduction

A reference oscillator is required to drive the clock circuits of a timing IC such as the ZL30407. The accuracy of the PLL and its ability to meet stringent requirements such as Telcordia GR-253 and ITU-T are dependent on the behaviour of the reference oscillator.

Two types of oscillators are used with Zarlink synchronization I.C. devices, the TCXO (temperature compensated crystal oscillator) and the OCXO (oven compensated crystal oscillator). Each type uses a crystal to generate the desired frequency. The two types differ in the method used to maintain a constant output frequency over a range of ambient temperature.

Neither solution provides a perfectly temperature invariant output, but the OCXO offers higher performance, albeit at greater cost, power consumption and size.

This application note gives best practise advise on how to obtain the optimum performance for the choosen oscillator. The manufacturers datasheets should be consulted for details of external components selection and further guidelines.

2.0 Power Considerations

The oscillator's power supply should be filtered using the techniques described above, in accordance with the sensitivity of the device to power supply noise.

- A local power plane or bus and power filtering should be used to isolate the device from external power noise sources, unless power supply noise sensitivity is specified otherwise by the device manufacturer.
- In the case of an OCXO, local bulk capacitors must be provisioned large enough to handle changes in current due to its internal heating unit turning on and off.

3.0 Thermal Behaviour

A TCXO is more sensitive to changes in ambient temperature conditions than an OCXO. Under steady state conditions, oscillators should perform within their declared specifications. A steady state is reached after a "warm-up" period that includes the oscillator and circuit board on which it is mounted, under conditions of constant temperature and airflow.

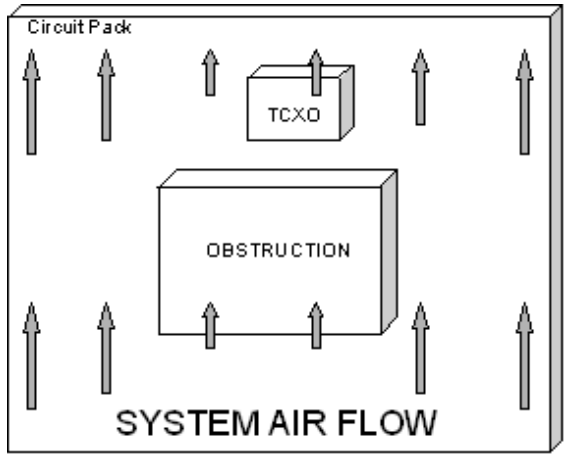
When the airflow or ambient temperature changes, the device's internal compensation mechanisms kick in and attempt to adjust the internal conditions. Compensation occurring within the device shows up as small variations of phase and frequency in the output clock.

In the case of a TCXO, temperature compensation is electrical, and seeks to offset the effect of a temperature change on the physical crystal. The OCXO attempts to maintain a constant temperature environment around the crystal, using a heater to sustain an internal temperature that is above the maximum rated external ambient temperature.

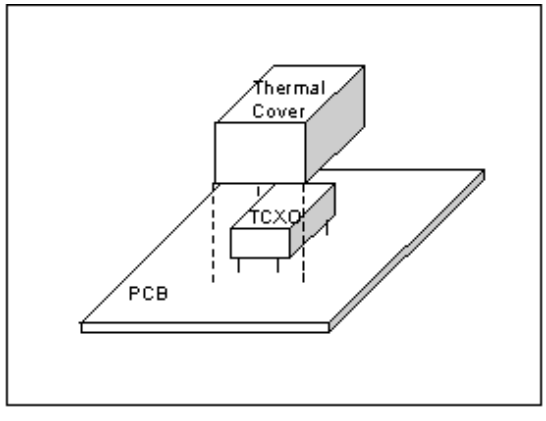
Each type is a closed loop system with a built in lag in its compensation response, with the net result being some variation in the output frequency. Devices with digital compensation loops also show "staircase" effects in the output phase and frequency adjustment, in accordance with the discrete resolution.

When designing an oscillator into an application, every measure should be taken to mitigate the effects of external air flow and temperature on the device.

- Try to place the oscillator where air flow is over the board is reduced by obstructions such as other tall devices, mechanical parts, etc… A mechanical baffle can be used to divert air away from the device if required. If an airflow model is available for the circuit pack and/or the system, this can be helpful in selecting a low air flow site for the oscillator. Local air flow is also influenced by the placement of components on adjacent boards, fans, and exit vents for example.



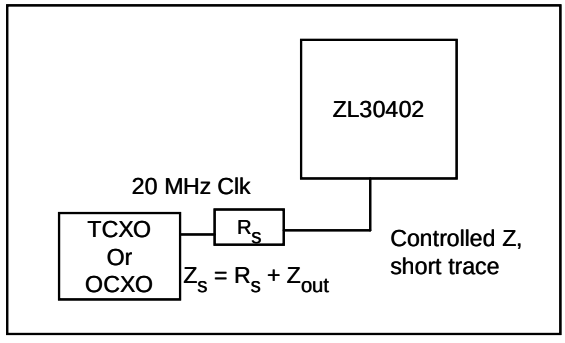
- A plastic or metal shroud can be designed to fit over top of a TCXO to provide a layer of insulation from sudden temperature changes. In general, OCXO devices should not require a cover, but this may not hold true for the newer, smaller form factor designs. It is important to note that any such improvised solution must still allow the device to operate well inside its recommended temperature range under all environmental conditions.



4.0 Oscillator - Timing PLL Interconnection

Signal integrity is a prime consideration for the signal interface between the timing PLL and the reference oscillator. The oscillator output is low jitter, and the objective is to avoid adding to the signal between the oscillator and PLL input pin.

- Co-locate the timing PLL and reference oscillator so that signal trace route length can be minimized. The oscillator output is single ended, and thereby vulnerable to crosstalk.
- Connect the oscillator directly to the timing PLL. Avoid using buffers between them, if possible. If a buffer must be used, select a technology that will add as little noise as possible.
- Provide pads for a series termination resistor on the oscillator output, in case a resistance must be inserted to eliminate signal over/undershoot by impedance matching.



The equation is $Z_S = R_S + Z_{out}$, where Z_S is the total source impedance, R_S is the series termination resistor value, and Z_{out} is the oscillator's signal output impedance.

Z_S should match the characteristic impedance of the trace (typically 50 ohms) connecting the oscillator to the DPLL.

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