ZLAN-57

ZL50211
2048 Channel VEC System

Application Note

Contents

August 2003

The design contained within this document is intended as reference material only, and not as a fully qualified system. It is intended to be used as a starting point for a customer design.

1.0 General Overview

This document describes the design of a 2048 channel voice echo canceller daughtercard using the ZL50211 256 channel device as a building block. The input/output stream rate from the daughtercard is assumed to be 16Mbps. The card is intended to make itself as transparent to the user as possible. To this end, it can be treated by the user simply as a single device which 16 streams at 16M (containing RIN and SIN VEC data), and outputs 16 streams at 16M (containing ROUT and SOUT VEC data). It uses an 8 bit data bus (D[0..7]) and a 19 bit address space (A[0..19]).

2.0 Rate Conversion

The ZL50211 has a 2Mbps TDM interface. With the system supplying TDM data at 16Mbps, there must be some rate conversion implemented on the daughtercard. Rate conversion from 16M to 2M and back again can be handled in several different ways, either in FPGAs/CPLDs or TDM switches.

In the case of the TDM switches, 4 MT90869 switches could be used to rate convert. This would add 6 frames of delay (750us) to the system, in addition to the delay through the VEC.

Using shift registers in a CPLD or FPGA, this delay can be reduced to a 7.8us delay (16 16M channels). This minimizes delay through the VEC matrix, but adds complexity to the channel allocation of the system. For instance, channel 0 on a 16M stream will be output at channel 16 from the VEC matrix. This is a reasonable trade-off to make in many cases.

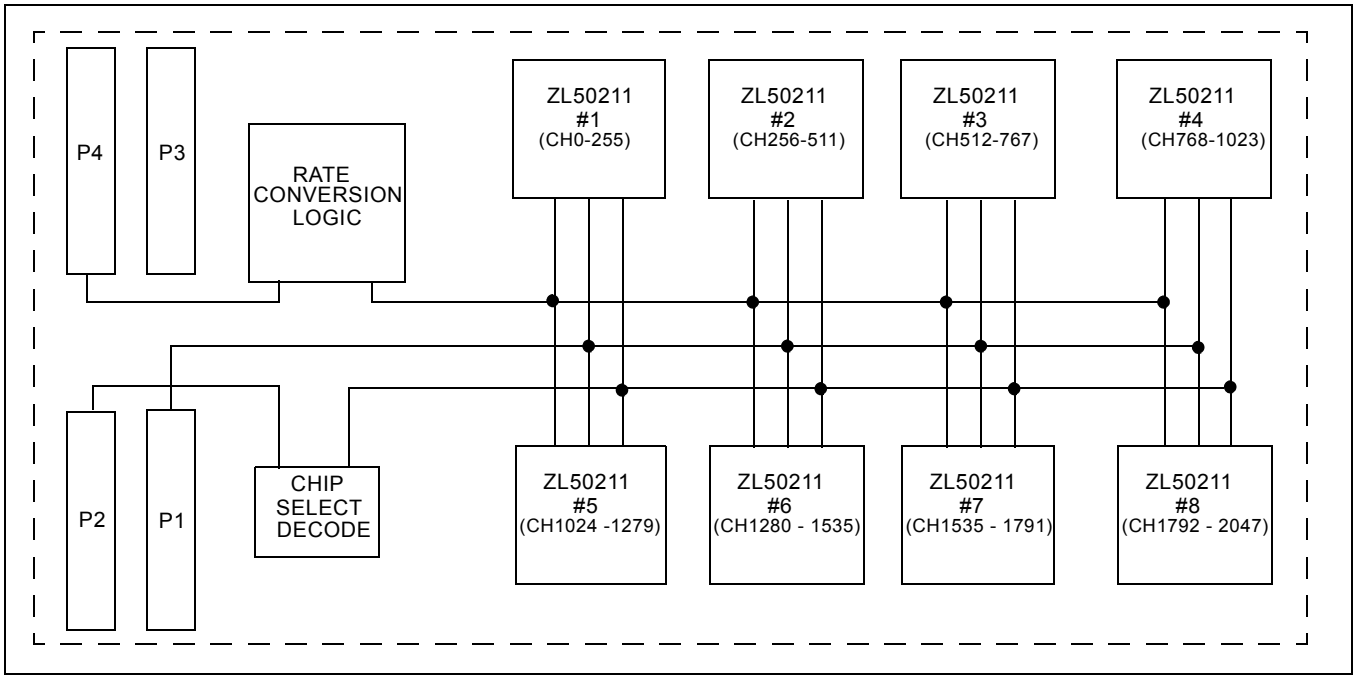


Figure 1 - Overview of 2048 Channel Daughtercard

Several diagrams (Figures 2-4) are included in this document showing how these shift registers should be implemented logically. The HDL code is not included, but a separate document is available which shows the complete design of a 16M to 8M conversion design. This document can be used as a starting point in order to develop the 16M to 2M design.

If using programmable logic with built-in ram like most FPGAs now have, it is more efficient to use this ram and counters rather than implementing shift registers in flip flops. This is left as an exercise for the reader. Zarlinks' application support team is available to customers to help design a system such as this.

3.0 Address Decoding

The ZL50211 is a multi-chip module with 8 ZL50232 dies packaged into a single device. Some of the signals have been combined to single pins (for example, address and data lines) whereas other lines are brought out separately for each device (for example, the chip select lines). Depending on the system design, this can be inconvenient when dealing with some of the pins (CS, IRQ, nDTA, RESET). When using multiple ZL50211s, these problems can escalate. For instance, when using 8 ZL50211s (such as in this design), there are 64 chip select lines to deal with.

This design shows how simple 3-to-8 decoders can be used to map the chip selects to a more convenient address space. 6 address lines are decoded to create the necessary chip select lines. This can be seen on sheet 5 of the schematics. This is shown as discrete components on the schematics for clarity.

A18	A17	A16	A15	A14	A13		
0	0	0	0	0	0	= VEC 1,	DIE 1
0	0	0	0	0	1	= VEC 1,	DIE 2
0	0	0	0	1	0	= VEC 1,	DIE 3
0	0	0	0	1	1	= VEC 1,	DIE 4
0	0	0	1	0	0	= VEC 1,	DIE 5
0	0	0	1	0	1	= VEC 1,	DIE 6
0	0	0	1	1	0	= VEC 1,	DIE 7
0	0	0	1	1	1	= VEC 1,	DIE 8
0	0	1	0	0	0	= VEC 2,	DIE 1
0	0	1	0	0	1	= VEC 2,	DIE 2
0	0	1	0	1	0	= VEC 2,	DIE 3
0	0	1	0	1	1	= VEC 2,	DIE 4
..	.	.					
1	1	1	1	0	0	= VEC 8,	DIE 5
1	1	1	1	0	1	= VEC 8,	DIE 6
1	1	1	1	1	0	= VEC 8,	DIE 7
1	1	1	1	1	1	= VEC 8,	DIE 8

A18-A16 = VEC #, A15-A13 = DIE #,
A12-A0 = Normal VEC addressing

Table 1 - Address Decoding Matrix

IRQ, nDTA and RESET are simply tied together and presented to the system as a single line. This assumes that all VECs will be reset at the same time and that only one VEC will be accessed by the microport at any particular time. This is consistent with the goal of making the VEC matrix appear as a single device. With the interrupts all tied together, the system will only have to monitor a single line in order to deal with tone detections. This does mean that it will have to poll the system to find which VEC core is causing the interrupt. At worst case, this means that 64 reads will have to be performed in order to find which channel is causing the IRQ.

4.0 Conclusion

As can be seen, it is relatively straightforward to design a 2048 channel card using the Zarlink ZL50211. The design is flexible enough to form the basis of an industry standard echo canceller card. For instance, a PICMG 2.15 type 2 card offers an H.110 like bus running at 8Mb/s with a PCI address/data bus to control the card. By dropping the rate conversion mentioned here to 8M and adding a PCI bridge, this design can be easily extended to a full PICMG 2.15 or P1386 mezzanine style card.

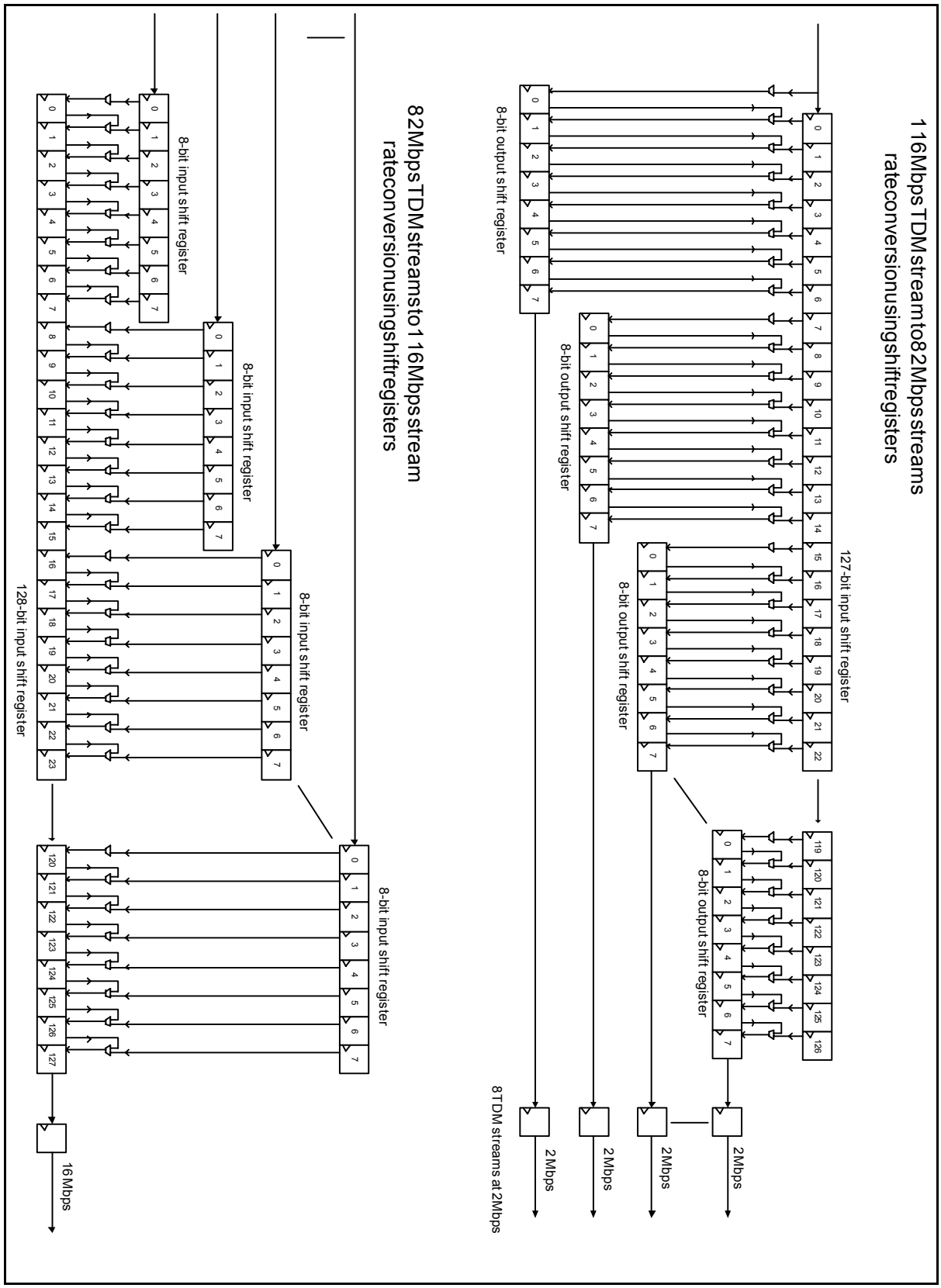


Figure 2 - Rate conversion using shift registers

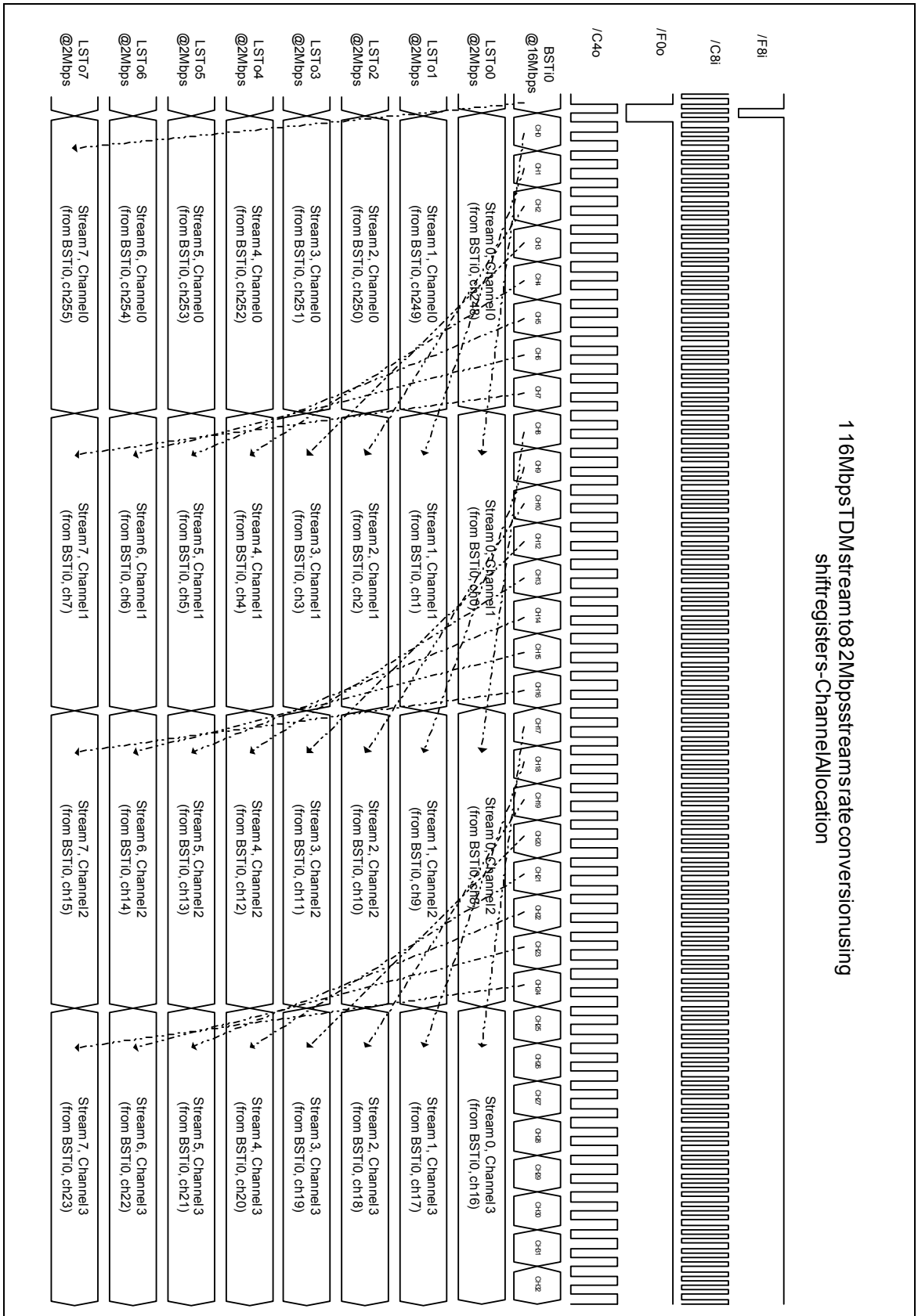


Figure 3 - 16Mbps to 2Mbps Channel Allocation

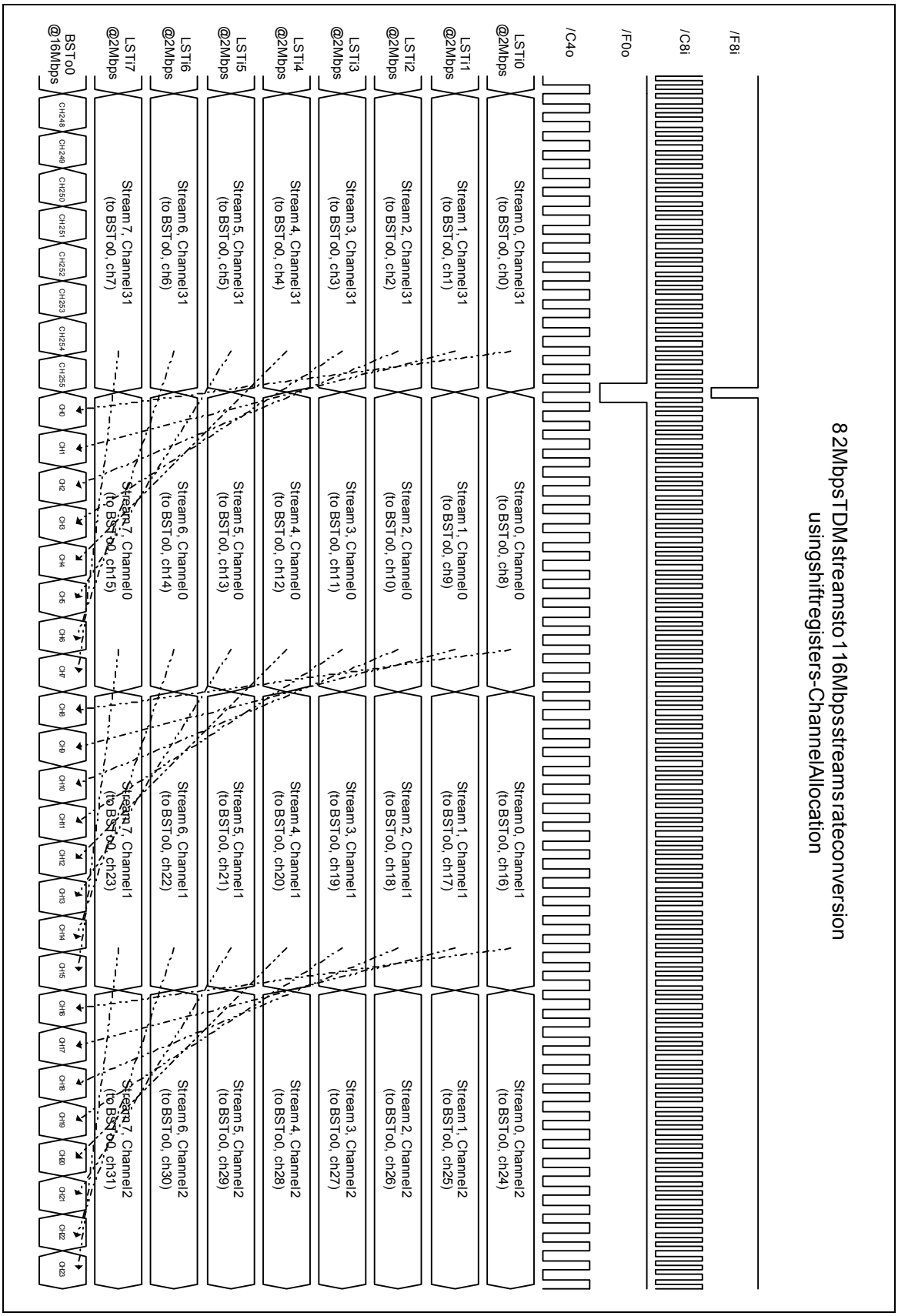
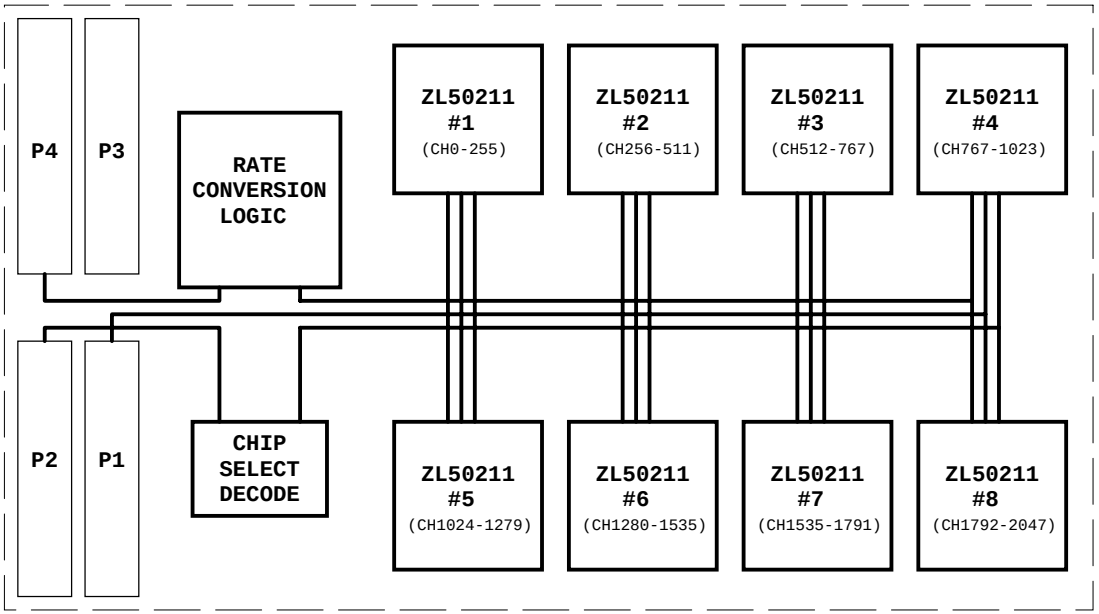


Figure 4 - 2Mbps to 16Mbps Channel Allocation

2048 CHANNEL VOICE ECHO CANCELLOR SAMPLE DESIGN
(SHOWN AS A DAUGHTERCARD WITH 16Mbps INTERFACE)



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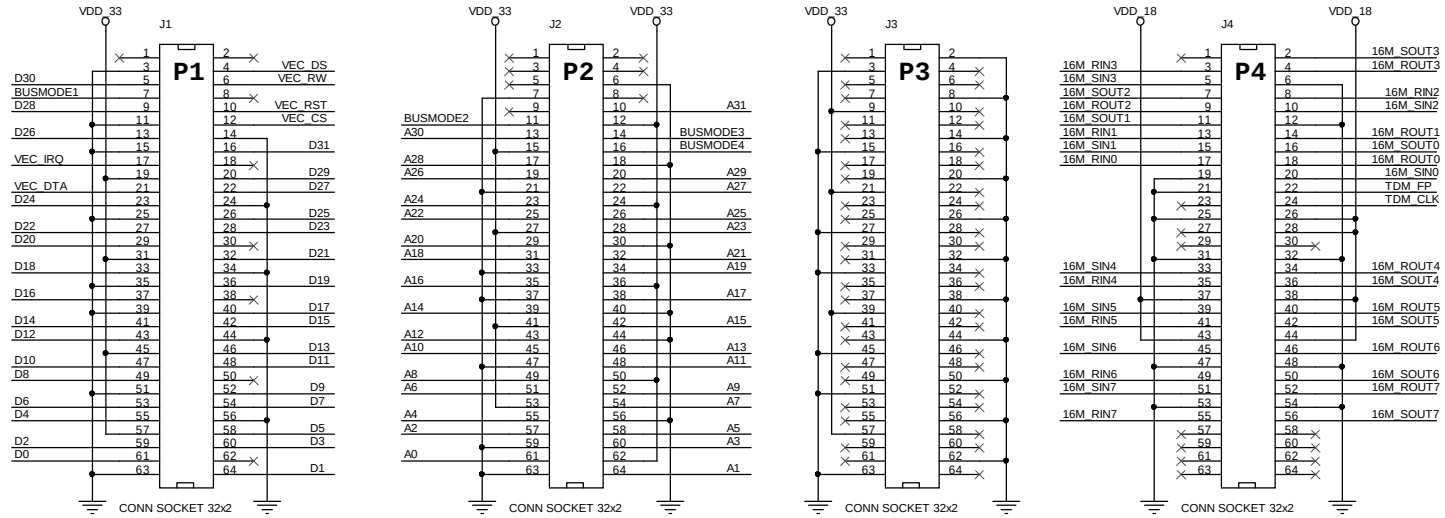
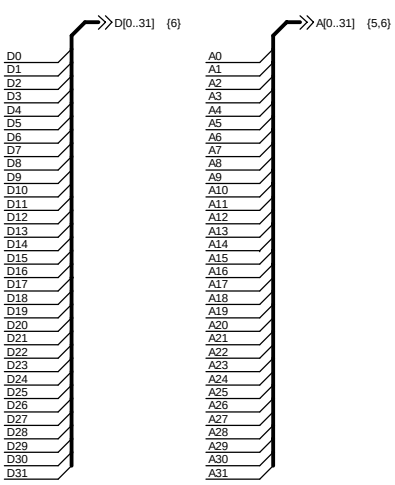
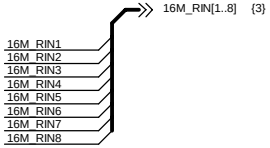
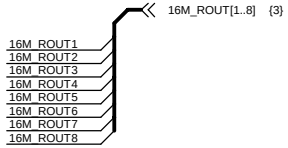
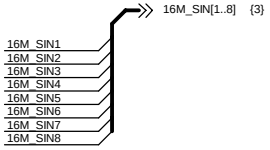
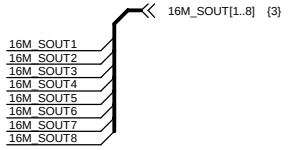


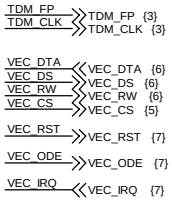




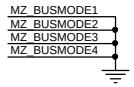








NOTE: These headers follow the Coherent module signalling style, which is based from P1386/P1386.1/PICMG2.15



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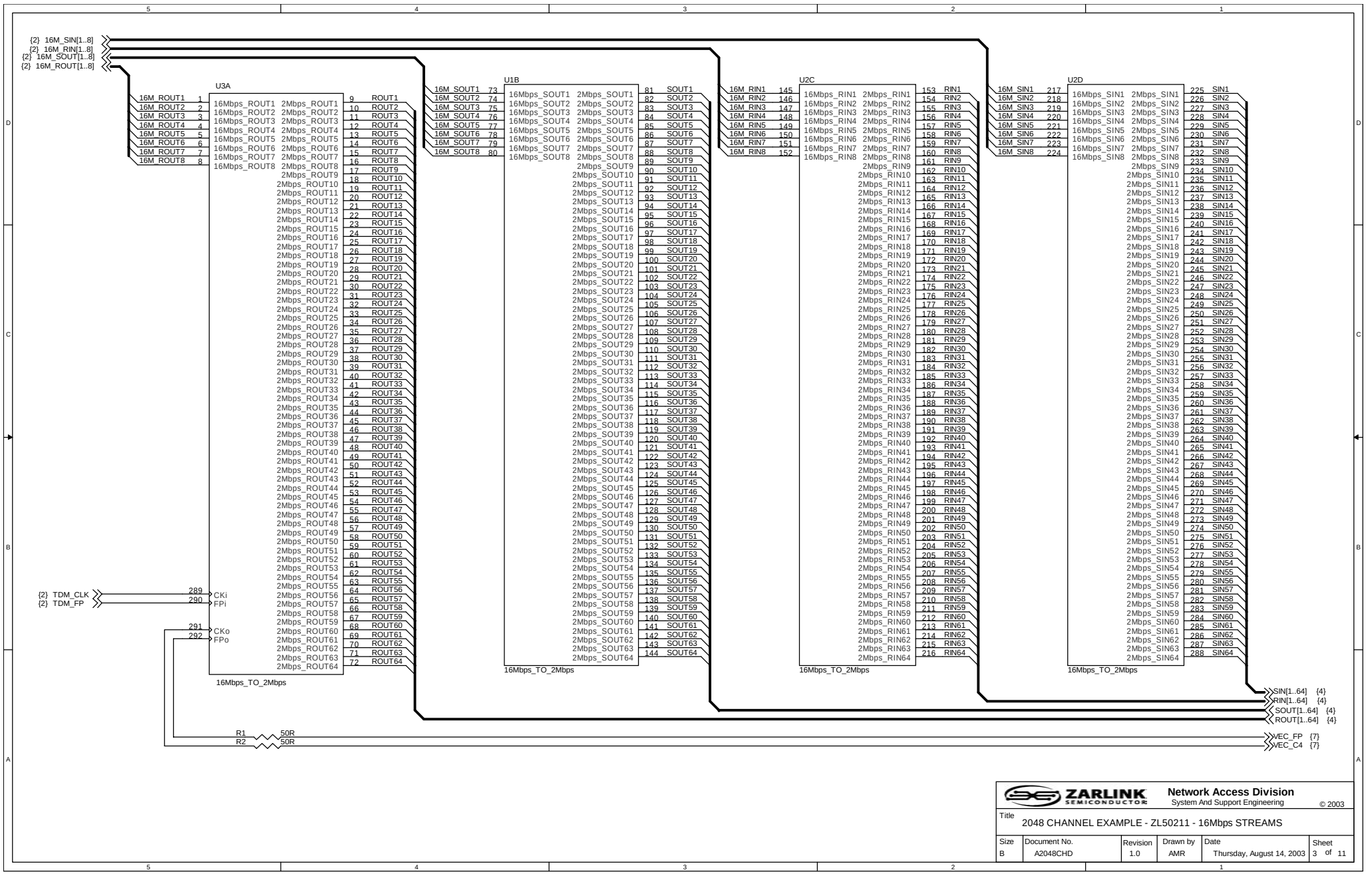

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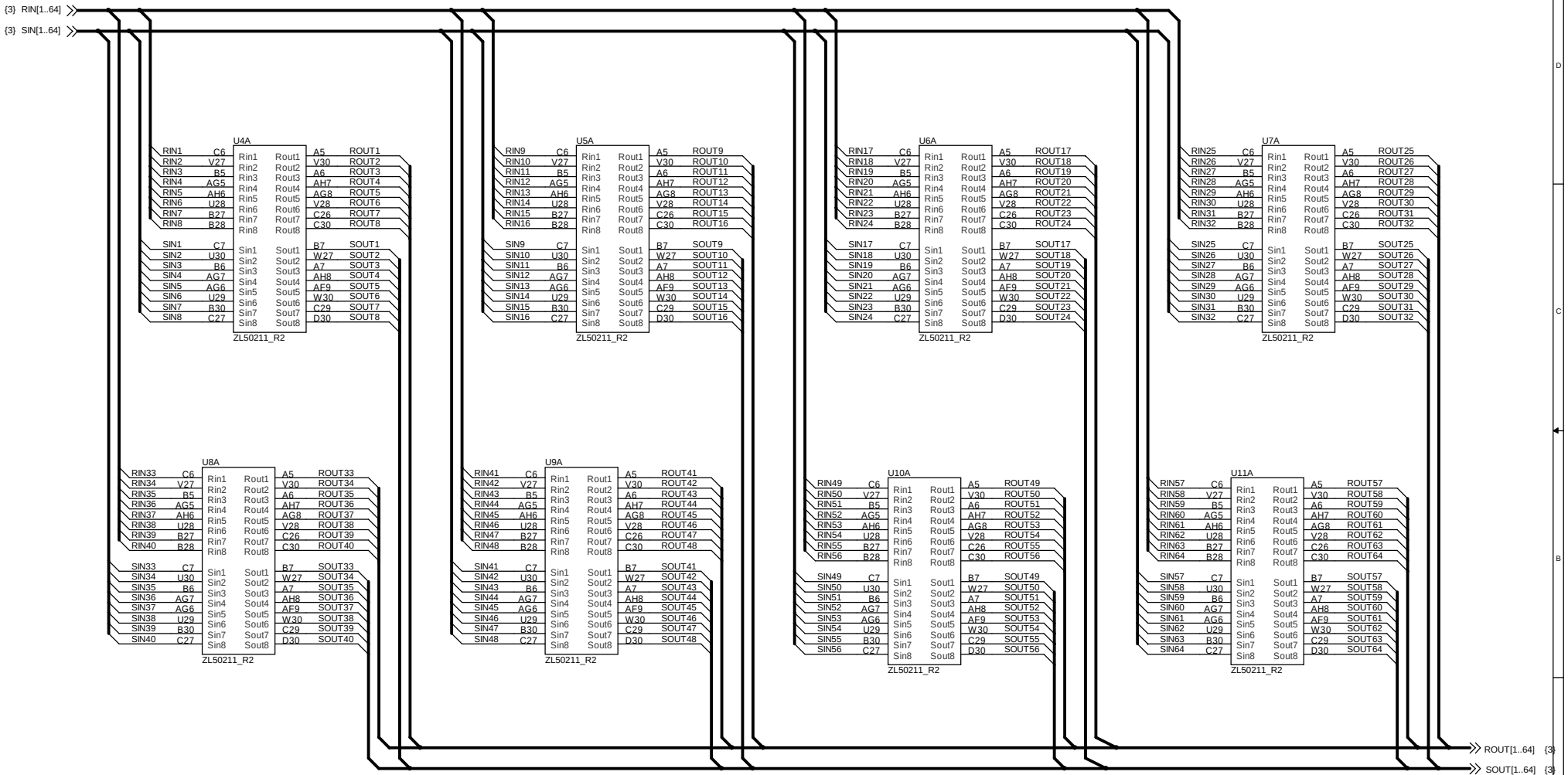

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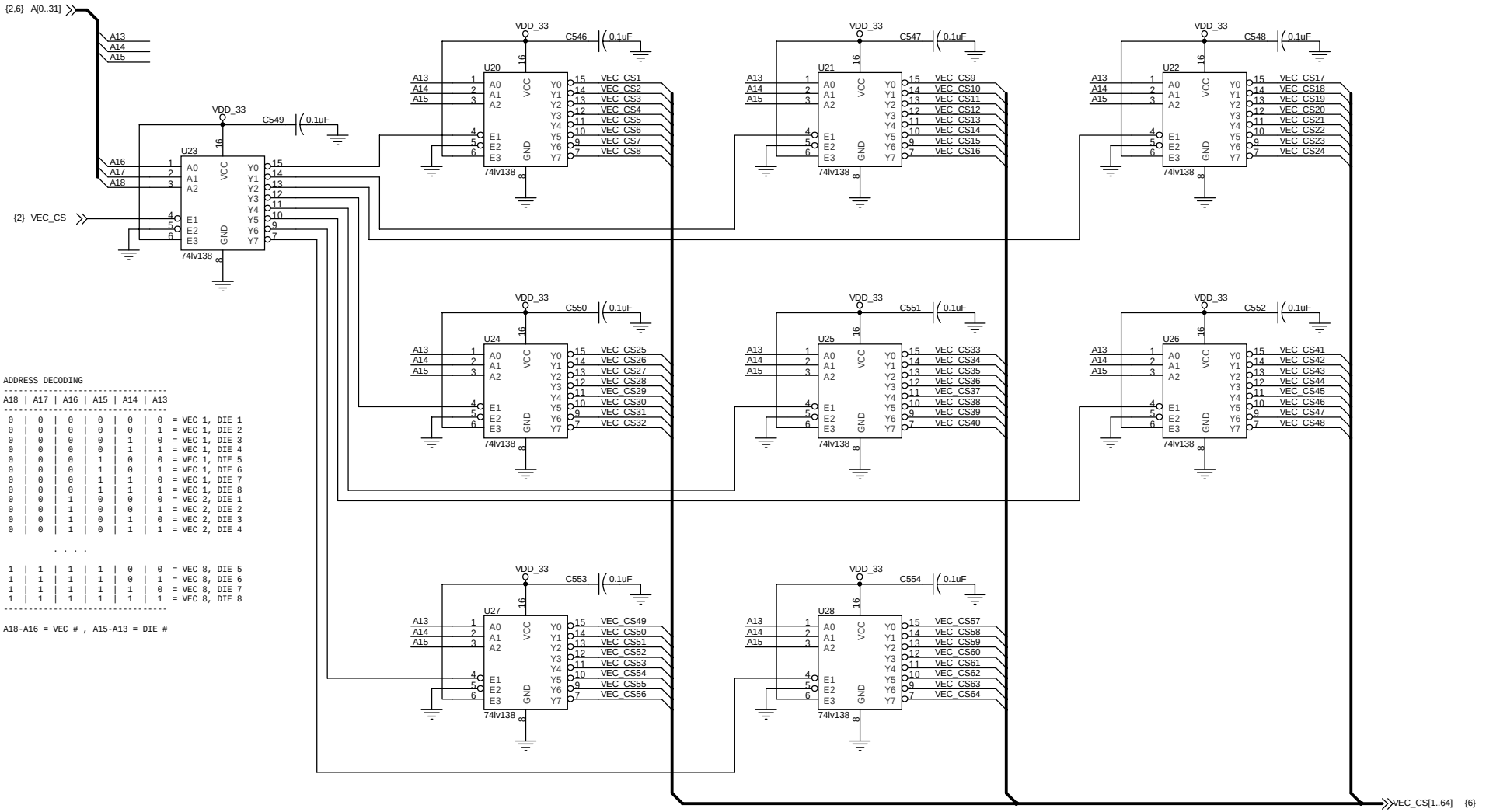

ADDRESS DECODING

A18	A17	A16	A15	A14	A13	
0	0	0	0	0	0	= VEC 1, DIE 1
0	0	0	0	0	1	= VEC 1, DIE 2
0	0	0	0	1	0	= VEC 1, DIE 3
0	0	0	0	1	1	= VEC 1, DIE 4
0	0	0	1	0	0	= VEC 1, DIE 5
0	0	0	1	0	1	= VEC 1, DIE 6
0	0	0	1	1	0	= VEC 1, DIE 7
0	0	0	1	1	1	= VEC 1, DIE 8
0	0	1	0	0	0	= VEC 2, DIE 1
0	0	1	0	0	1	= VEC 2, DIE 2
0	0	1	0	1	0	= VEC 2, DIE 3
0	0	1	0	1	1	= VEC 2, DIE 4
.	.	.	.	.	.	
1	1	1	1	0	0	= VEC 8, DIE 5
1	1	1	1	0	1	= VEC 8, DIE 6
1	1	1	1	1	0	= VEC 8, DIE 7
1	1	1	1	1	1	= VEC 8, DIE 8

A18-A16 = VEC # , A15-A13 = DIE #

NOTE: This address decoding is intended for illustration purposes only. This decoding would normally take place in programmable logic, such as a PAL or CPLD. Timing impact of delays through the 74LV128 3to8 decoders has not been investigated, and should be considered before actually implementing this design.

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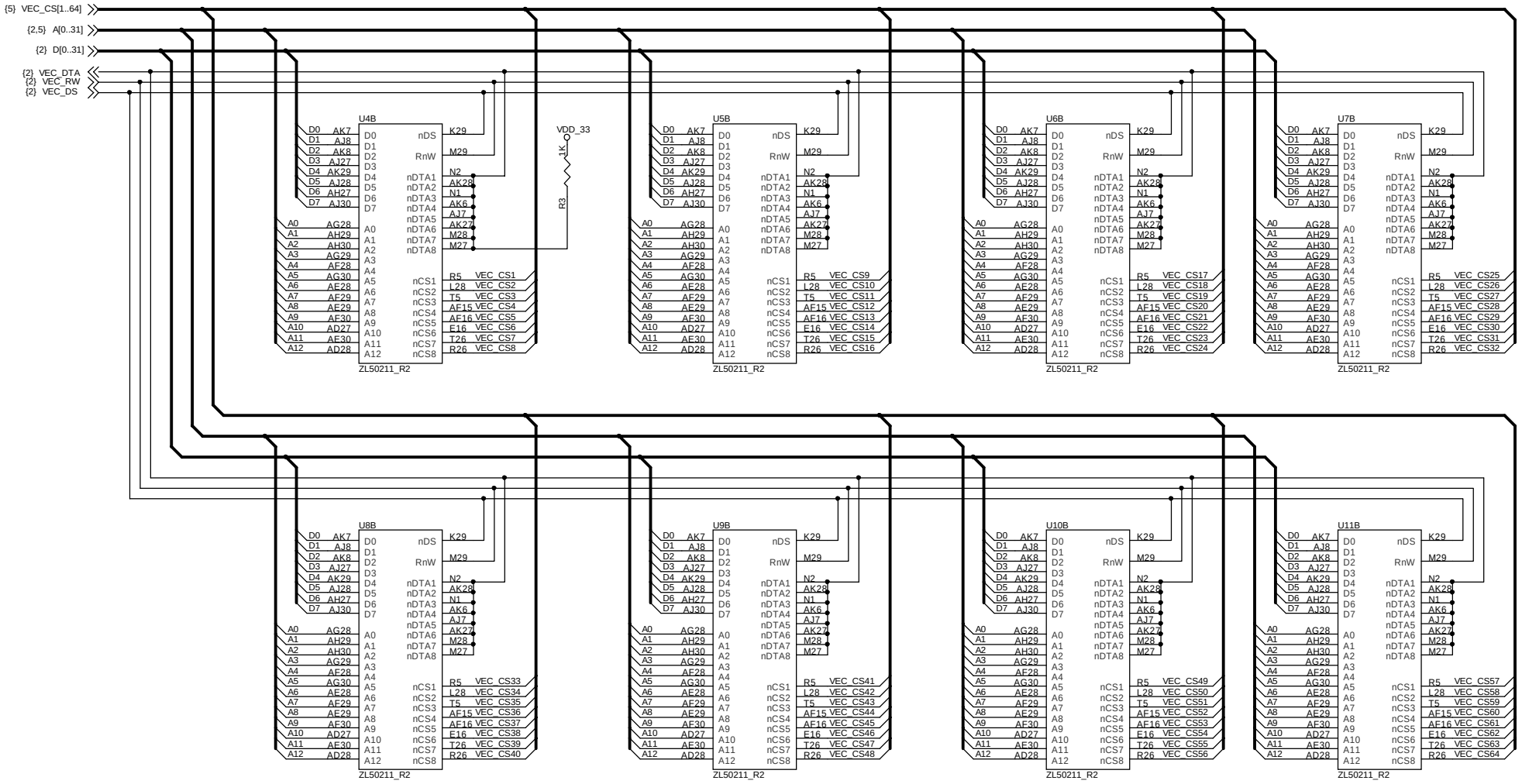

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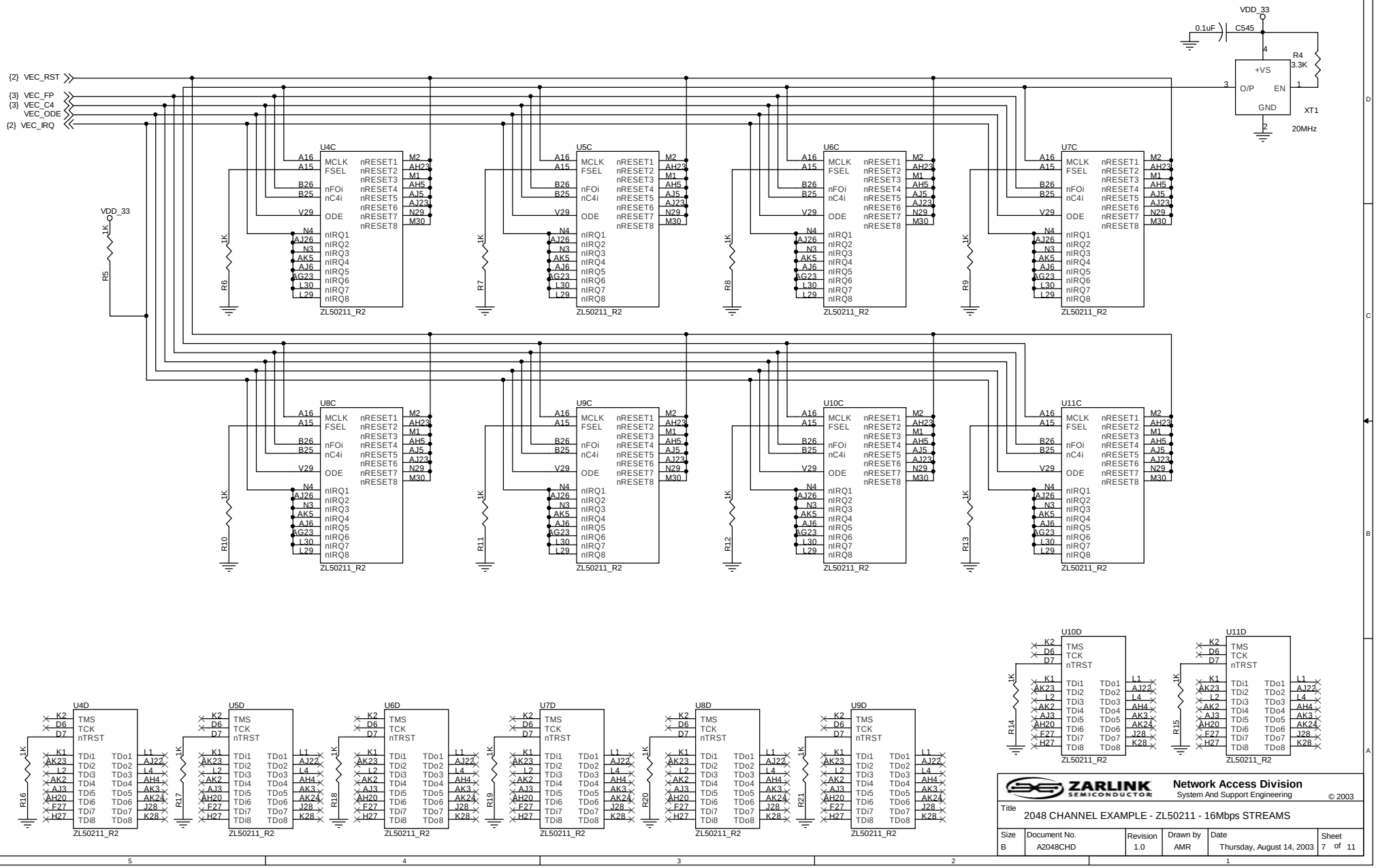

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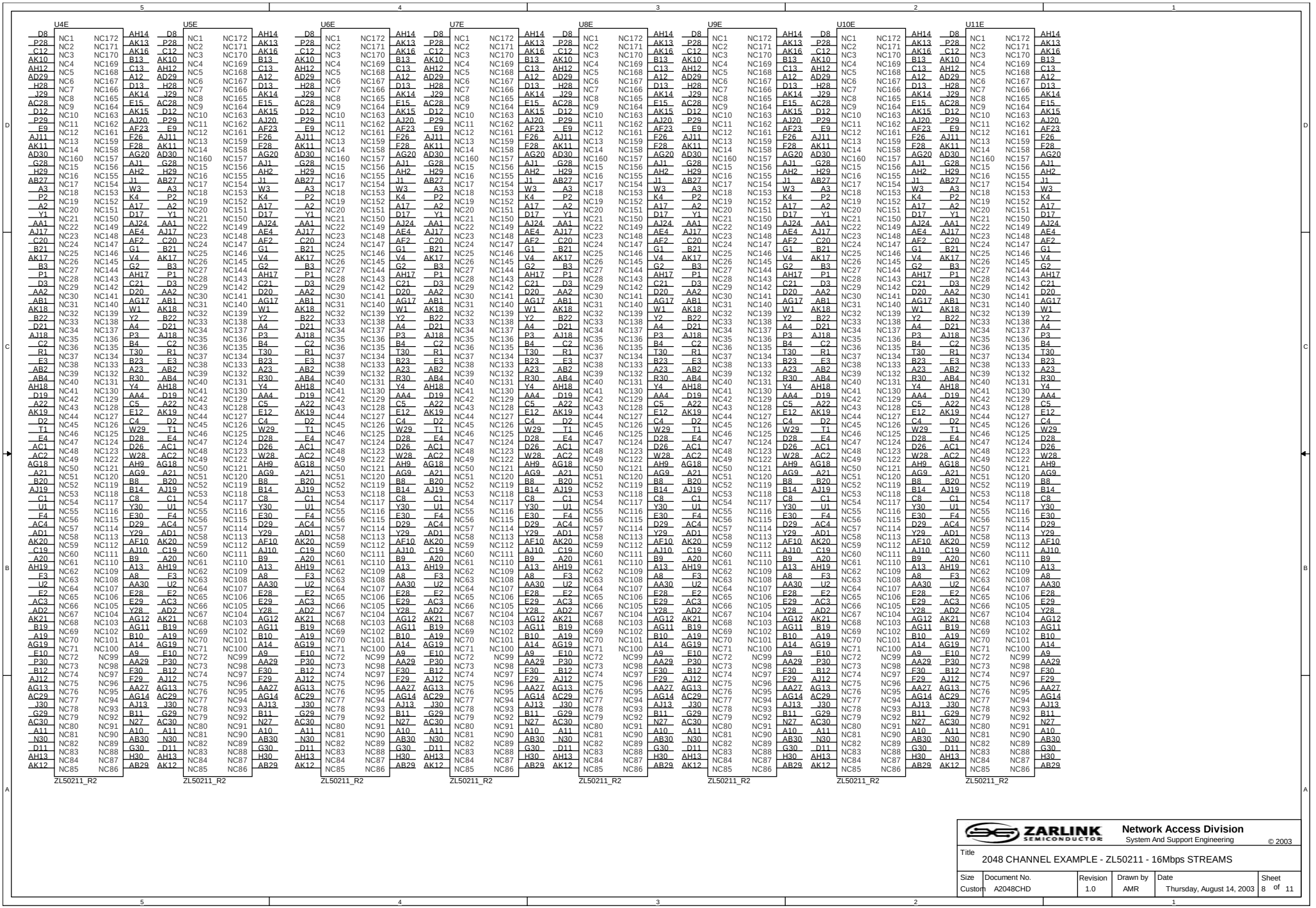
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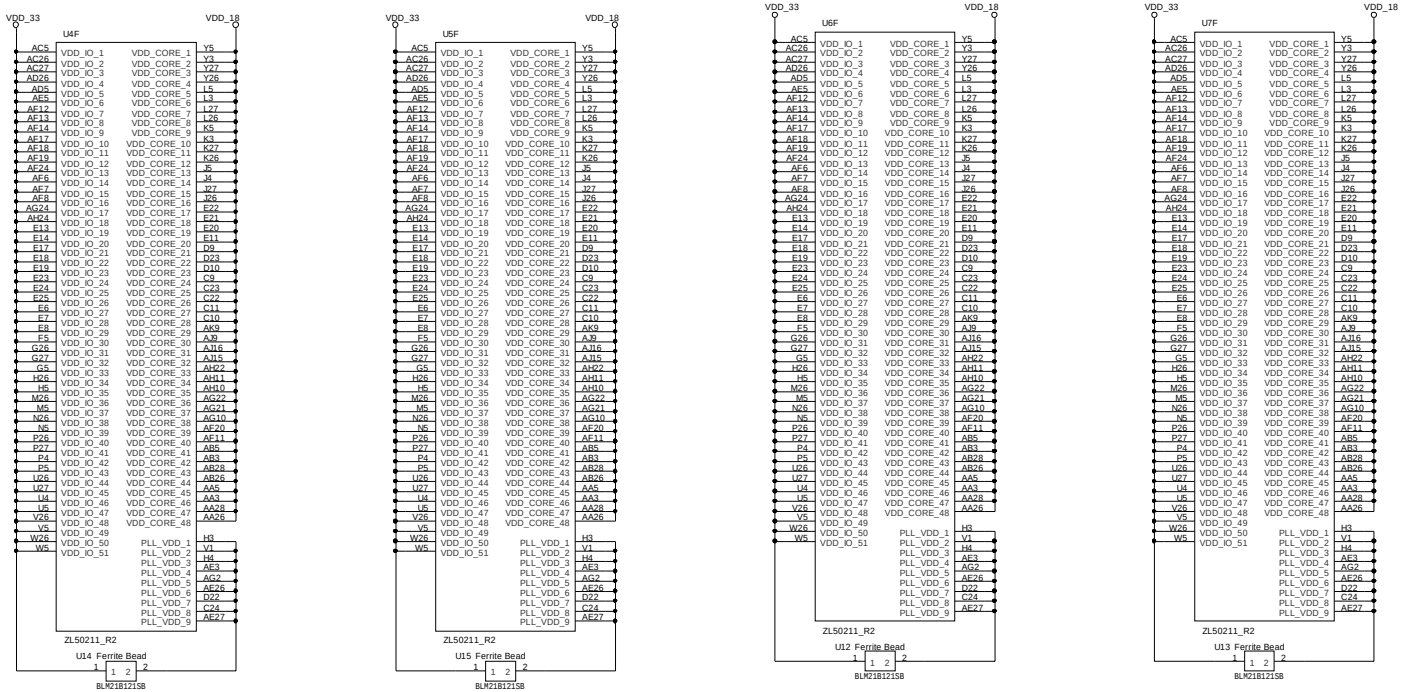

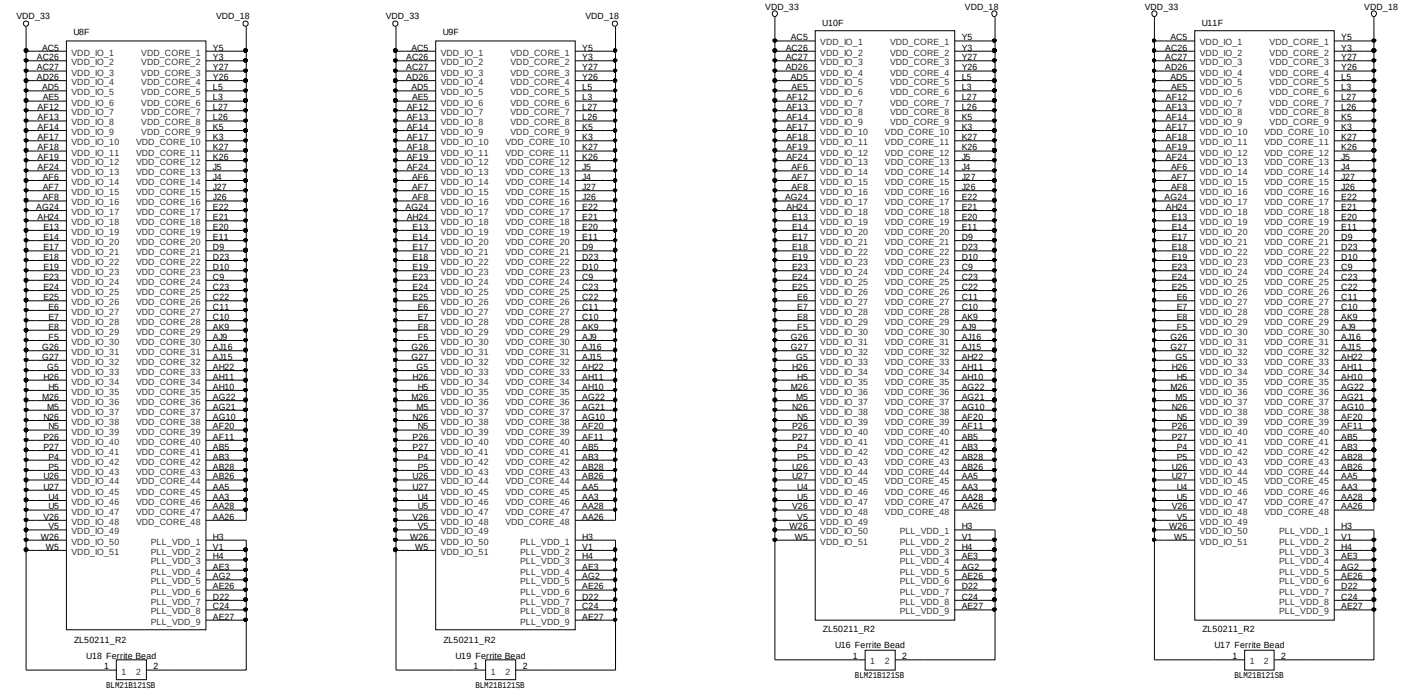

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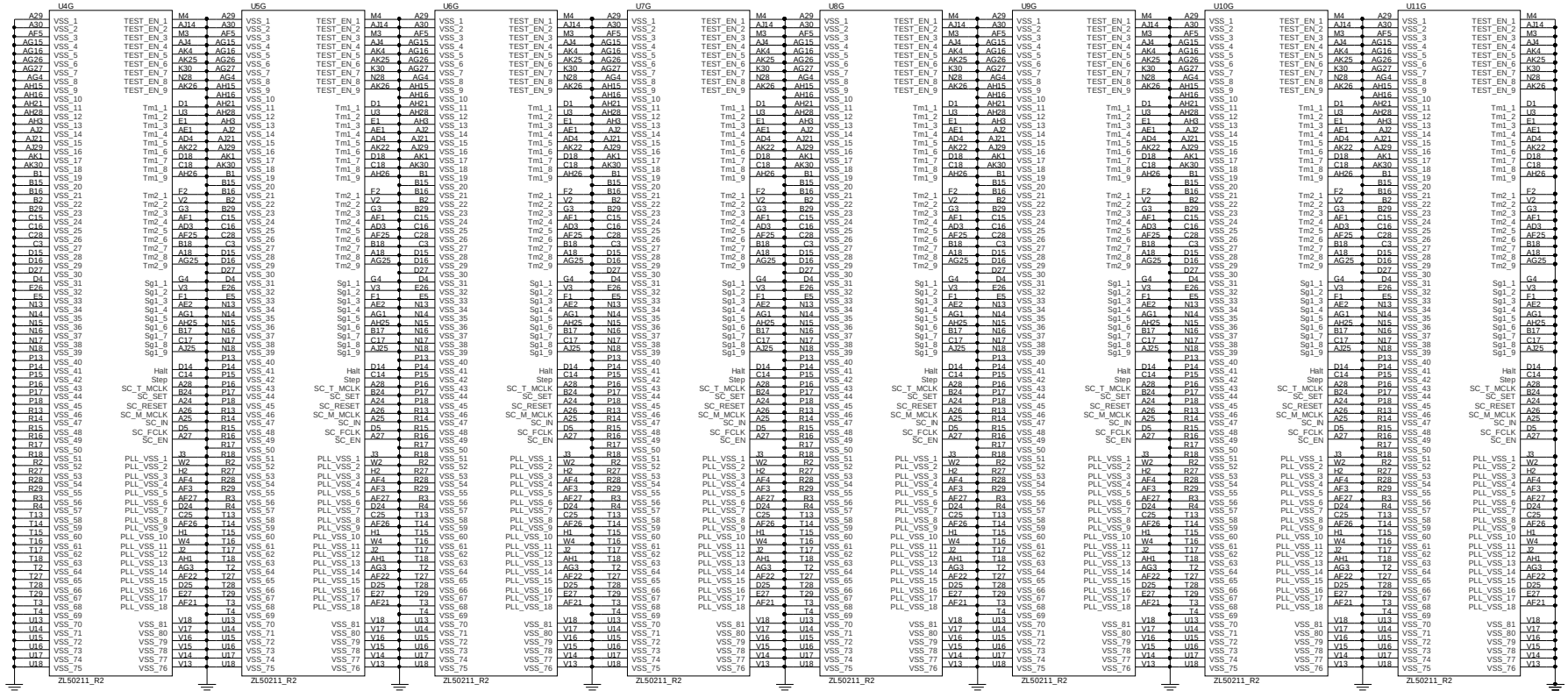

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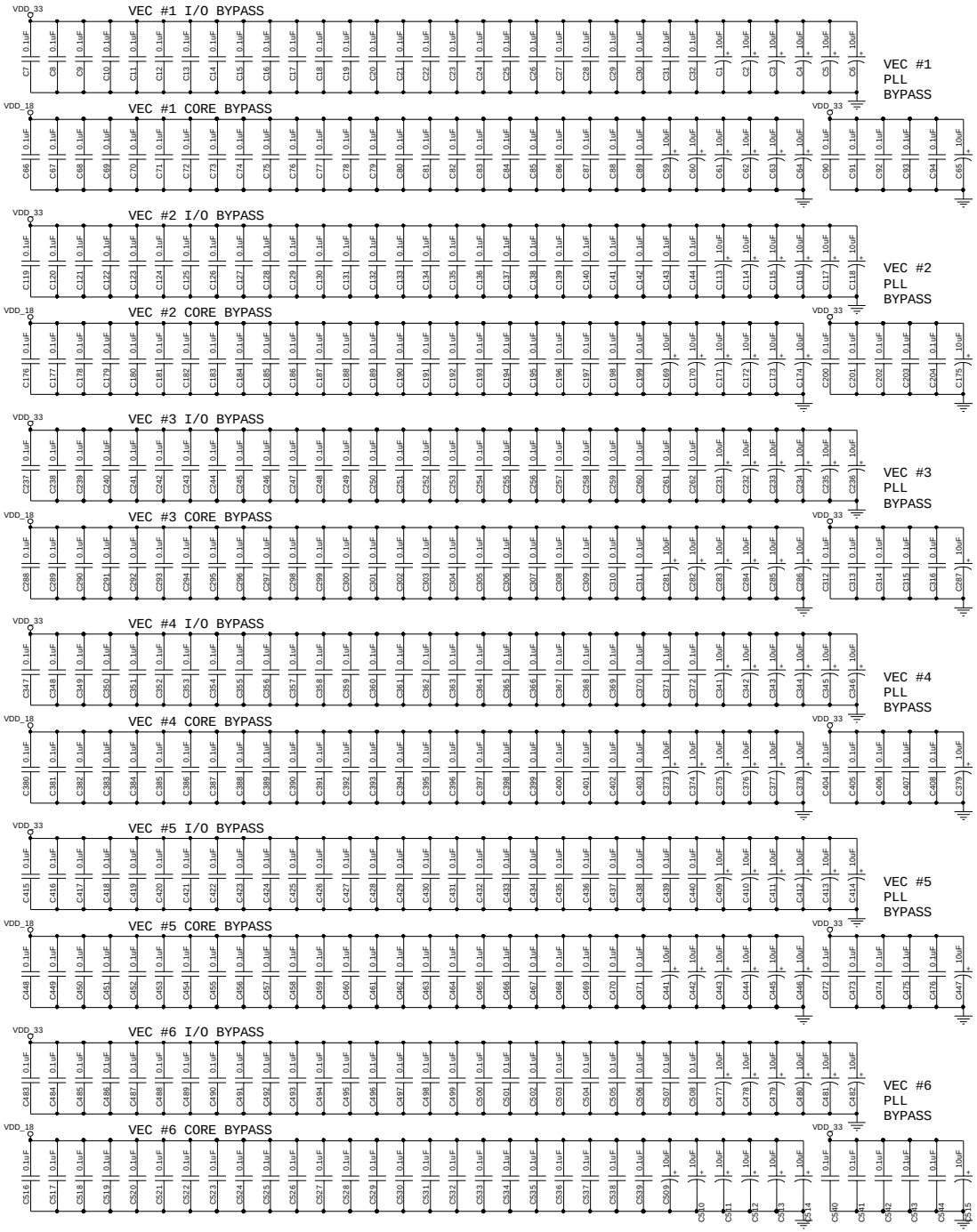

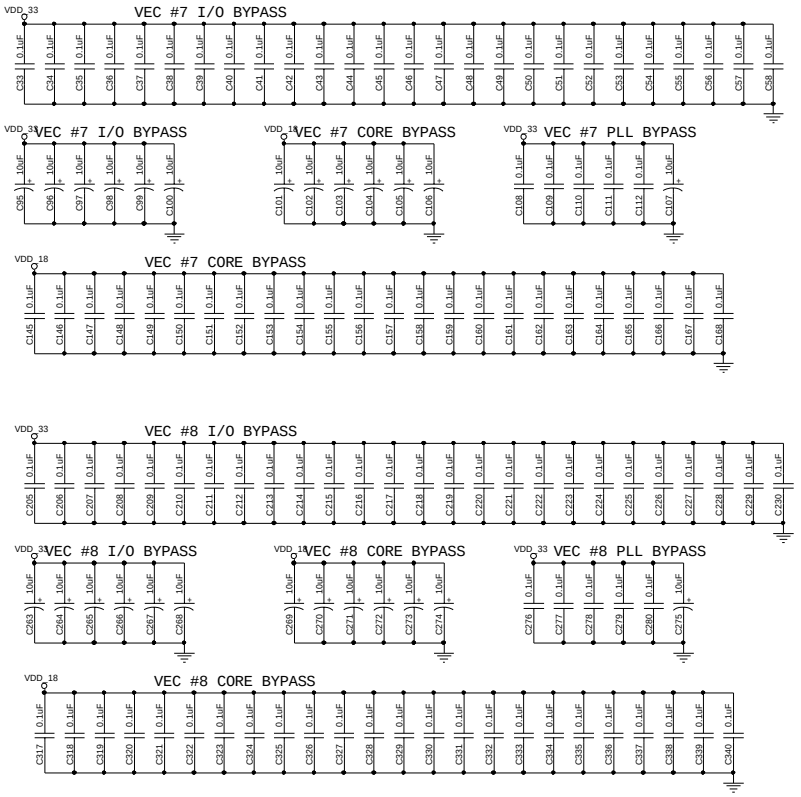

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