ZLAN-55

MT93L16 Improving Convergence Speed

Application Note

August 2003

Contents

1.0 General Overview

The initial register settings of the MT93L16 are intended to provide a conservative stable system in any environment. When a customer is designing the device into their own system, these register values can be tweaked to meet the exact needs of that system.

There are several registers which are hidden from the a user of the Zarlink VEC, as these registers can be very complicated to set up correctly. This text assumes that the reader understands echo delay profiles and knows what the profile of the intended system will look like.

2.0 Register Description

2.1 Acoustic Echo Canceller Adaptation Speed Register (Mu) (0x3D, 0x3C)

Actual mu sent to acoustic LMS. This register is where the user can feed an externally calculated mu value. This register allows the user to program the adaptation speed. The default value is 0x1000 which corresponds to decimal value 2.0. 0x3D is the high byte and 0x3C is the low byte.

2.2 Decay step size control register, Decay Step Number Register, Flat Delay Register (0x26, 0x27, 0x24)

The Exponential Decay registers (Decay Step Number and Decay Step Size) and Flat Delay register allow the LMS adaptation step-size (MU) to be programmed over the length of the FIR filter. A programmable MU profile allows the performance of the echo canceller to be optimized for specific applications. For example, if the characteristic of the echo response is known to have a flat delay of several milliseconds and a roughly exponential decay of the echo impulse response, then the MU profile can be programmed to approximate this expected impulse response, improving the convergence characteristics of the adaptive filter. Note that in the following register descriptions, one tap is equivalent to 125us (64ms/512 taps).

2.3 FD_{6-0} Flat Delay

This register defines the flat delay of the MU profile. The value of FD is 0 to 64ms (0 to 512 taps) for normal mode and 0 to 128ms (0 to 1024 taps) for extended mode. This register occupies the lower 7 bits of address 0x24.

2.4 SSC_{2-0} Decay Step Size Control

This register controls the step size (SS) to be used during the exponential decay of MU. The decay rate is defined as a decrease of MU by a factor of 2 every step of the FIR filter. The minimum step size is 0.5ms (or 4 taps) and can increase in steps of 0.5ms to a maximum of 64ms (512 taps). This register occupies the lower 3 bits of address 0x26.

2.5 NS_{7-0} Decay Step Number

This register defines the number of steps to be used for the decay of MU where each step has a period of SS. This register can be found at address 0x27.

2.6 Start of Exponential Decay (SD)

The point at which the profile, starts to decay is determined by the step size and the number of steps. The following equation can be used to determine SD: SD=64ms - (NS x SS).

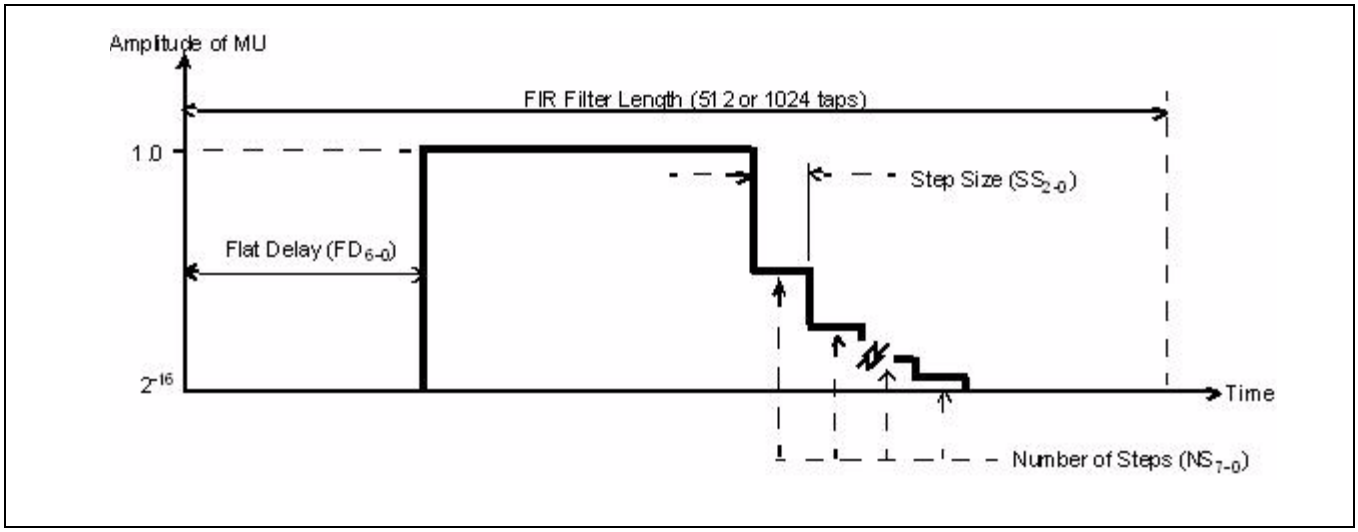

Figure 1 - The MU Profile

3.0 Example Profile

3.1 Calculations for determining register values for an example echo profile

Profile parameters:

MU=0.7
Flat delay = 15ms
Step size = 3ms
number of steps =10

3.2 Calculation of register values

Flat delay register value:

$$FD = \left(\frac{\text{Flat Delay (sec)}}{\text{Frame Period (sec)}}\right) * \left(\frac{1}{8}\right)$$

$$FD = \left(\frac{0.015}{0.000125}\right) * \left(\frac{1}{8}\right)$$

FD = 15 or 0x0F

SSC register value:

$$SSC = \log_2 \left(\frac{\text{Step Size (sec)}}{\text{Frame Period (sec)}} \right) * \left(\frac{1}{4} \right)$$

$$SSC = \log_2 \left(\frac{0.003}{0.000125} \right) * \left(\frac{1}{4} \right)$$

$$SSC = \log_2 (6)$$

$$SSC = 2.58 = 3$$

Start of decay:

$$SD = \text{Maximum Delay} — (NS * SS)$$

$$SD = 0.064 — (10 * 0.03)$$

$$SD = 0.034 \; sec$$

MU register value:

MU register value = MU amplitude * maximum value

MU register value = 0.7 * 16384

MU register value = 11469 or 0x2CCD

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