ZLAN-54

ZL502xx and MT93Lxx VEC Register Tuning Information

Application Note

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1.0 General Overview

This application note provides information on several of the registers in the ZL502xx and MT93Lxx families of echo cancellers. This consists primarily of the Flat Delay Register, Decay Step Number Register, Decay Step Size Control Register, DTDT Register, NLPTHR Register and the Adaptation Step Size Register.

We don't recommend customers to change these settings. Our newer echo cancellers (MT9300, MT93L00, ZL502xx) are G.168 compliant, based in part on the default values of these and other registers. If these registers are changed, we cannot guarantee that our device will still meet G.168. Of course, G.168 is not the final word on ECAN performance. There is always room for improvement over the default values, given knowledge of the system characteristics. Given this warning, this application note gives some brief explanations about these registers.

2.0 Flat Delay Register, Decay Step Number Register, Decay Step Size Control Register

Our echo canceller uses 512-taps (64ms) adaptive filters to store the reference data from Rin. These data are individually attenuated according to an adaptive algorithm and summed to generate a replica of the echo. This replica of the echo is subtracted from the Sin signals to cancel out the echo.

If the general echo characteristics in a system is known, the Flat Delay, Decay Step Number, and Decay Step Size Control registers can be programmed to improve convergence speed and further reduce echo. These three registers basically impose an equalization profile on the data stored in the 512 taps.

For example, if a system is known to have an echo path of at least 10ms, then the Flat Delay registers can be programmed to a value of 10 (dec), so that the newest 10ms (80 taps) of data in the adaptive filter are ignored. On the other hand, if the chance of having an echo path longer than 30ms is very low, then the Decay Step Number and Decay Step Size Control registers can be programmed to, for example, 17 and 2 (dec) respectively, which correspond a decay of the equalization profile after 30ms (240 taps), in 17 steps with 2ms (16 taps) step size, from 1 to 2E-16.

For more details about how to calculate the flat delay, step number, and step size from the register values, please refer to the data sheet.

These registers, if programmed properly, can improve echo cancellation performance. However, the equalization profile also limits an echo canceller's capability. For example, if the flat delay in a device is programmed to 10ms, then the device can no longer handle 5ms echo. It is very important that the system's echo characteristics are fully understood before an equalization profile is imposed.

3.0 DTDT Register

The use of this register is clearly explained in the "Double-Talk Detector" section of the data sheet. The adaptation process is halted when double-talk is detected, but the VEC continues to cancel echo using the old echo profile. This will prevent the echo canceller from diverging to the double-talk signal. Changing this register will affect how the VEC cancels echo under double-talk condition, but it won't affect echo cancellation performance under normal condition.

4.0 NLPTHR Register

Again, the use of this register is clearly explained in the "Non-Linear Processor (NLP)" section of the data sheet. This register defines at what residual echo level the non-linear processor should kick in to further suppress echo. By default the NLP filter is programmed to enable at 21dB. This provides optimal performance under the G.168 standard. Programming this threshold so that the NLP actives sooner will make the echo canceller appear to converge more quickly, but runs the risk of clipping speech.

5.0 Adaptation Step Size Register

This defines a constant - we call it Mu - which is the most important constant in the adaptive echo-cancellation algorithm. Its value determines how fast the echo canceller can converge to echo. When this value is large, the VEC converges faster, but it becomes less stable and oscillate around the optimal point more often, and vice versa. The Mu value has been optimized in our device to provide good performance under all system conditions. We strongly recommend our customers not to modify this value, unless they have a very good idea of what network conditions the echo canceller will be encountering.

6.0 Conclusion

All voice systems have different characteristics and design goals. The default register settings of the ZL502xx and MT93Lxx families designed both to meet the ITU-T G.168 standard as well as provide good performance across a wide range of systems. While these settings work well in the majority of systems, there is always room for improvement when exact network conditions are known. This application note provides background information on the registers that can have a large influence on system performance.

Echo canceller systems often amount to a series of tradeoffs in which different performance goals directly contrast each other. Each register in the echo canceller has direct and indirect effects on other registers. Tuning an echo canceller system most often consists of small register changes and retesting the system between each tweak to see the full result. This can take some time and patience is required.

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