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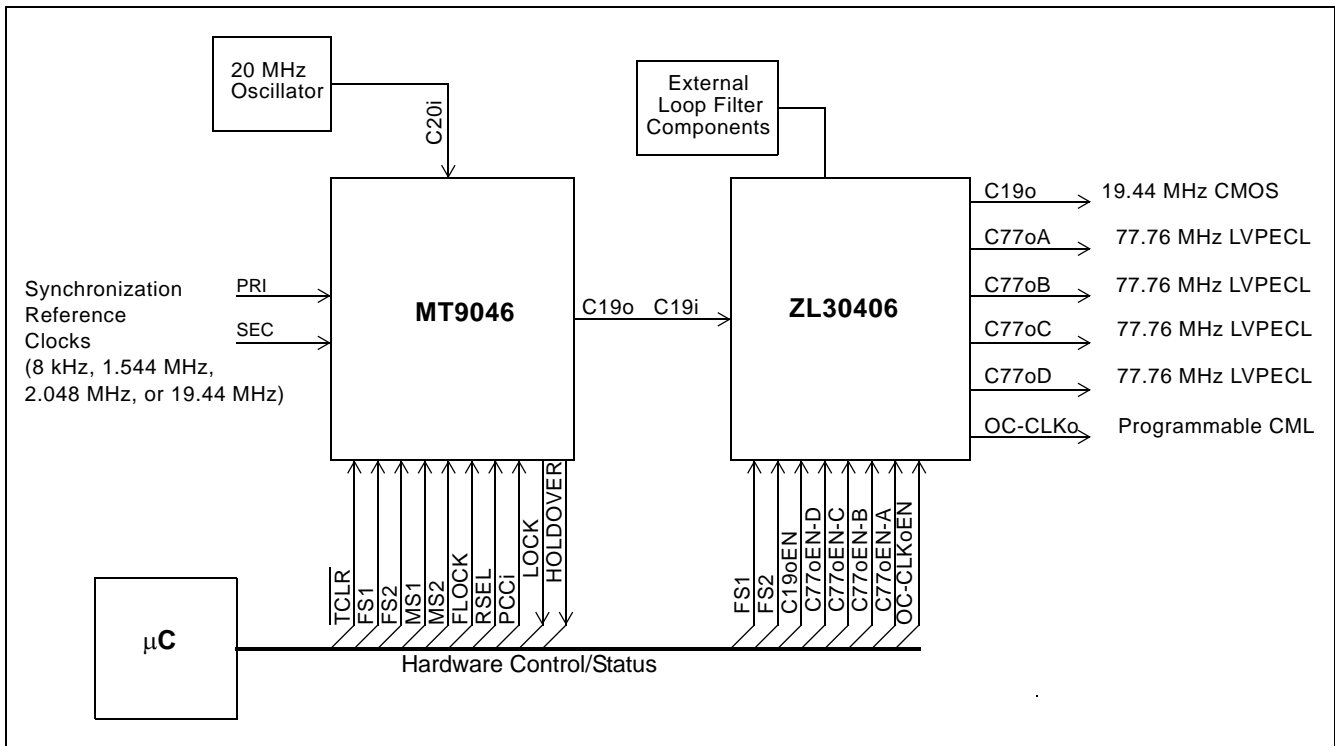
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1.0 Summary

This application will provide details on how to combine Zarlink's Digital PLL products with Zarlink's ZL30406 SONET/SDH Clock Multiplier Analog PLL to provide a robust, ultra-low jitter timing solution for SONET and SDH linecards applications. The DPLL will provide important features such as "hitless" reference switching, short term holdover and rate conversion from low frequency backplane clocks such as 8 kHz. The APLL will provide frequency multiplication with ultra-low jitter output clocks that surpass the jitter requirements of Telecordia GR-253-CORE and ITU-T G.813 specifications for rates up to and including OC-48 and STM-16.

Appendix - Reference Schematic

Figure 1 - SONET/SDH Timing Linecard Block Diagram

2.0 SONET/SDH Linecard Solutions

2.1 SONET/SDH Linecard Requirements

In most SONET/SDH clock architectures, the central timing cards (Master and Slave) are responsible for much of the system level timing requirements specified by the relevant SONET/SDH standards (Telecordia GR-1244-CORE and GR-253-CORE for SONET and ITU-T G.813 for SDH). The Linecards in these systems are generally responsible for:

- Providing “hitless Reference Switching” between the input references of the Master and Slave timing cards
- Providing low-jitter clocks that comply with the appropriate requirements

Table 1 lists the output jitter generation requirements for SONET (GR-253-CORE) and SDH (G.813 Option 2).

OC-N/STM-N Level	OC-N/STM-N Level	Jitter Measurement Filter	Jitter Requirement (UI)	Jitter Requirement (psec)
OC-3/STM-1	155.52 Mbits/sec	12 kHz to 1.3 MHz	0.1 UI _{pp}	643
			0.01 UI _{RMS}	64.3
OC-12/STM-4	622.08 Mbits/sec	12 kHz to 5 MHz	0.1 UI _{pp}	161
			0.01 UI _{RMS}	16.1
OC-48/STM-16	2488.32 Mbits/sec	12 kHz to 20 MHz	0.1 UI _{pp}	40
			0.01 UI _{RMS}	4

Table 1 - SONET/SDH Jitter Requirements

Table 2 lists the output jitter generation requirements for SDH (G.813 Option 1).

	Interface	Jitter Measurement Filter	Jitter Requirement (UI)	Jitter Requirement (psec)
STM-1	155.52 Mbits/sec	1 MHz to 20 MHz	0.1 UI _{pp}	643
		5 kHz to 20 MHz	0.5 UI _{pp}	3215
STM-4	622.08 Mbits/sec	250 kHz to 5 MHz	0.1 UI _{pp}	161
		1 kHz to 5 MHz	0.5 UI _{pp}	804
STM-16	2488.32 Mbits/sec	65 kHz to 1.3 MHz	0.1 UI _{pp}	40
		500 Hz to 1.3 MHz	0.5 UI _{pp}	200

Table 2 - SDH Jitter Requirements

2.2 MT9046 + ZL30406 Solution

2.2.1 Introduction

Using the MT9046 DPLL (digital phase-locked) with the ZL30406 APLL (analog phase locked-loop) as shown in Figure 1, Zarlink can provide a cost-effective, ultra-low jitter linecard solution for SONET/SDH applications for up to and including OC-48/STM-16 rates.

MT9046 Features:

- “Hitless” reference switching
- Rate conversion from low frequency backplane clocks (i.e., 8 kHz)
- 1.9 Hz loop filter
- Lock indication
- Short term holdover and holdover indication
- Input reference frequency monitoring (MT9045 must be used instead of MT9046)

ZL30406 features:

- Externally programmable loop filter
- 4 low-jitter 77.76 MHz LVPECL output clocks
- 1 low-jitter 19.44 MHz CMOS output clock
- 1 low-jitter selectable CML output clock (19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz)

2.2.2 Design Considerations

2.2.2.1 Device Control and Setup

Both the MT9046 and ZL30406 are easily controlled and monitored through a set of hardware pins. Please refer to the specific data sheets for detailed information on their operation.

2.2.2.2 ZL30406 Loop Filter

The characteristics of the ZL30406 Loop filter can be defined by equation 1 and 2, shown below:

Equation 1

$$\text{BANDWIDTH} = \frac{R1 \cdot K}{2\pi}$$

Equation 2

$$\text{DampingFactor} = \zeta = \frac{R1}{2} \cdot \sqrt{K \cdot C1}$$

where,

$$K = \frac{K_{VCO} \cdot I_{CP}}{N} = 11.0625$$

K_{VCO} = VCO gain

I_{CP} = Charge Pump Current

N = Divider Ratio

R1, C1 and C2 = External Loop filter components

From equations 1 and 2, we can develop equations for selecting our Loop filter components for our desired loop bandwidth and damping factor. Note, the damping factor must be greater than 0.707 to ensure that the PLL remains stable.

Equation 3

$$R1 = \frac{2\pi \cdot BW}{K}$$

Equation 4

$$C1 = \frac{\left(\frac{2 \cdot \zeta}{R1}\right)^2}{K}$$

Capacitor C2, is optional, and will not have a large impact on PLL performance, but in general the figure of merit for PLL stability is for C2 to be less than 1/10th the value of C1, employing higher multiples will further improve device stability.

From the results of our bench evaluation, when using the MT9046 as the input reference to the ZL30406 the recommended loop filter is shown below.

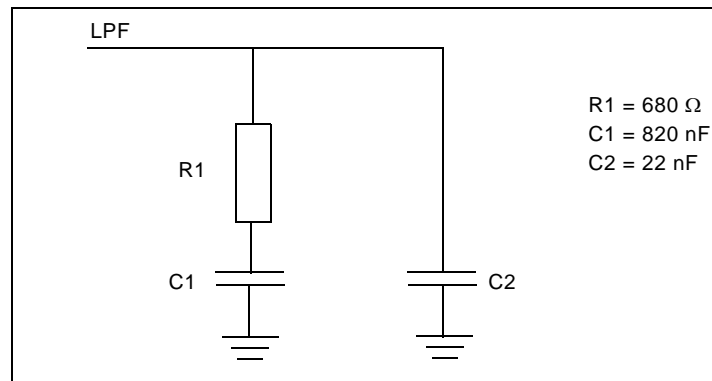


Figure 2 - Recommended Loop Filter

2.2.2.3 MT9046 Master Oscillator Selection

In linecard applications where the SONET/SDH system level timing requirements are met on the master/slave timing cards and there is no requirement for holdover, there is no requirement for a high accuracy, temperature compensated crystal oscillator such as a TCXO or OCXO. A low-cost +/-32 ppm (or better) crystal oscillator can be used.

When the MT9046 is operating in normal mode and the active reference is lost, the device is placed in auto-holdover mode and the holdover pin goes high, the user would recognize this state and immediately switch to the secondary reference. This temporary switch to holdover is of very short duration and does not require an expensive oscillator, if the application calls for long term holdover on the linecard then a more stable, temperature compensated crystal oscillator would be necessary.

If your application calls for more extensive input frequency monitoring, Zarlink's MT9045 DPLL can be substituted for the MT9046. The MT9045 has Out of range indicators that detect when the input reference is more than +/- 17 ppm from its nominal rate. In order to properly use this feature, a more accurate crystal oscillator would be required (+/-4.6 ppm).

2.2.2.4 Power Supply Decoupling Recommendations

Here is a list of power supply recommendations to help ensure optimal jitter performance of the ZL30406 (for more detail please refer to the reference schematic in the appendix of this document):

- Ferrite bead power supply filters should be used to filter high frequency noise from possible onboard digital switching circuit sources.
- Separate nets are recommended to provide some isolation between different power pin groups on the ZL30406 (see VCC_406A and VCC_406B in the reference schematic)
 - For each power net, a small local copper area or "island" should be laid out on an internal layer beneath the applicable ZL30406 power pins.
 - A low pass filter should be placed at the entry to the VCC1 power net.
- A decoupling capacitor should be placed within 200 mils of each power pin, on the same side, at the periphery of the TQFP-64 package. The recommended cap value is 0.1 uF, size 0603 or 0402.
- Each decoupling capacitor should have separate power and ground vias. Large diameter or double vias are preferred to control inductance.
- For ZL30406 ground pins, use double vias or large diameter vias to connect to the internal ground plane and in general, try to minimize trace and via inductance.
- The ZL30406 BIAS pin is powered from VCC1 through a network of two 33 uF caps and a 220 ohm resistor. In layout, these should be grouped close to the BIAS pin and routed with wide traces.

2.2.2.5 Clock Termination

Figures 3 through 6 shows some standard termination methods for LVPECL and CML output clocks.

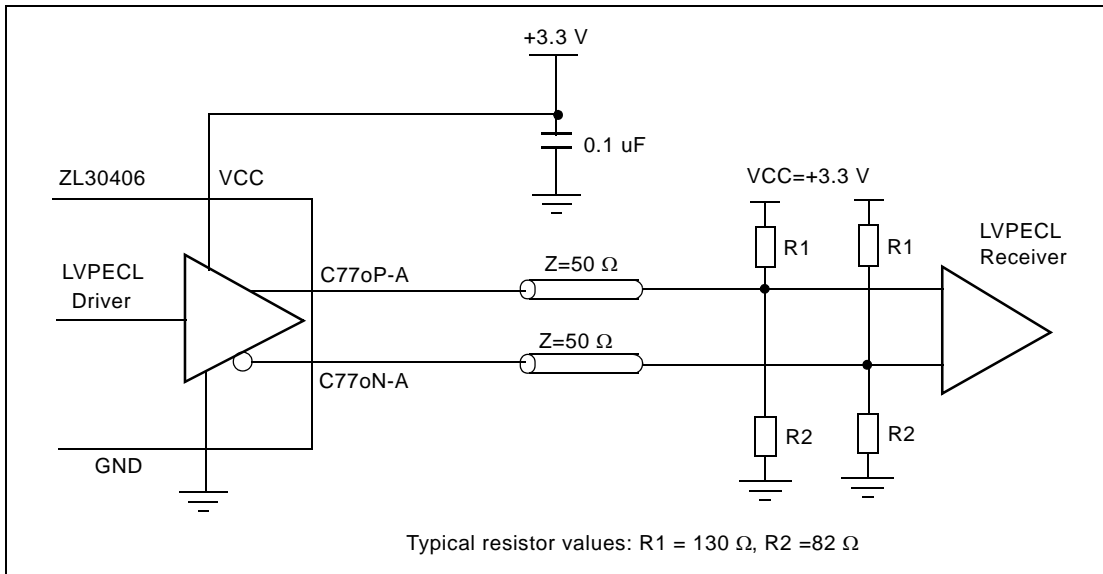


Figure 3 - LVPECL to LVPECL Interface

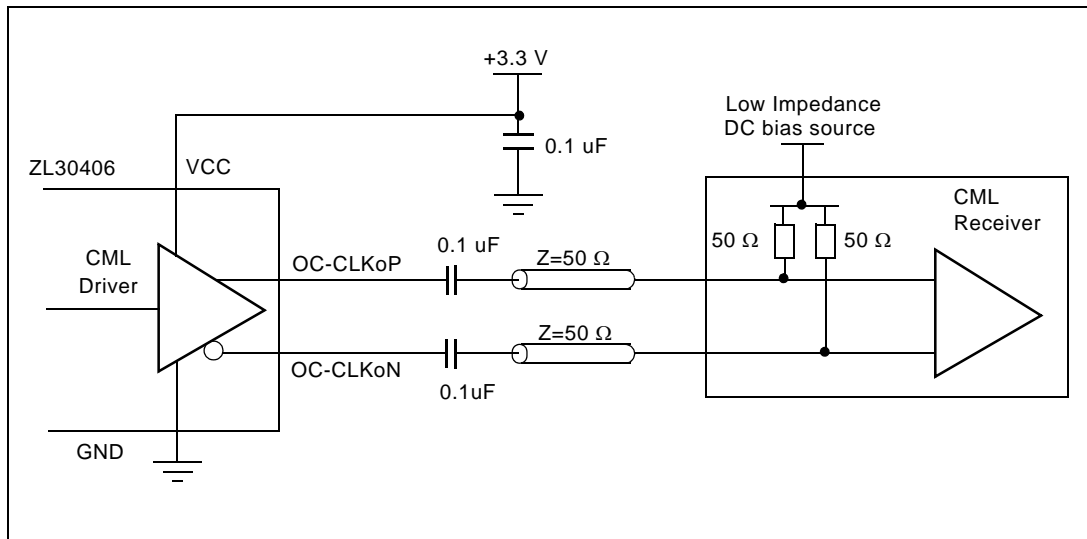


Figure 4 - CML to CML Interface

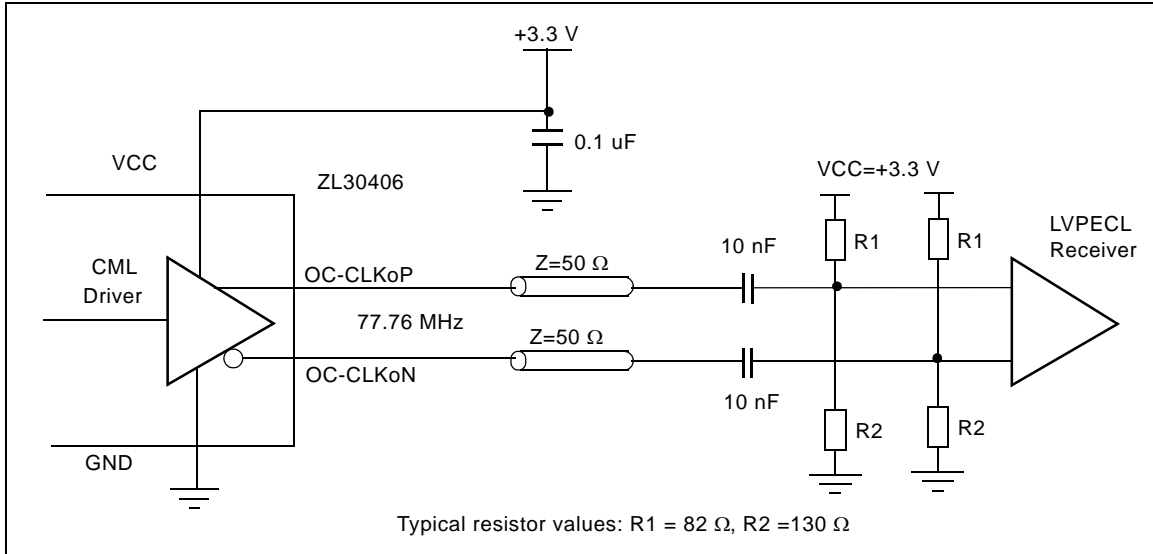


Figure 5 - CML to LVPECL Interface

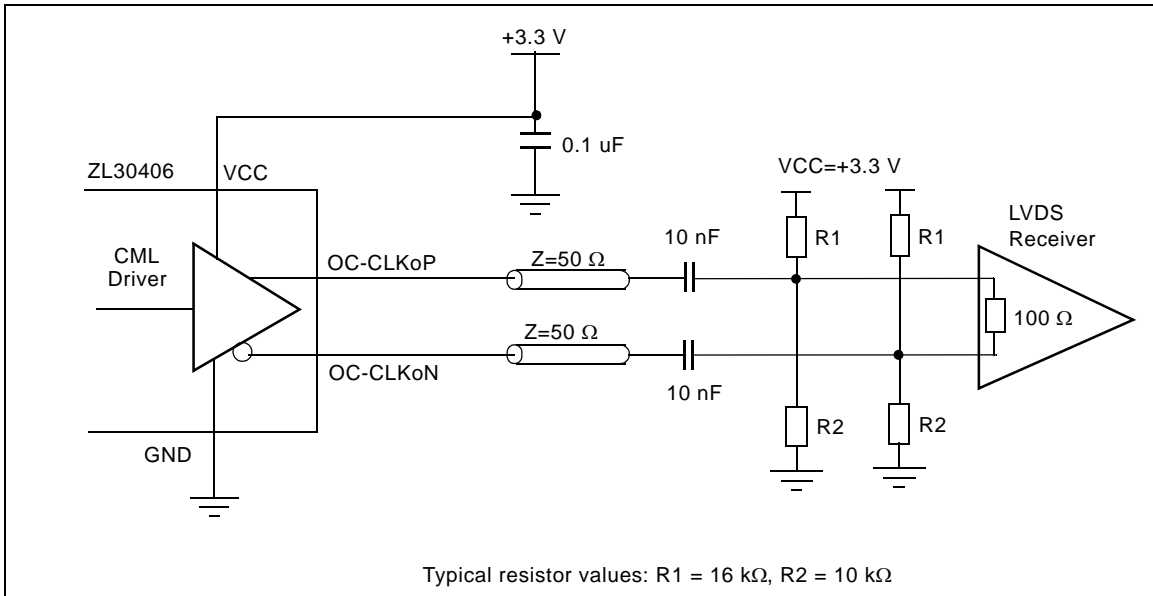


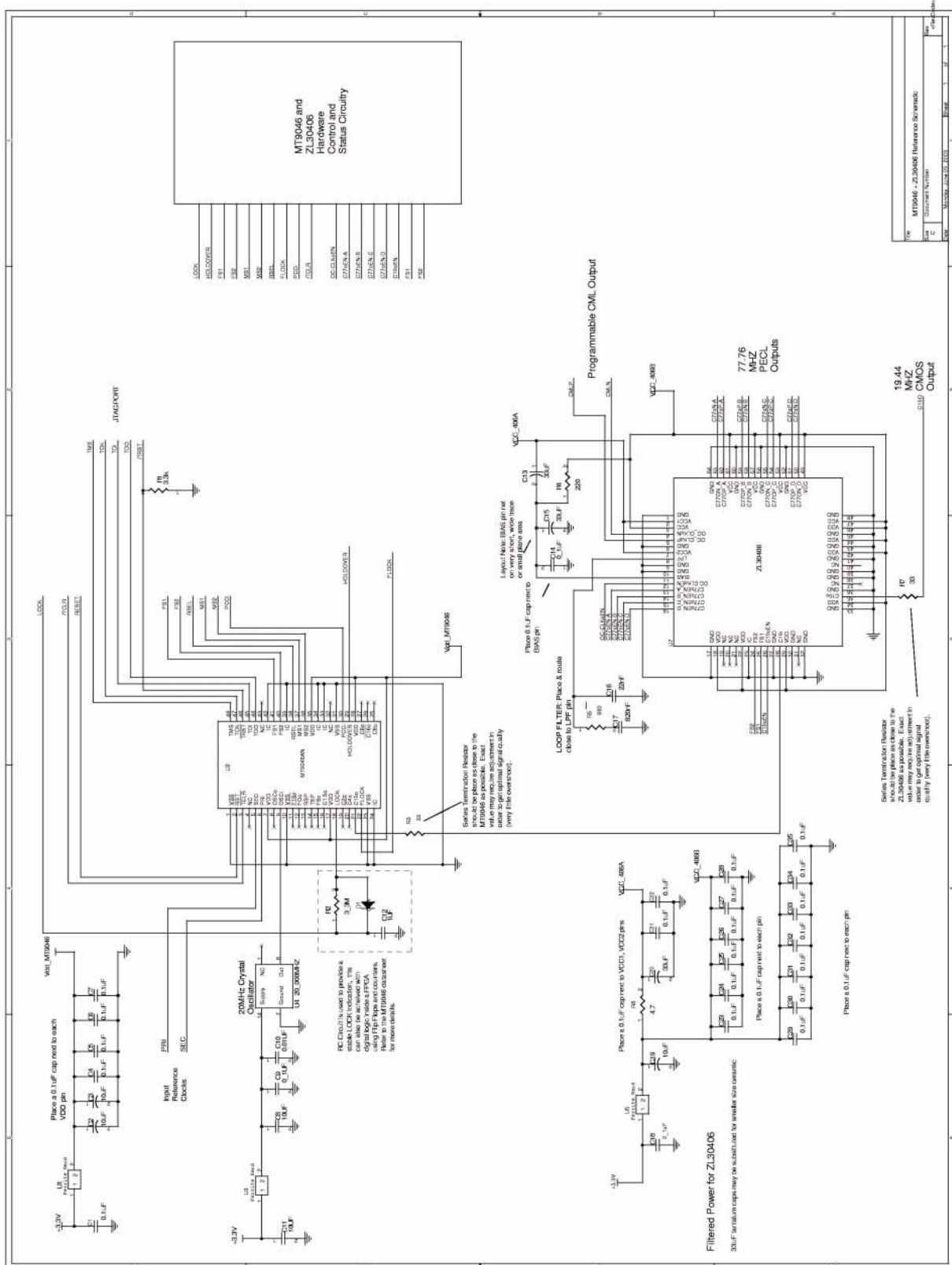
Figure 6 - CML to LVDS Interface

2.2.3 Jitter Performance

Table 3 shows typical jitter performance of the MT9046 and ZL30406 versus the output jitter generation requirements of SONET (GR-253-CORE) and SDH (G.813 Option 2).

Jitter Filter	Requirement	155.52 MHz CML Output	77.76 MHz LVPECL Output	19.44 MHz CMOS Output
OC-3/STM-1 (12 kHz-1.3 MHz)	643 ps (pk-pk)	12.95 ps (pk-pk)	17.27 ps (pk-pk)	41.78 ps (pk-pk)
	64.3 ps (rms)	1.02 ps (rms)	1.37 ps (rms)	3.29 ps (rms)
OC-12/STM-4 (12 kHz-5 MHz)	161 ps (pk-pk)	16.0 ps (pk-pk)	21.21 ps (pk-pk)	54.22 ps (pk-pk)
	16.1 ps (rms)	1.26 ps (rms)	1.67 ps (rms)	4.27 ps (rms)
OC-48/STM-16 (12 kHz - 20 MHz)	40 ps (pk-pk)	19.18 ps (pk-pk)	25.15 ps (pk-pk)	N/A
	4 ps (rms)	1.51 ps (rms)	1.98 ps (rms)	N/A

Table 3 - Typical Jitter Performance of the MT9046 + ZL30406





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