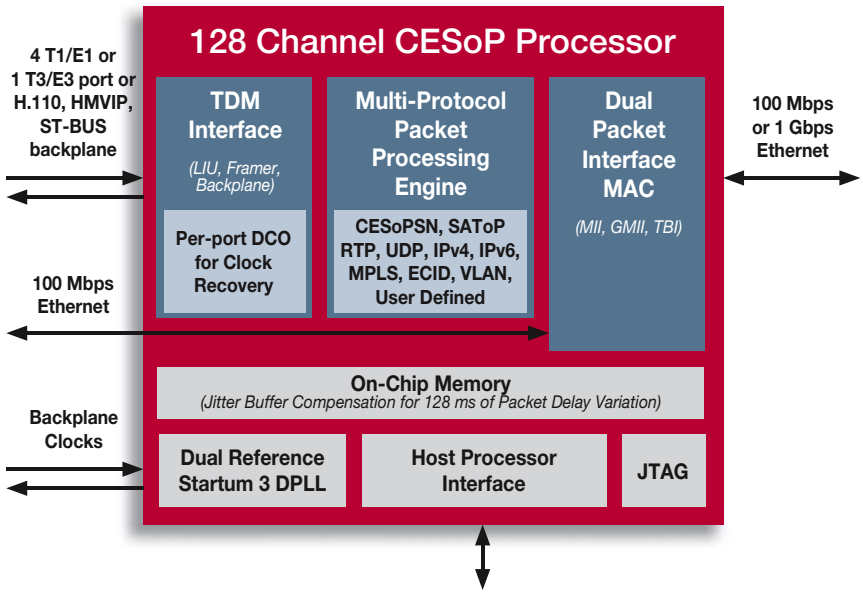
CESoP PROCESSORS ZL50118/19/20

PRODUCT PREVIEW

The ZL50120 family of low-density Circuit Emulation Services-over-Packet processors offers a powerful and flexible approach to carrying TDM voice and data traffic, with associated timing and signaling, across Ethernet, IP, and MPLS networks.

Each device provides a flexible TDM interface with embedded timing that fully meets T1/E1 timing and synchronization standards, allowing a seamless interface with T1/E1 equipment. With an integrated digital PLL, internal jitter buffer memory and dual packet interface, the ZL50120 family reduces bill of material costs and board space, and simplifies access equipment design. Complimenting the ZL50111 family of high-density CES-over-Packet chips, Zarlink offers a complete portfolio of bridging devices capable of sending from one to 32 T1/E1 streams of TDM traffic over any PSN (packet-switched network).

ZL50120 Simplified Block Diagram



ZL50118	1 T1 or 1 E1 stream or 1 MVIP/ST-BUS stream at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps
ZL50119	2 T1 or 2 E1 streams or 2 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps
ZL50120	4 T1 or 4 E1 streams or 1 J2, 1 T3, 1 E3 or 1 STS-1 stream or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps

Applications

- TDM traffic over packet networks
- PON, FTTx, Broadband access
- TDM over Wi-Fi and WiMAX
- 3G Wireless Backhaul
- IP DSLAM, NG-DLC
- MDU/MTU

CESoP Processors Expand Reach

- Flexible TDM access interface supports T1/E1, T3/E3, H.110, HMVIP and ST-BUS streams
- Nx64 kbps trunking enables traffic grooming, fractional T1/E1 services
- Fast Ethernet port allows Ethernet and TDM traffic aggregation, simplifying system-level design
- Programmable multi-protocol packet encapsulation supports RTP, UDP, Ethernet VLANs, IPv4, IPv6 and evolving MPLS, PWE3 and MEF Circuit Emulation standards

Carrier-Grade Voice Quality

- Patented hardware/software techniques for clock recovery and synchronization
- Advanced QoS mechanism allows traffic prioritization
- Extremely low and stable latency, intrinsic delays < 500 microseconds

Embedded Timing

- Embedded timing recovers clocks across packet networks
- Per-port T1/E1 clock recovery in unstructured CES mode
- Adaptive clock recovery meets G.823 for E1, G.824 for T1 timing
- Dual-reference Stratum 3 DPLL supports TDM H.110 and HMVIP master/slave timing operation

Standard Compliant

- ITU-T recommendation Y.1413
- IETF PWE3 draft standards CESoPSN and SAToP
- MEF implementation agreement for PDH circuits
- MPLS forum draft CESoMPLS implementation agreement

Evaluation boards and API are available

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APPLICATION

EPON (Ethernet Passive Optical Network)

Facing growing data traffic volumes and increased competition, carriers are extending their packet networks to cost-effectively deliver multiple services to end users.

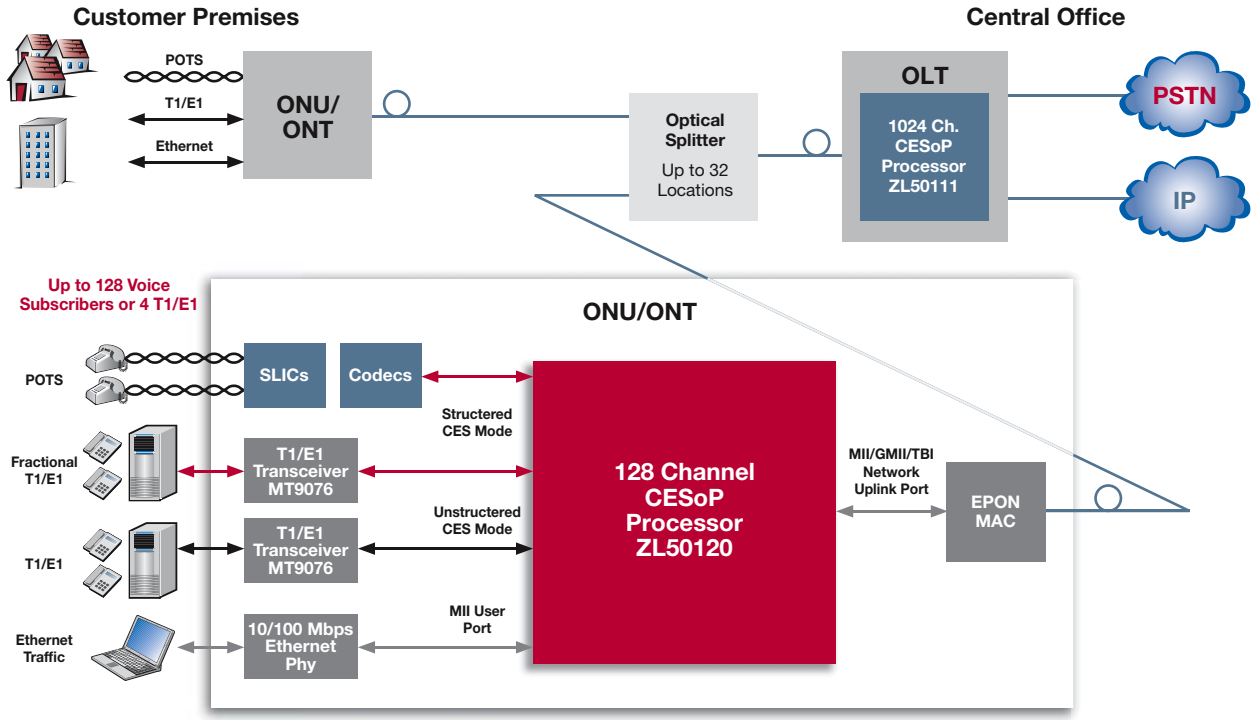
The diagram below shows how the ZL50120 low-density CES-over-Packet processor may be used in the ONU/ONT (Optical Networking Unit/Terminal) of an EPON (Ethernet Passive Optical Network) to provide POTS, T1/E1, fractional T1/E1 and Ethernet services.

The flexible TDM interface allows the device to be used directly with CODECs and framers in structured CES mode. In unstructured CES mode, the device interfaces directly to LIUs providing independent timing recovery for each TDM port.

The per-port DCO (Digitally Controlled Oscillator) ensures precise synchronization of TDM and T1/E1 traffic across an EPON. Patented hardware/software techniques support adaptive and differential timing and synchronization.

The dual Ethernet interface enables local Ethernet and TDM traffic to be aggregated onto the Fast/Gigabit Ethernet network uplink.

Together with the high-density ZL50111 CESoP processor located in the Central Office's OLT (Optical Line Terminal), Zarlink offers the industry's only end-to-end portfolio of circuit-to-packet devices for carrying TDM traffic over packet networks.



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