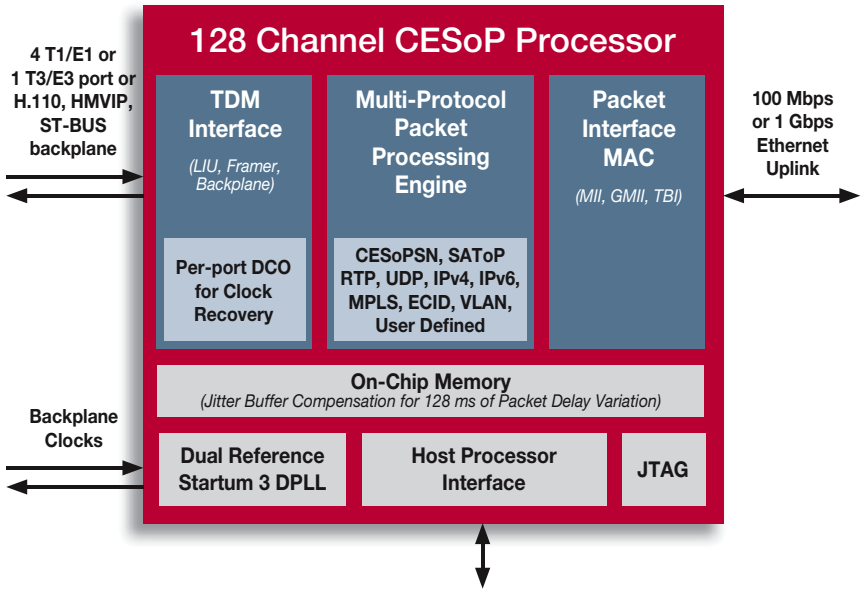
CESoP PROCESSORS ZL50115/6/7

PRODUCT PREVIEW

The ZL50117 family of low-density CES-over-Packet processors is a powerful and flexible method for carrying TDM voice and data traffic, with associated timing and signaling, across Ethernet, IP, and MPLS networks.

Each device provides a flexible TDM interface with embedded timing solution that fully meets T1/E1 timing and synchronization standards. With an integrated DPLL, internal jitter buffer memory and FE/GE packet interface, the ZL50117 processor family reduces BOM (bill of material) and board space and simplifies access equipment design.

ZL50117 Simplified Block Diagram



ZL50115	1 T1 or 1 E1 stream or 1 MVIP/ST-BUS stream at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 32 DS0 or Nx64 Kbps channels)
ZL50116	2 T1 or 2 E1 streams or 2 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps (Maximum of 64 DS0 or Nx64 Kbps channels)
ZL50117	4 T1 or 4 E1 streams or 1 J2, 1 T3, 1 E3 or 1 STS-1 stream or 4 MVIP/ST-BUS streams at 2.048 Mbps or 1 H.110/H-MVIP/ST-BUS streams at 8.192 Mbps

Applications

- Legacy traffic over PSN
- TDM over Wi-Fi and WiMAX
- 3G Wireless Backhaul

CESoP Processors Expand Reach

- Flexible TDM access interface supports T1/E1, T3/E3, H.110, H-MVIP and ST-BUS streams
- Nx64 kbps trunking for traffic grooming and fractional T1/E1 services
- Programmable multi-protocol packet encapsulation supports RTP, UDP, Ethernet VLANs, IPv4, IPv6 and MPLS, PWE3 and MEF Circuit Emulation standards

Carrier-Grade Voice Quality Support

- Patented hardware/software techniques for clock recovery and synchronization
- Advanced QoS mechanism allows traffic prioritization
- Extremely low and stable latency, intrinsic delays of <500 ms

Embedded Timing

- Embedded timing recovers clocks across packet networks
- Per-port T1/E1 clock recovery for asynchronous streams
- Adaptive clock recovery far exceeding G.823 for E1 and G.824/T1.403 for T1 timing
- Dual-reference Stratum 3 DPLL supports TDM H.110 and H-MVIP master and slave timing operation

Standard Compliant

- ITU-T recommendation Y.1413
- IETF PWE3 draft standards CESoPSN and SAToP
- MEF Implementation Agreement for PDH circuits (8.0)
- MPLS Forum CESoMPLS Implementation Agreement (8.0.0)

Customer Support

Evaluation boards and API are available, supported by Zarlink's network of in-house application engineers.

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APPLICATION

Access Networks

CES-over-Packet technology allows service providers to roll out packet-based access networks, while still providing customers with legacy T1/E1 services.

The diagram below shows how the ZL50117 low-density CESoP processor seamlessly emulates TDM traffic, such as POTS, T1/E1 and fractional T1/E1, across an IP, MPLS or Ethernet network. With Zarlink's CESoP processors, a wired, wireless or optical packet network infrastructure can deliver converged voice and data services.

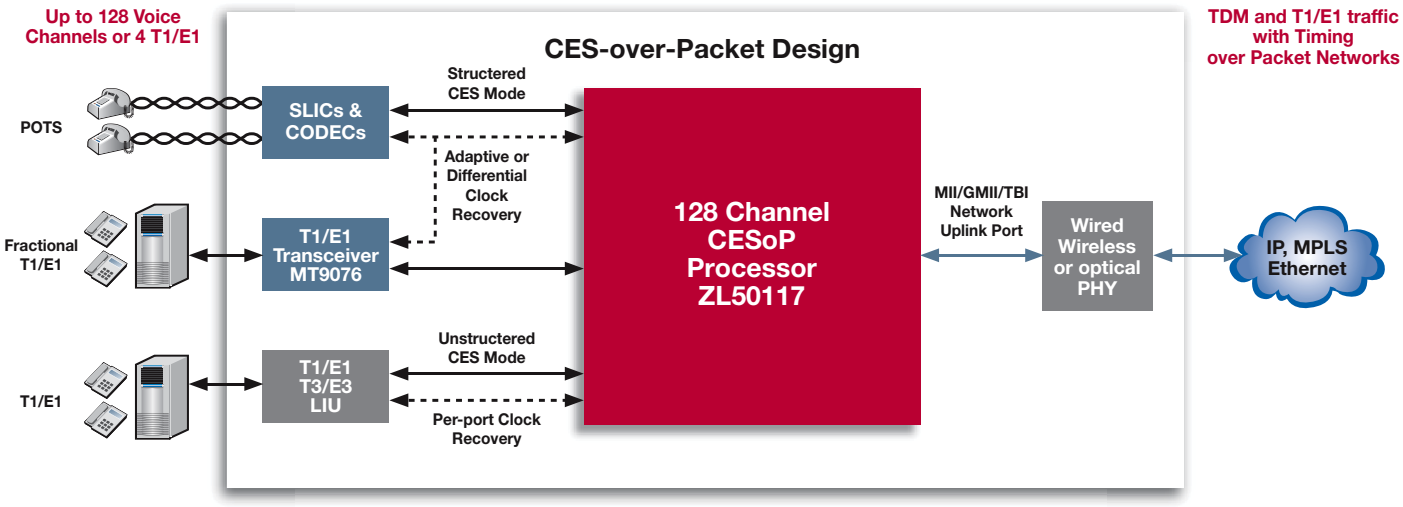
The TDM interface allows the device to be used directly with Codecs and framers in structured CES mode. In unstructured CES mode, the device interfaces directly to LIUs, providing independent timing recovery for each TDM port. The device supports up to 128 DS0, 4 T1/E1 or 1 J2.

The ZL50117 chip ensures high QoS, and supports four classes of service on packet egress for priority treatment of time-sensitive traffic. When packets are received from the Ethernet network, they are parsed to determine the egress destination, queued based on sequence number, with lost packets filled-in to maintain timing integrity.

An on-chip per-stream DCO (Digitally Controlled Oscillator) ensures precise synchronization of T1/E1 traffic across the packet network. Patent-pending software supports adaptive or differential timing so the best scheme can be used for a given application. For added flexibility, the ZL50117 processor can be configured to act as the master or slave timing source using the embedded Stratum 3/4/4E DPLL.

The ZL50117 device is equipped with on-board memory that compensates for up to 128 ms of PDV (Packet Delay Variations) in the network, with external support for up to 128 ms.

Zarlink offers the industry's only end-to-end portfolio of circuit-to-packet devices with densities ranging from 1 to 32 T1/E1 (32 to 1024 DS0) streams. The single-chip approach eliminates external circuitry, providing a cost-effective system-level solution that saves board space compared to equivalent discrete designs using communications processors.



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