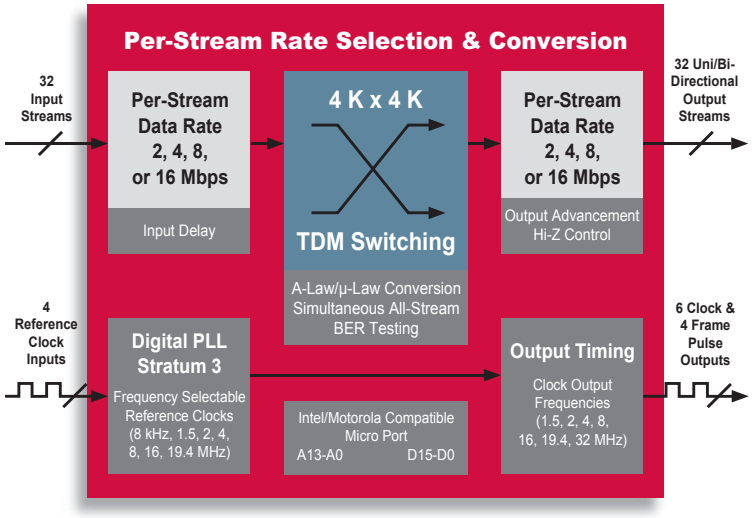
ZL50015/18/21

TDM/TSI SWITCH FAMILY WITH INTEGRATED DPLL

VOICE/DATA

ZL50021 Simplified Block Diagram



The ZL™50015/18/21 switching family is Zarlink's series of feature-rich TDM switching ICs for low-bandwidth networking equipment. As the industry's first low- and mid-density TDM switches with integrated high-performance DPLL (digital phase-locked loop) circuitry, the family includes 1 K, 2 K, and 4 K channel devices offering up to 32 input and 32 output or 32 bi-directional output streams with data rates from 2 Mbps to 16 Mbps. The family delivers a wide range of flexible features, including per-stream rate selection and conversion, and on-chip A-Law/μ-Law conversion and BER testing.

Typical Applications

- Remote access servers and concentrators
- Media gateways
- Wireless base stations
- Digital loop carriers
- PBX and IP-PBXs

Enhanced 1 K, 2 K and 4 K TDM Switches Deliver Unrivalled Performance

- 32 input and 32 output or 32 bi-directional streams
- Per-stream rate selection allows direct interface with peripheral components operating at different data rates
- Embedded A-Law/μ-Law code conversion
- Simultaneous all-stream Bit Error Rate (BER) testing eliminates external components
- Pin-to-pin compatibility between 1 K, 2 K and 4 K devices provides easy migration

Integrated DPLL for precise network timing and synchronization

- First commercially available 2 K and 4K TDM/TSI switches to integrate a Stratum 3 DPLL with holdover in a monolithic Integrated Circuit (ZL50018/21)
- DPLL accepts four independent input references, attenuates jitter below 1 ns, and generates industry-standard system clocks and frame pulses
- Range of programmable DPLL features, including filter corner frequency, locking range, and auto-holdover hysteresis range

Standards Compliant

- Exceeds Telcordia GR-1244-CORE requirements for Stratum 3 and 4E
- Telcordia GR-253-CORE for clock monitoring requirements
- ITU-T 0.151 requirements for per-stream BER detection
- ITU-T G.711 A-Law/μ-Law PCM encoding
- IEEE-1149.1(JTAG) standard

Related Products

- Voice echo cancellers
- T1/E1 transceivers
- TDM-to-IP processors

Customer Support

The ZL50015/18/21 TDM switching family is supported by Zarlink's network of in-house application engineers.

	Size	Streams	Integrated PLL	Package
ZL50015	1 K x 1 K	16 Input, 16 Output (Uni or Bi-Directional)	Stratum 4E	256-ball PBGA (17 x 17 mm) 256-pin LQFP (28 x 28 mm)
ZL50016			—	
ZL50018	2 K x 2 K	32 Input, 32 Output (Uni or Bi-Directional)	Stratum 3 DPLL	
ZL50019			Stratum 4E DPLL	
ZL50020			—	
ZL50021	4 K x 4 K	32 Input, 32 Output (Uni or Bi-Directional)	Stratum 3 DPLL	
ZL50022			Stratum 4E DPLL	
ZL50023			—	

ZARLINK SEMICONDUCTOR

ZL50015/18/21

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Applications

Zarlink's enhanced TDM/TSI switching family with integrated Stratum DPLL meets the density and flexibility requirements of low-bandwidth converged and wireless networking equipment, ranging from PBXs, IP-PBXs, integrated access devices and remote access concentrators, to wireless base stations and next-generation digital loop carriers.

The diagram below represents a typical implementation of a feature-rich 4 K x 4 K centralized switching architecture using currently available components and programmable logic devices. As illustrated, the integrated features of Zarlink's ZL50021 TDM switch reduce board space by combining the functionality of over five components in a high-performance 17 mm x 17 mm BGA package.

The ZL50021 is the first 4 K TDM switch with an on-chip DPLL exceeding Telcordia's Stratum 3 specification (GR-1244-CORE) to ensure network timing and synchronization. The device includes reference monitoring capability to ensure the quality of the four input clock references, and integrated software control mode providing efficient clock management in case of synchronization impairments.

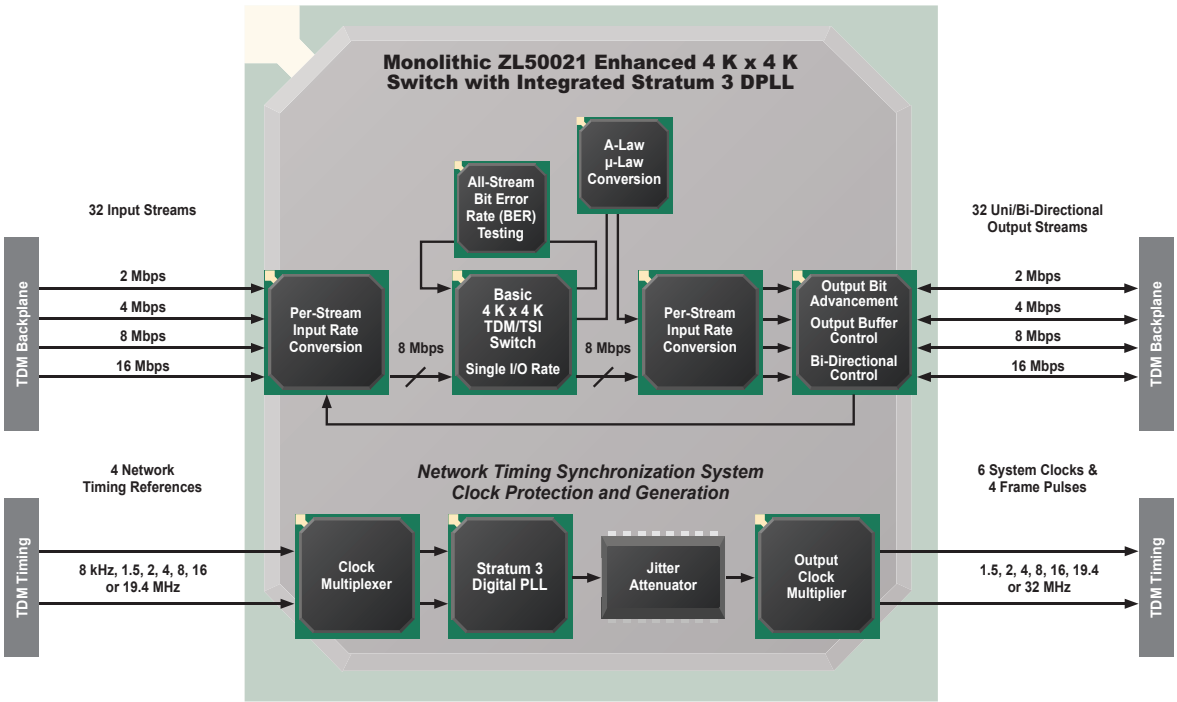
With low intrinsic jitter below 1 ns and multiple output clocks, the integrated DPLL eliminates the need for external devices, such as jitter attenuators and output clock multipliers.

The ZL50021 device offers 32 input and 32 output streams, or optionally 32 bi-directional streams, providing an easy interface to the TDM backplane. Patented rate conversion technology allows per-stream data rate selection from 2 Mbps to 16 Mbps. Designers can easily interface devices running at different data rates, providing easy bandwidth provisioning without requiring external rate converters.

The ZL50021 integrates unique features such as G.711 per-channel A-Law/μ-Law conversion to seamlessly convert between voice standards. Simultaneous Bit Error Rate (BER) testing on all I/O streams eliminate the need for programmable logic devices.

By combining advanced TDM switching and high-performance DPLL functions in a monolithic IC, the ZL50021 saves design and component costs while boosting the performance and reliability of low-bandwidth voice and data equipment.

Typical Feature-Rich 4 K x 4 K Centralized Switching Application



A single ZL50021 replaces over 5 components and programmable logic devices

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