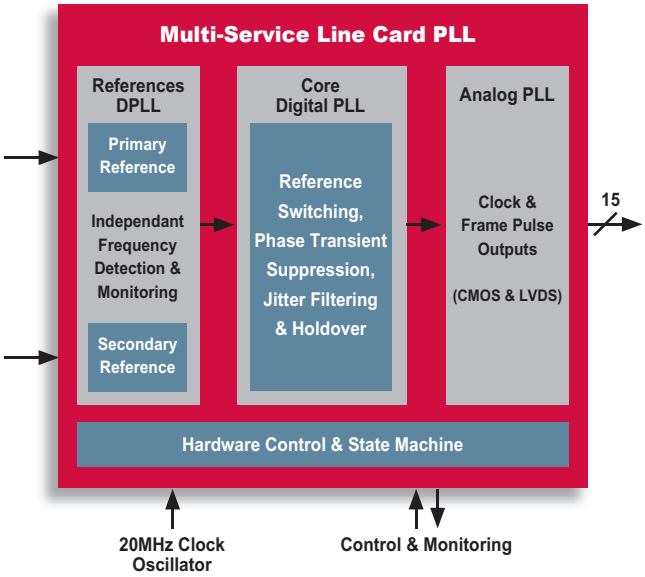
ZL30410
MULTI-SERVICE LINE CARD PLL

VOICE/DATA

ZL30410 Simplified Block Diagram



The ZL™30410 is a digital phase locked loop (DPLL) ideal for Synchronous Optical Network (SONET), Synchronous Digital Hierarchy (SDH) and T1/E1 line cards.

The ZL30410 is based on an enhanced DPLL architecture that ensures an efficient route to compliance with international synchronization standards. Featuring industry-leading jitter performance, reference out of range detection, and excellent holdover accuracy, the ZL30410 ensures reliable line card clocks even in the presence of jitter, wander and interruptions to the reference signal.

The new DPLL is a standard, IC-based solution that eliminates requirements for external loop filter components and reduces board space, cost and complexity compared to traditional DSP-based or module solutions.

Applications

- Line card synchronization for SDH, SONET, DS3, E3, J2 (DS2), E1 and DS1 interfaces
- Timing card synchronization for SDH Option 1 and PDH Network Elements
- Clock generation for ST-BUS and GCI timing

At a Glance

- Package: 80-pin LQFP
- Volume Production: Now

High Performance

- Industry-leading digital PLL jitter performance of 325ps on 155.52MHz clock allows a direct interface to STM-1/OC-3 framers and mappers.
- Very low MTIE after hitless reference switching between references with different frequencies.
- Automatic reference out of range detection continuously monitors timing references, and alarms if frequency error exceeds 12ppm.
- Holdover accuracy of 0.07ppb (10^{-9}) ensures precise timing when the network reference is down.

Flexible for Multiple System Requirements

- Supports free-run, normal (locked) or holdover modes.
- Selectable loop filter corner frequency supports line card (12Hz) and SDH Option 1 timing card (6Hz) applications.
- STM-1, OC-3, DS3, E3, 19.44MHz, DS2, E1, DS1, 8kHz and TDM bus clock outputs to 16.384MHz.
- Accepts reference inputs from two independent sources and synchronizes to any combination of 8kHz, 1.544MHz, 2.048MHz and 19.44MHz.

Simplifies Line Card Design

- Hardware interface control and status pins allow the device to operate without a dedicated microprocessor interface.
- External oscillator enhances flexibility with choice of size, source, quality and cost.

Standards Compliant

- ITU-T G.813 Option 1 and Option 2
- Telcordia GR-253-CORE

Customer Support

The ZL30410 is supported by a customer evaluation board, as well as with Zarlink's network of in-house field application and design engineers.

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SONET and SDH are the leading transport technologies for high-speed networks, offering versatility, reliability and the ability to support synchronous and asynchronous traffic. Synchronization of network elements in the SONET/SDH infrastructure is critical to system performance.

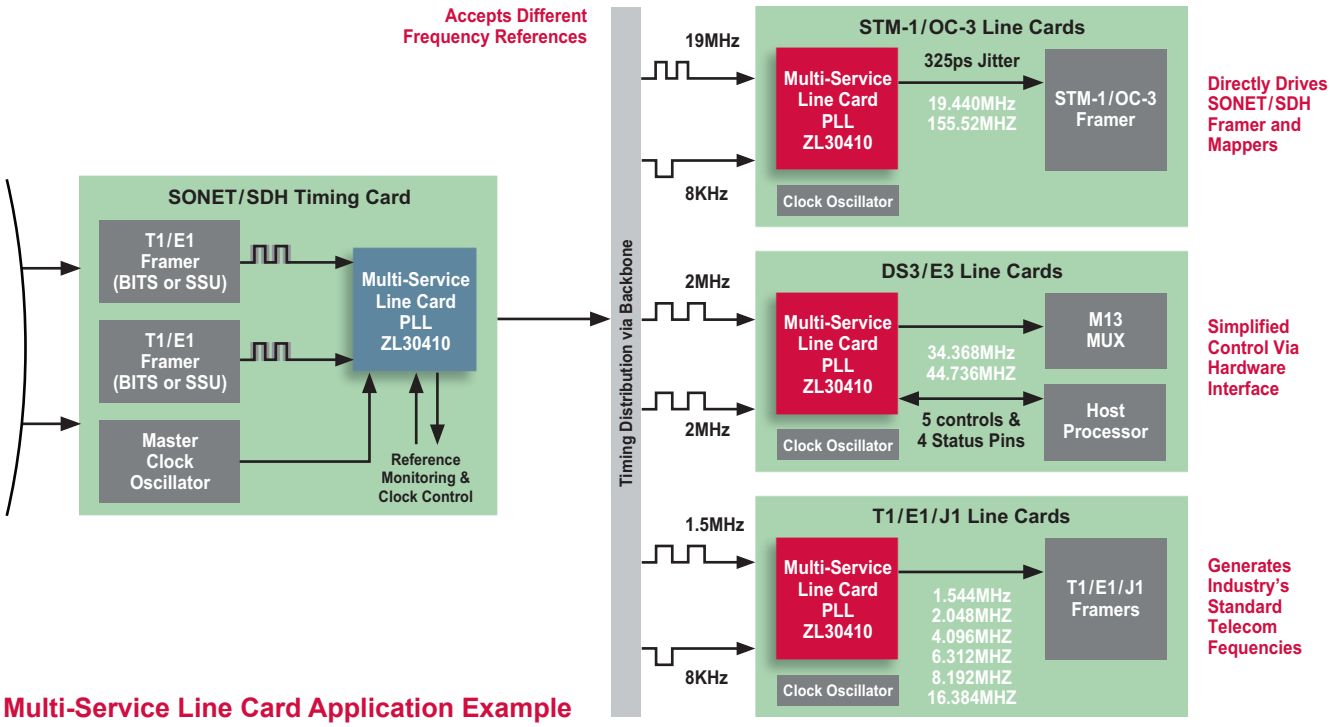
As shown below, the ZL30410 synchronizes line cards in compliance with the ITU-T G.813 Option 1 and Option 2, and the Telcordia GR-253-CORE specifications. Paired with a 20MHz clock oscillator, the ZL30410 provides line card clocks that support all of the stability requirements for wander, phase transient control and holdover.

The DPLL enables hitless reference switching between references of different frequencies, and provides Stratum 3E holdover accuracy of 0.07ppb. This allows network equipment to continue to send and receive data even when the source of network synchronization is interrupted or changed.

The ZL30410 further improves synchronization with reference out of range detection, which allows the device to verify the accuracy of reference signals, and reject references exceeding 12ppm.

Achieving the industry's best digital PLL jitter performance, the ZL30410 can directly drive jitter-sensitive STM-1 and OC-3 components. It also provides clocks and framing pulses required by commonly used STM-1, OC3 and T1/E1 framers and mappers. This eliminates requirements for a companion analog PLL or clock dividers, as well as external loop filters, thereby reducing cost, board space and complexity.

The ZL30410 can also serve as the main timing card DPLL in SDH Option 1 and T1/E1 stratum 4 or 4E systems. Equipped with hardware interface control and status pins, the device is able to operate in all modes without a dedicated microprocessor.



Multi-Service Line Card Application Example

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