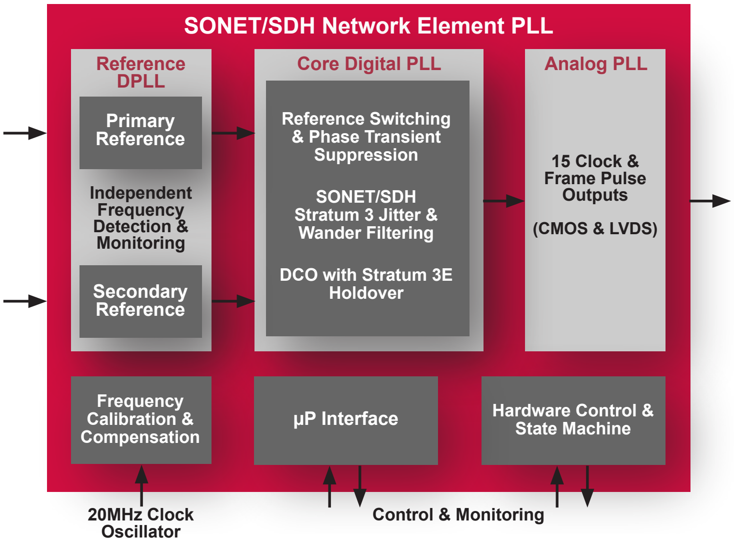
ZL30407
DIGITAL PLL

VOICE/DATA

ZL30407 Simplified Block Diagram



The ZL™30407 is a digital phase locked loop (DPLL) that synchronizes SONET (Synchronous Optical Network) and SDH (Synchronous Digital Hierarchy) network equipment.

The ZL30407 is based on an enhanced DPLL architecture that provides an efficient route to compliance with international synchronization standards. Featuring industry-leading jitter performance, reference out of range detection, and excellent holdover accuracy, the ZL30407 ensures that network clocks meet SONET Stratum 3, SONET minimum clock and G.813 requirements, even in the presence of jitter, wander and interruptions to the reference signal.

The new DPLL is a standard, IC-based solution that eliminates the requirements for external loop filter components and reduces board space, cost and complexity compared to traditional DSP-based or module solutions.

Applications

- SONET/SDH Add/Drop Multiplexers
- Mobile Switching Centers
- Internet Routers
- ATM Edge Switches

At a Glance

Package: 80-pin LQFP (pin-compatible with the MT90401 and ZL30402)
Volume Production: Now

High Performance

- Industry-leading digital PLL jitter performance of 325ps on 155.52MHz clock allows a direct interface to OC-3/STM-1 framers and mappers.
- Reference out of range detectors continuously monitor timing references and raise an alarm if frequency error exceeds 12ppm.
- Stratum 3 DPLL with Stratum 3E holdover accuracy of 0.001ppb (parts per billion) ensures precise timing when the network reference is down.
- Very low MTIE after hitless reference switching between references with different frequencies.
- Automatic reference frequency detection.

Flexible for Multiple System Requirements

- Supports free-run, normal (locked) or holdover modes.
- Selectable loop filter corner frequency supports SONET or SDH operation.
- OC-3/STM-1, DS3, E3, 19.44MHz, DS2, E1, DS1, 8kHz and TDM bus clock outputs to 16.384MHz.
- Accepts reference inputs from two independent sources and synchronizes to any combination of 8kHz, 1.544MHz, 2.048MHz and 19.44MHz.
- Programmable +/- phase adjustment of output clocks.

Simplifies Design

- Hardware and software control options enhance flexibility and simplify the design of advanced functionality.
- External oscillator enhances flexibility, offering the designer choice of size, source quality and cost.

Standards Compliant

- Telcordia GR-253-CORE for SONET Stratum 3 and SONET minimum clock
- Telcordia GR-1244-CORE for Stratum 3
- ITU-T G.813 Option 1 and Option 2

Customer Support

The ZL30407 is supported by a customer evaluation board, as well as with Zarlink's network of in-house field application and design engineers.

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Applications

SONET and SDH are the leading transport technologies for high-speed networks, offering versatility, reliability and the ability to support synchronous and asynchronous traffic. Synchronization of network elements in the SONET and SDH infrastructure is critical to system performance.

The ZL30407 offers an efficient route to meeting stringent synchronization requirements. As shown below, the device can be used at every node in the network where transmit data must by synchronized to a Stratum 1 reference clock.

The DPLL offers a range of synchronization features as well as excellent jitter performance that provides OEMs with confidence in meeting international specifications. Line cards built with the ZL30407 easily comply with Telcordia's GR-1244-CORE for Stratum 3, GR-253-CORE for SONET Stratum 3 and SONET minimum clocks, and the ITU-T's G.813 Option 1 and Option 2.

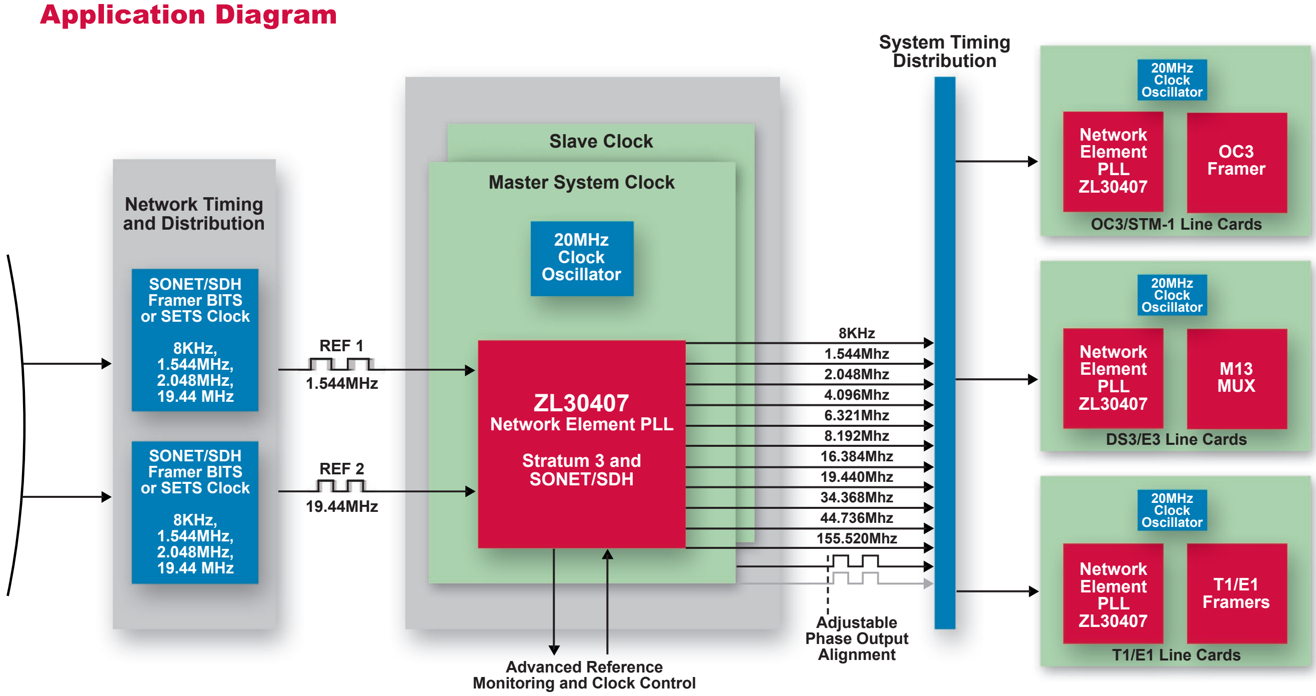
Paired with a 20MHz clock oscillator, the ZL30407 provides a complete SONET or SDH node clock that supports all of the stability requirements for wander, phase transient control and holdover. The Stratum 3 DPLL provides Stratum 3E holdover accuracy of 0.001ppb, allowing network equipment to continue to send and receive data even when the source of network synchronization is interrupted or changed.

The ZL30407 further improves synchronization with reference out of range detection, which allows the device to verify the accuracy of reference signals, and automatically reject references exceeding 12ppm range.

Achieving the industry's best digital PLL jitter performance at 155MHz, the ZL30407 can directly drive jitter-sensitive OC-3/STM-1 components. This eliminates requirements for a companion analog PLL, as well as external loop filters, thereby reducing cost, board space and complexity.

The ZL30407 is pin-compatible with Zarlink's MT90401 and ZL30402 DPLLs, allowing customers to easily upgrade systems for enhanced performance features.

Application Diagram



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