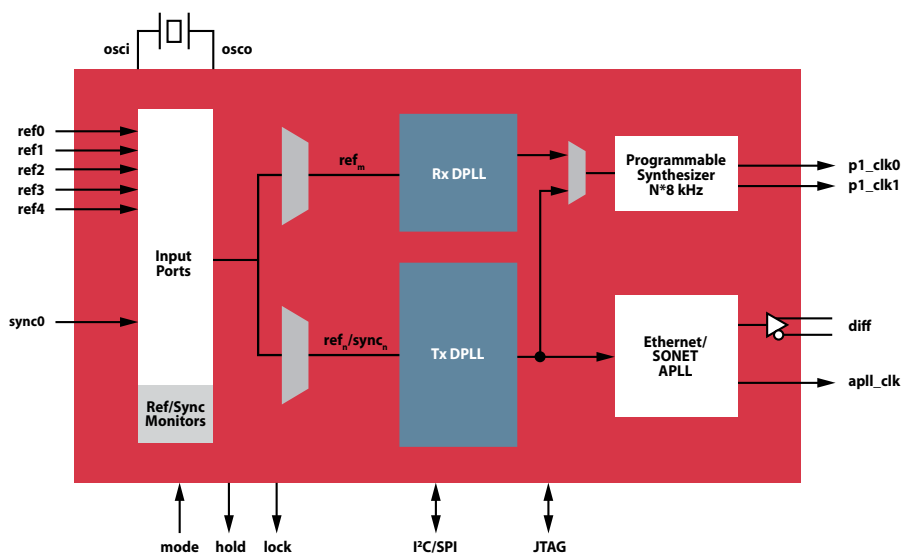


## PRODUCT PREVIEW

Zarlink's ZL30146 phase locked loop (PLL) is part of the Company's market-leading portfolio of single-chip Synchronous Ethernet solutions. The highly integrated products allow manufacturers to easily upgrade or design networking equipment that supports accurate end-to-end transmission of voice, video, data and mobile applications and services over IP-based wired and wireless networks.

Targeting line card applications, the ZL30146 chip incorporates two independently configurable DPLLs for PDH/SONET/SDH and Ethernet network interface cards requiring both transmit and receive paths. The device requires only off-the-shelf, low-cost 20 MHz oscillators or even a crystal, where competing devices require an expensive high precision clock or high frequency rate oscillator. As a result, manufacturers can quickly and cost-effectively upgrade line cards to fully support Synchronous Ethernet.

Zarlink's Synchronous Ethernet solutions are the only single-chip products in full compliance with the International Telecommunications Union (ITU-T) Recommendation G.8262.



### Applications

- ➔ ITU-T G.8262 line cards supporting 1 GE and 10 GE interfaces
- ➔ SONET/SDH line cards up to OC-192/STM-64

### Highly Integrated SyncE Solution for Line Cards

- ➔ Synchronizes to standard telecom or Ethernet backplane clocks and provides jitter filtered output clocks for SONET/SDH, PDH and Ethernet network interface cards
- ➔ Supports the requirements of ITU-T G.8262 for synchronous Ethernet equipment slave clocks
- ➔ Meets the SONET/SDH jitter generation requirements up to OC-192/STM-64
- ➔ Two independent DPLLs provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- ➔ Synchronizes to telecom reference clocks (2 kHz, N\*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- ➔ Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, 3.5 Hz, 1.7 Hz, or 0.1 Hz
- ➔ Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- ➔ Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs
- ➔ Programmable output synthesizer to generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz (e.g., T1/E1, DS3/E3)
- ➔ Generates several styles of output frame pulse with selectable pulse width, polarity, and frequency
- ➔ Configurable input to output delay and output to output phase alignment
- ➔ Configurable through a serial interface (SPI or I2C)
- ➔ DPLLs can be configured to provide synchronous or asynchronous clock outputs

## APPLICATION

### Timing for PDH/SONET/SDH and Ethernet Network Interface Cards

The ZL30146 OC-192/STM-64 PDH/SONET/SDH/Synchronous Ethernet Network Interface Synchronizer is a highly integrated device that provides timing for both PDH/SONET/SDH and Ethernet network interface cards.

The device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (Tx DPLL, Rx DPLL) which are both independently configurable through the serial interface (SPI or I<sup>2</sup>C).

As illustrated below, the ZL30146 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 622.08 MHz or 156.25 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. On the receive path, the Rx DPLL and the programmable synthesizer translate the line recovered clock (8 kHz or 25 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30146 allows easy integration of Ethernet line rates with today's telecom backplanes.

