SONET/SDH LINE CARD SYNCHRONIZER **ZL30117/22**

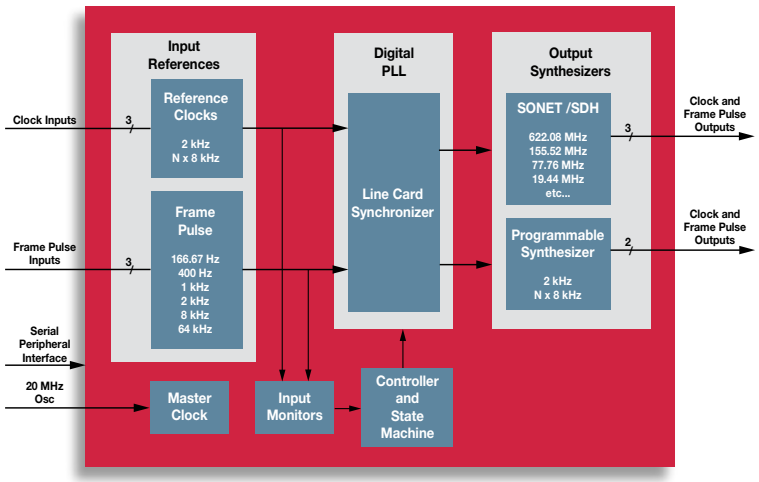
PRODUCT PREVIEW

Zarlink's ZL30117 and ZL30122 chips are the industry's smallest, lowest power programmable analog/digital PLLs that solve the timing challenges posed by the popular AdvancedTCA (telecommunications computing architecture), AMC (advanced mezzanine card) and MicroTCA architectures.

Highly integrated devices, the ZL30117/22 PLLs combine the hitless reference switching capabilities of a digital PLL with the jitter performance of an analog PLL. The ZL30117 and ZL30122 are pin compatible and software compatible devices differentiated by jitter performance. With ultra-low jitter performance of less than 1ps, the ZL30117 can be used in applications up to OC-192/STM-64. The ZL30122 limits jitter to less than 3ps and can be used for applications up to OC-12/STM-16. The ZL30117/22 devices accept three reference inputs, supporting clock frequencies in any multiple of 8 kHz up to 77.76 MHz, as well as supporting 2 kHz. The ZL30117/22 can directly lock to any of the three standard clock inputs available to an AMC in an ATCA or MicroTCA application. The holdover capability of the ZL30117/22 chips also enables them to ride out a complete loss of an incoming reference, which can occur when switching from a failed clock unit to a backup clock unit. The ZL30117/22 PLLs continue to operate in full compliance with network requirements for several seconds after losing their reference, allowing time for the system to switch to another reference source.

Simplifying design, the device synthesizes SONET/SDH interface clocks, tributary clock families and SBI or Telecom busses without requiring significant board space or the use of multiple PLLs.

ZL30117/22 Simplified Block Diagram



Applications

- WAN router line cards
- DSLAM line cards
- RNC/Mobile switching center line cards
- Next generation SONET/SDH line cards
- AdvancedTCA™ boards
- Advanced Mezzanine Cards

Integrated Timing Chips for SONET/SDH Line Cards

- Pin compatible and software compatible single-chip devices integrate reference switching performance of a DPLL with jitter generation of an APLL
  - ZL30117 meets jitter requirements up to OC-192/STM-64
  - ZL30122 meets jitter requirements up to OC-12/STM-16
- Configurable DPLL
  - Provides all features for generating SONET/SDH compliant clocks
- PLL operates in free-run, normal and holdover modes and provides automatic hitless reference switching
- CMOS outputs for 19.44 MHz and 77.76 MHz clocks eliminate external dividers or clock multiplying PLLs
- Programmable frame pulse formatter replaces CPLD or FPGA gates
- Selectable output clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz) eliminate external dividers & clock multiplying DPLLs
- Programmable output synthesizers generate clock frequencies from any multiple of 8 kHz up to 77.76 MHz and 2 kHz
- Three reference inputs supporting clock frequencies in any multiple of 8 kHz up to 77.76 MHz and 2 kHz
- Meets Telcordia GR-253-CORE and ITU-T G.813 jitter requirements up to OC-192/STM-64

Customer Support

The ZL30117 and ZL30122 chips are supported by evaluation boards, reference designs and Zarlink's network of in-house field application and design engineers.

ZARLINK SEMICONDUCTOR

ZL30117/22 SONET/SDH LINE CARD SYNCHRONIZER

APPLICATION

Advanced Mezzanine Card Synchronization

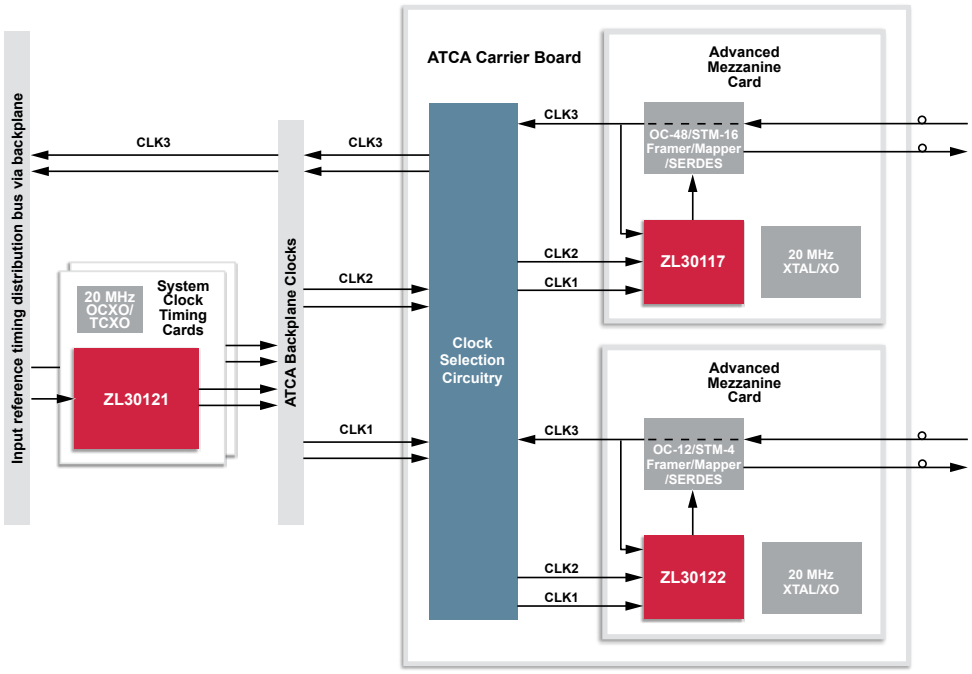
Zarlink's ZL30117 and ZL30122 are compact, highly integrated PLLs that synthesize SONET/SDH interface clocks, tributary clock families and SBI or Telecom bus clocks locked to backplane references. Incorporating digital and analog PLLs, these single chip devices manage timing for next-generation SONET/SDH platforms operating at speeds up to OC-192/STM-64. The ZL30117 and ZL30122 are pin compatible and software compatible devices differentiated by jitter performance. With ultra-low jitter performance of less than 1ps, the ZL30117 can be used in applications up to OC-192/STM-64. The ZL30122 limits jitter to less than 3ps and can be used for applications up to OC-12/STM-16. Competing two-chip or module approaches are more than twice the size of the ZL30117/22 and require external devices to manage high-speed network timing.

As illustrated below the ZL30117/22 can lock to any of the CLK1, CLK2 or CLK3 AMC (advanced mezzanine card) clock signals. When the ACTA carrier board switches its timing source between the redundant ATCA backplane clocks, the clock selection circuitry needs only to squelch its clock outputs to force the ZL30117/22 into holdover and then switch over to the new clock source. The ZL30117/22 prevents bit errors during the switch-over by continuing to generate stable clocks.

The ZL30117/22 can be configured to manually or automatically switch between valid input references upon reference failure. When using automatic reference switching, reference selection criteria is based on input priority and an optional revertive feature ensures the highest priority valid reference is always selected. When no valid references are available, the device automatically enters holdover mode and continues to generate output clocks based on historical reference frequency data.

The ZL30117/22 can simultaneously generate five output clocks from two independent clock frequency families. Common SONET/SDH clock frequencies, programmable n x 8 kHz clock frequencies and a variety of programmable frame pulses can be generated simultaneously. Programmable phase delay adjustment and programmable frame pulse formatting is also available and both CMOS and differential LVPECL outputs are provided. This means virtually any required frequency can be generated and adjusted as required, eliminating the need for additional oscillators, external dividers, clock multiplying PLLs or level translation devices.

Delivering leading integration, flexibility, programmability and performance, the ZL30117/22 can be implemented as the sole timing and synchronization source for virtually any line card deployed in multi-service provisioning and multi-service switching platforms.



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