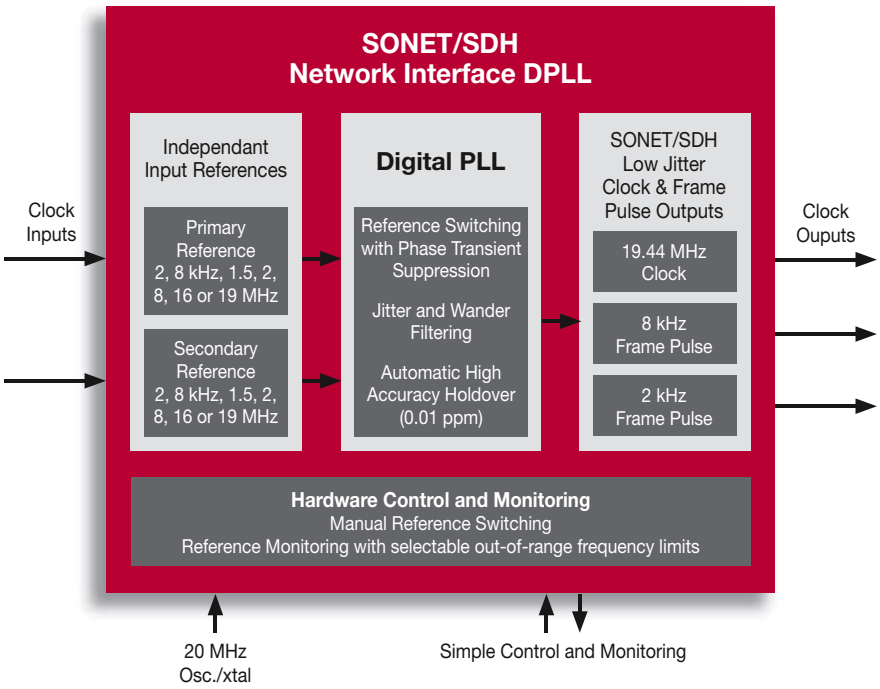
DIGITAL PLL **ZL30108**

PRODUCT PREVIEW

The ZL30108 is the world's smallest digital phase locked loop (DPLL) for SONET/SDH line cards in high-speed networking equipment.

Measuring just 5 mm x 5 mm, the device provides high-performance line card synchronization that surpasses all OC-3/STM-1 specifications. With integrated features, including reference monitoring, reference switching, automatic holdover, jitter filtering and jitter shaping, the DPLL ensures reliable line card clocks even in the presence of jitter, wander and interruptions to the reference signals.

The ZL30108 can be used in combination with Zarlink's family of analog PLLs to provide an easy-to-implement, compact timing and synchronization solution for high-speed SONET/SDH network equipment.



Applications

- Line card synchronization for SONET and SDH systems
- Wireless base station network interface cards

Packaging and Availability

- Ultra-compact (5 mm x 5 mm) 32-pin QFN package
- Available now in production quantities

High Performance/Small Package

- Small 5 mm x 5 mm package addresses dense SONET/SDH line card "real estate" constraints
- Jitter performance better than 24 psrms on 19.44 MHz clock, allowing a direct interface to OC-3/STM-1 framers and mappers
- Accepts two input references, synchronizing to 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz and 19.44 MHz frequencies
- Automatic reference frequency detection with reference out-of-range detectors continuously monitor timing references and raise an alarm if frequency error exceeds user-defined limits
- Accurate holdover ensures precise timing if the network reference is temporarily lost
- Innovative jitter shaping and filtering techniques ensure compatibility with Zarlink analog PLLs for higher-speed timing and synchronization

Simplifies Design of Line Cards

- Supports free-run and normal (locked) modes
- Automatic entry into Holdover and return from Holdover
- Simplified control via hardware interface pins to operate the device without the need for a dedicated microprocessor interface
- External oscillator/crystal enhances flexibility, offering designers choice of size, source, quality, cost

Standards Compliant

- ITU-T G.813 STM-1 jitter performance
- Telcordia GR-253-CORE OC-3 jitter performance

Customer Support

The ZL30108 is supported by a customer evaluation board and Zarlink's network of in-house field application and design engineers.

ZARLINK SEMICONDUCTOR

SONET/SDH Line Card Timing

SONET and SDH are the leading transport technologies for high-speed networks, offering versatility, reliability and the ability to support synchronous and asynchronous traffic.

Zarlink's ZL30108 DPLL provides the best combination of features, jitter performance and small size for SONET/SDH line cards operating at rates up to OC-3/STM-1. The device can also be used in combination with Zarlink's family of analog PLLs to provide end-to-end timing and synchronization for higher-speed networking equipment.

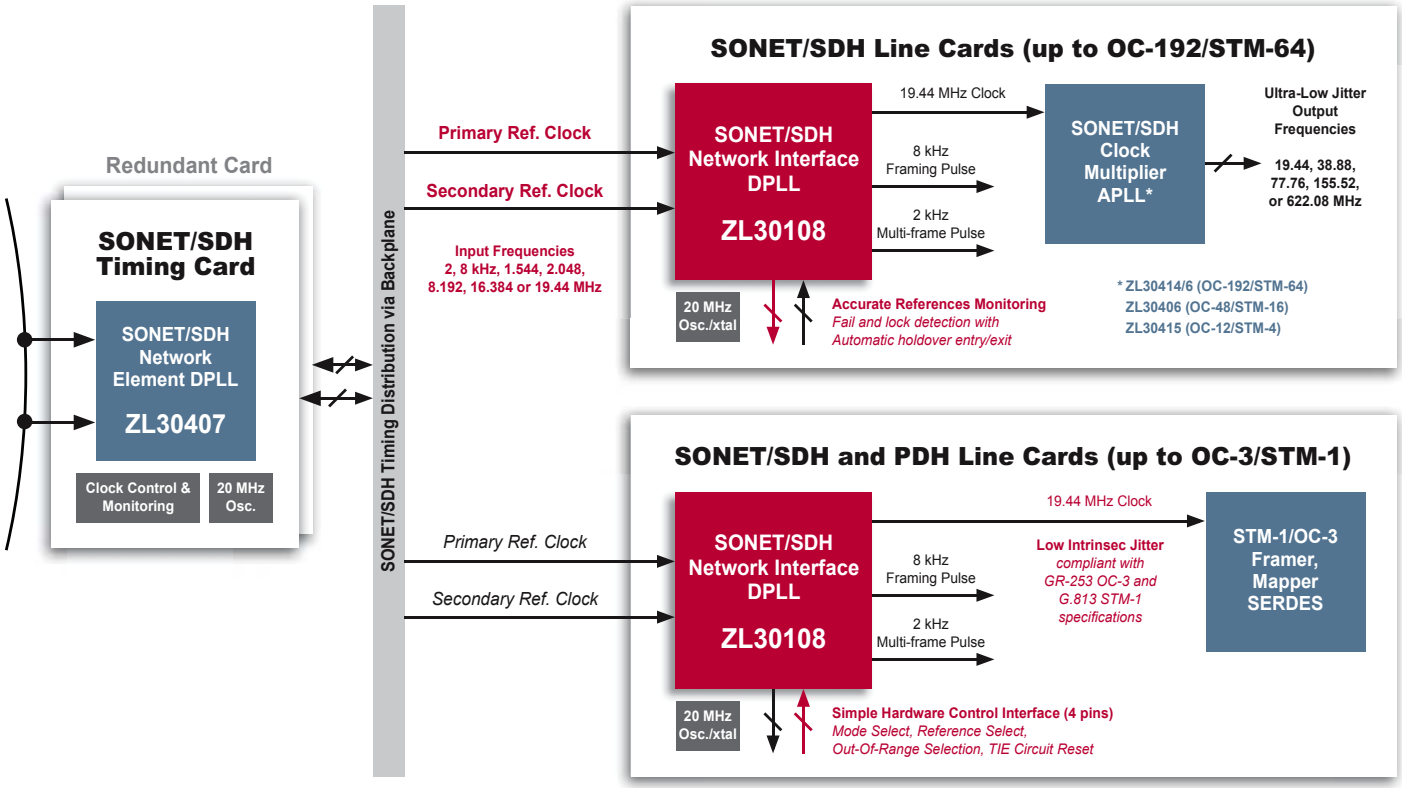
As illustrated below, the ZL30108 accepts a primary and secondary input reference synchronized to a wide range of frequencies. Each input is continuously monitored for frequency accuracy and pulse quality.

When the network frequencies are outside the programmable frequency range, the ZL30108 provides hitless reference switching between the primary and secondary clock without any phase disruption to the line card clocks and frame pulses.

The ZL30108 provides a 19.44 MHz clock output with jitter performance of better than 24 psrms, delivering significant jitter margin versus OC-3/STM-1 specifications. The device also produces an 8 kHz framing pulse and 2 kHz multi-frame pulse with less than 0.5 nspp.

With the rollout of increasingly complex, high-speed network architectures, designers must use combinations of digital and analog PLLs working in tandem. With innovative techniques, jitter from the ZL30108 can be shaped so it produces lower jitter, or is easily filtered by a Zarlink analog PLL for higher frequency applications.

For example, the ZL30108 DPLL and ZL30415 analog PLL can be used in tandem to provide and end-to-end, extremely compact and easy-to-implement timing and synchronization solution for OC-12/STM-4 line cards.



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