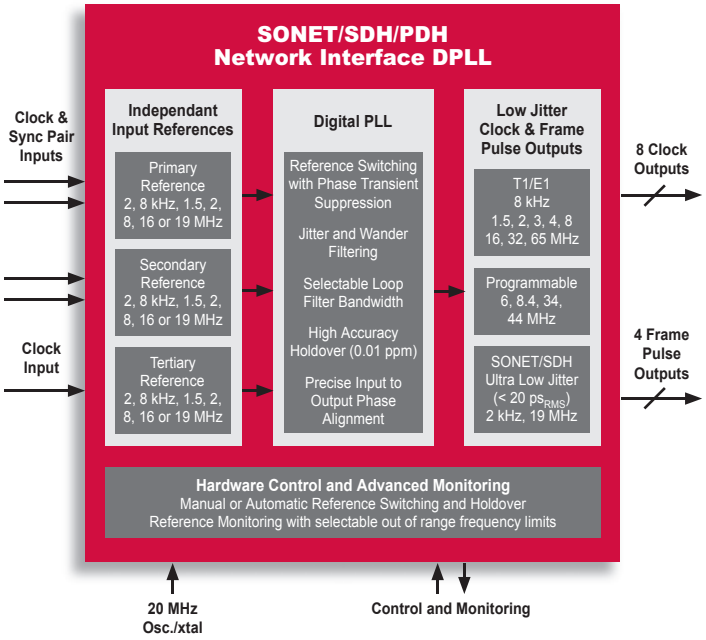
ZL30106

SONET/SDH/PDH NETWORK INTERFACE DIGITAL PLL

VOICE/DATA



The ZL™30106 is a DPLL (digital phase locked loop) that synchronizes SONET/SDH and PDH line cards.

The ZL30106 is based on an enhanced DPLL architecture that provides an efficient route to compliance with international synchronization standards. Featuring industry-leading jitter performance, reference out-of-range detection, and excellent holdover accuracy, the ZL30106 ensures reliable line card clocks in the presence of jitter, wander and interruptions to the reference signal.

This new DPLL is a standard, IC-based device that eliminates the requirements for external loop filter components and reduces board space, cost and complexity compared to traditional approaches.

Applications

- Line card synchronization for SONET, SDH and PDH systems
- Wireless base station network interface cards
- AdvancedTCA™ and H.110 line cards

High Performance

- Industry-leading digital PLL jitter performance of 20 ps_{RMS} on 19.44 MHz clock allows a direct interface to STM-1/OC-3 framers and mappers
- Accepts three reference clocks that synchronize to any combination of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz and 19.44 MHz
- Automatic reference frequency detection with reference out-of-range detectors continuously monitors timing references and raise an alarm if frequency error exceeds user defined limits
- Primary and secondary input references synchronize to clock-and-sync pair
  - Provides phase re-alignment of misaligned references
  - Enables simultaneous hitless reference switching of a clock-and-sync pair
  - Allows wide-bandwidth DPLL operation with low-frequency references
- Accurate holdover ensures precise timing when the network reference is down

Simplifies Design of Line Cards

- Supports free-run, normal (locked), holdover or automatic modes
- Selectable loop filter corner frequency of 29 Hz or 922 Hz supports multiple line card configurations
- Provides a range of clock outputs for SONET/SDH, DS3/E3, DS2/E2, DS1/E1, and TDM bus
- Tertiary reference clock input offers additional synchronization and monitoring for the line card
- Simplified control via hardware interface pins for device operation, without the need for a dedicated microprocessor interface
- External xtal./oscillator enhances flexibility, offering the designer choice of size, source, quality and cost

Packaging and Availability

- 64-pin TQFP package
- Available now in production quantities

Standards Compliant

- ITU-T G.813 Option 1 and Option 2 STM-1 jitter performance
- Telcordia GR-253-CORE OC-3 jitter performance

Customer Support

The ZL30106 is supported by a customer evaluation board and Zarlink's network of in-house field application and design engineers.

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Applications

SONET and SDH are the leading transport technologies for high-speed networks, offering versatility, reliability and the ability to support synchronous and asynchronous traffic. As shown below, the ZL30106 can be used to provide fully featured, high-performance line card synchronization, complying with ITU-T and Telcordia OC-3/STM-1 jitter specifications.

The ZL30106 accepts a wide range of standard reference clock and frame pulse frequencies. Each reference input is monitored within its specific frequency range and maximum frequency deviation limits. The device simultanously synchronizes to clock-and-sync pair references, enabling a wide bandwidth PLL operation while synchronized to a low-frequency frame pulse.

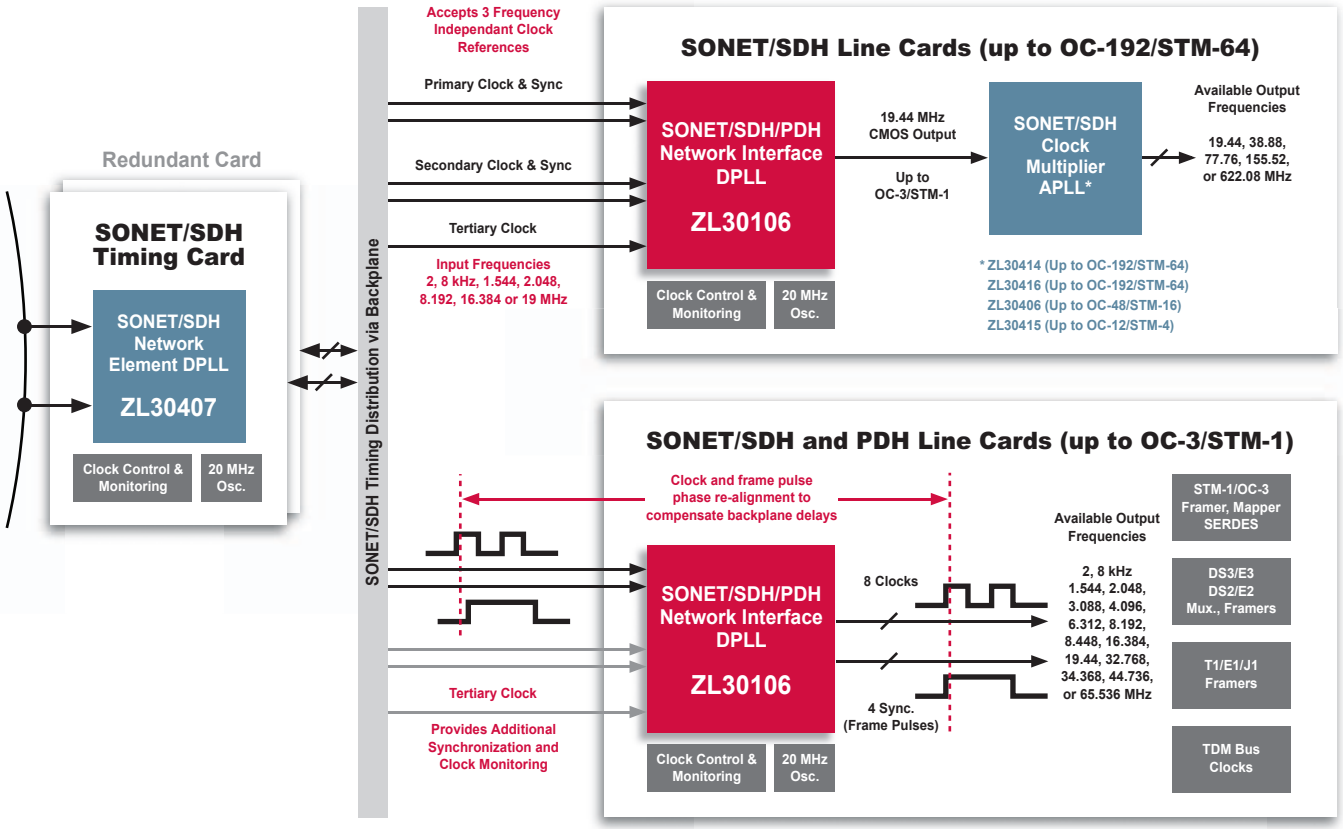
When the network frequencies are outside the programmable frequency range, the ZL30106 provides hitless reference switching between the primary and secondary clock and sync pair references without any phase disruption to the line card clocks and frame pulses.

When clock references are down, the ZL30106's holdover mode keeps the line card clocks accurate within 0.01 ppm of the previous valid reference. The tertiary reference clock input offers additional synchronization and monitoring for the line card.

Clock and frame pulse signals are often skewed by backplane delays, which reduces timing signal margins. The ZL30106 eliminates this effect by providing precise phase re-alignment of the active clock and sync references.

Achieving the industry's best digital PLL jitter performance, the ZL30106 offers a wide range of clocks and frame pulses that can directly drive jitter-sensitive STM-1 and OC-3 components. Zarlink also offers a range of high-performance clock multiplier analog PLLs for SONET/SDH line cards from OC-12/STM-4 up to OC-192/STM-64.

SONET/SDH/PDH Line Card Timing Application



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