DIGITAL PLL **ZL30100/1/9**

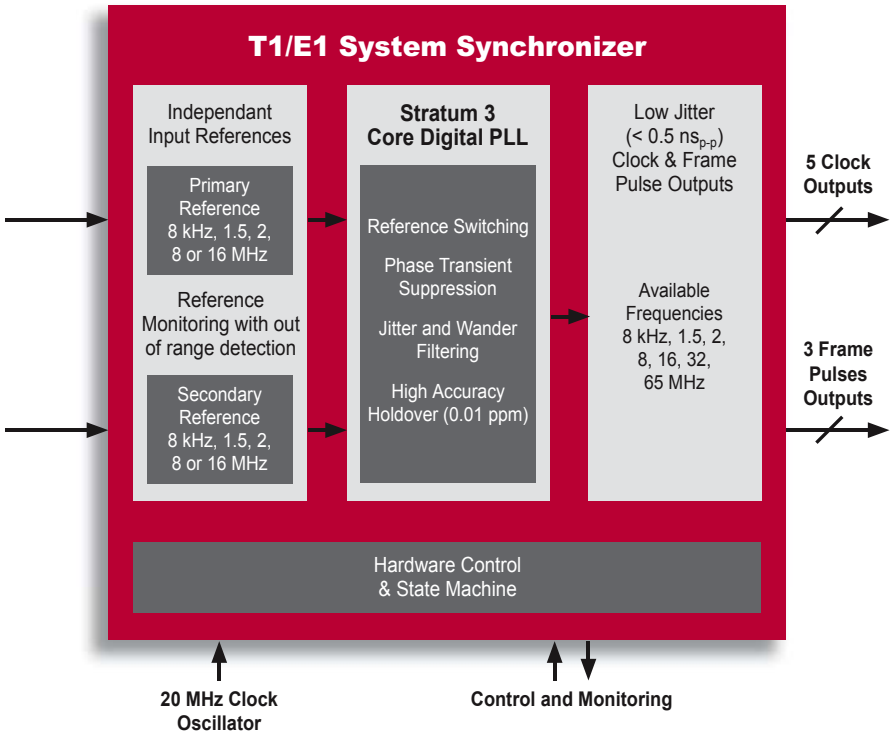
PRODUCT PREVIEW

The ZL30100/1/9 is Zarlink's series of high-performance digital phase-locked loops (DPLLs) ideal for synchronization and timing control of multi-trunk T1/E1 systems.

The ZL30100/1/9 is based on an enhanced DPLL architecture that ensures an efficient route to compliance with international synchronization standards. Featuring industry-leading jitter performance, flexible reference monitoring, and excellent holdover accuracy, the ZL30100/1/9 efficiently regulates critical synchronization in access, edge and customer premises equipment.

The ZL30101 digital PLL is well suited for central office and edge equipment demanding Stratum 3 timing. The ZL30100/9 digital PLLs provide a timing solution meeting Stratum 4/4E requirements for customer premises access equipment.

ZL30101 Simplified Block Diagram



Applications

- Synchronization and timing control for multi-trunk T1/E1 systems, such as DSLAMs, media gateways, wireless base stations and IP-PBXs
- Clock and frame pulse source for ST-BUS, GCI and other TDM buses
- Line card synchronization for PDH systems

Packaging and Availability

- Package: 64-pin TQFP
- Volume production: Now

Superior Jitter Performance and Enhanced Features for Range of Applications

- Pin-compatible digital PLLs meeting requirements for access, edge and customer premises equipment
  - ZL30100 & ZL30109 Stratum 4/4E
  - ZL30101 Stratum 3
- Industry-leading digital PLL jitter performance of less than 0.5 nanoseconds peak-to-peak
  - 24 ps_{RMS} maximum on 19.44 MHz clock (ZL30109)
- Exceptional holdover performance of 0.01 ppm for Stratum 3 systems and 0.15 ppm for Stratum 4/4E systems
- Accepts two input references and synchronizes to any combination of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz
  - ZL30109 also accepts 2 kHz and 19.44 MHz
- Reference monitoring capability with selectable limits continuously monitors the quality of timing references
- Supports free run, normal (locked) or holdover modes
- Provides a range of clock outputs: 1.544 MHz, 2.048 MHz, 16.384 MHz and either 4.096 MHz and 8.182 MHz or 32.768 MHz and 65.536 MHz
  - ZL30109 also generates 19.44 MHz
- Supports five styles of 8 kHz frame pulses
  - ZL30109 also supports a 2 kHz multi-frame pulse
- Simple hardware control interface allows the device to operate without a dedicated microprocessor interface

Standards Compliant

- Telcordia GR-1244-CORE for Stratum 3 and Stratum 4/4E
- ITU-T G.823, G.824
- ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interfaces

Customer Support

The ZL30100/1/9 is supported by a customer evaluation board and Zarlink's network of in-house field application and design engineers.

ZARLINK SEMICONDUCTOR

ZL30100/1/9 DIGITAL PLL

APPLICATION

Network Timing Distribution

Access, edge and customer premises equipment must be able to meet very strict international standards for timing and synchronization to ensure accurate system performance.

As illustrated below, the ZL30100/1/9 digital PLLs provide a complete off-the-shelf timing solution in a range of networking equipment.

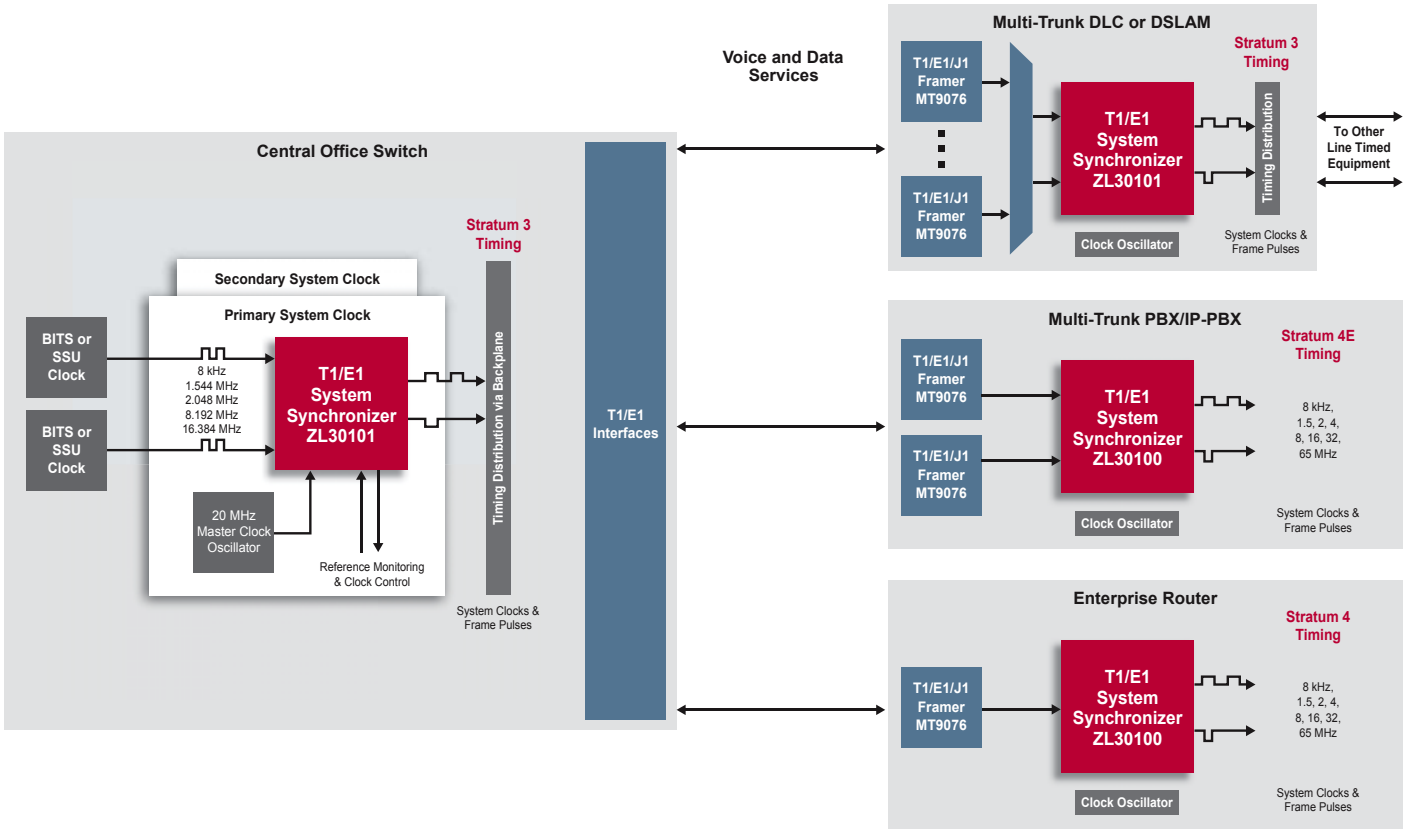
The ZL30101 digital PLL delivers the jitter performance and enhanced features for central office and edge equipment requiring Stratum 3 timing. The ZL30101 timing chip's holdover capability of 0.01 ppm allows this equipment to send and receive data even when the network synchronization source is lost or interrupted, ensuring there is no disruption in service for subscribers.

Line-timed customer premises and remote access equipment such as IP-PBXs, remote DSLAMs or enterprise routers and gateways, extracts its timing information from the same T1/E1 trunks that carry data. This equipment requires highly reliable clocks synchronized with central office equipment to ensure the proper flow of data between emerging and legacy networks.

The ZL30100 digital PLL allows designers to cost-effectively design a timing solution meeting Stratum 4/4E requirements for customer premises equipment. The device provides clocks meeting international standards during normal operation. Enhanced reference monitoring and switching capabilities allow the device to switch the source of timing from a failed interface to an operational interface without losing data.

On their inputs, both timing chips accept two references and automatically synchronize to any combination of 8 kHz, 1.544 MHz, 2.048 MHz, 8.192 MHz or 16.384 MHz. The digital PLLs deliver the most complete range of output clocks for Stratum 3 and Stratum 4/4E systems, including T1/E1 interface clocks as well as ST-BUS clocks and frame pulses up to 65.536 MHz, with industry-leading jitter performance of less than 0.5 ns (nanoseconds) peak-to-peak.

The ZL30100/1/9 digital PLLs allow designers to easily and cost-effectively meet Stratum 3 and Stratum 4/4E requirements to ensure the reliable transport of voice, data and multimedia traffic over a full range of networking equipment.



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