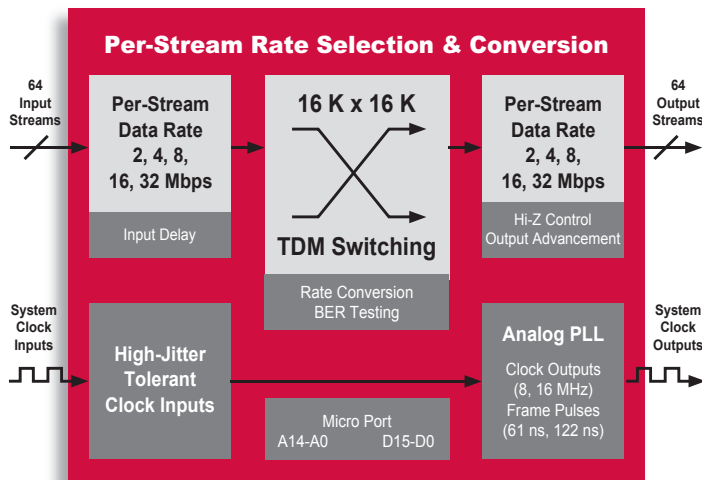


ZL50060 Simplified Block Diagram



The ZL™ 50050/51/52/53/57/58/60/61/62/63/64 are Zarlink's series of feature-rich TDM switching ICs. The series includes 8 K, 12 K and 16 K channel devices capable of up to 32 Mbps data rates on all streams. With exceptional jitter tolerance, as well as the industry's widest range of per-stream and per-channel programmable features, Zarlink's new switching ICs are ideal for a variety of high-capacity carrier-class equipment.

Typical Applications

- ➔ Media gateways
- ➔ Central office and Class 5 switches
- ➔ Remote access servers and concentrators
- ➔ Next-generation digital loop carriers
- ➔ Wireless base stations

8 K, 12 K and 16 K Feature-Rich Switches with Enhanced Flexibility

- ➔ Widest range of non-blocking switching ICs including 8 K, 12 K and 16 K channel devices offered with or without rate conversion
- ➔ Per-stream programmable rate selection at 2, 4, 8, 16 or 32 Mbps with rate conversion allows direct interface to peripheral components at different data rates
- ➔ Exceptional jitter tolerance of 17 ns at less than 32 Mbps, and 14 ns for 32 Mbps traffic allows direct use of clock signals from a backplane or a low cost digital PLL
- ➔ Flexible per-stream Input delay and Output advancement allows stream alignment adjustment to compensate for bus delays:
 - Input delay with channel and bit delay of up to 7 ¾ bits with ¼ bit resolution
 - Output advancement of 0 to 45 ns with resolution of 15 ns at less than 32 Mbps, and 0 to 22 ns with a resolution of 7.6 ns at 32 Mbps
- ➔ Two frame constant delay ensures frame integrity
- ➔ Backward compatibility with Zarlink's existing 8 K, 12 K and 16 K devices allows existing customers to easily upgrade their systems

Standards Compliant

- ➔ H-MVIP, MVIP, ST-BUS, GCI
- ➔ IEEE 1149.1 (JTAG)

Related Products

- ➔ Phase locked loops
- ➔ Voice echo cancellers
- ➔ Framers

Customer Support

Evaluation boards and API drivers are available for the ZL50050 series of switching ICs, supported by Zarlink's network of in-house application engineers.

	Size	Streams	Description	Package
ZL50050	8 K x 8 K	32 In/32 Out	Fully featured switch with per-stream rate selection and conversion	PBGA (pin compatible with MT90871)
ZL50051/53	8 K x 8 K	64 In/64 Out	Basic switch supporting 8 and 16 Mbps I/O rates	PBGA, LQFP
ZL50052	8 K x 8 K	16 In/16 Out	Basic switch supporting 32 Mbps I/O rate	PBGA
ZL50057/58	12 K x 12 K	48 In/48 Out	Fully featured switch with per-stream rate selection and conversion	PBGA (ZL50070 pin compatible with MT90870)
ZL50060/61	16 K x 16 K	64 In/64 Out	Fully featured switch with per-stream rate selection and conversion	PBGA (ZL50061 pin compatible with MT90869)
ZL50062/64	16 K x 16 K	64 In/64 Out	Basic switch supporting 2, 4, 8 and 16 Mbps I/O rates	PBGA, LQFP
ZL50063	16 K x 16 K	32 In/32 Out	Basic switch supporting 32 Mbps I/O rate	PBGA

ZL50050 SERIES

TDM/TSI SWITCHES

VOICE/DATA



Applications

The ZL50060 is ideal for scalable line card designs used in carrier-class equipment. As shown in the example below, the switching IC accepts 8 Mbps traffic from the T1/E1 mezzanine card providing 8 T1/E1 line service. The traffic is switched between the DSPs and the echo cancellation mezzanine cards (for voice processing) and the backplane.

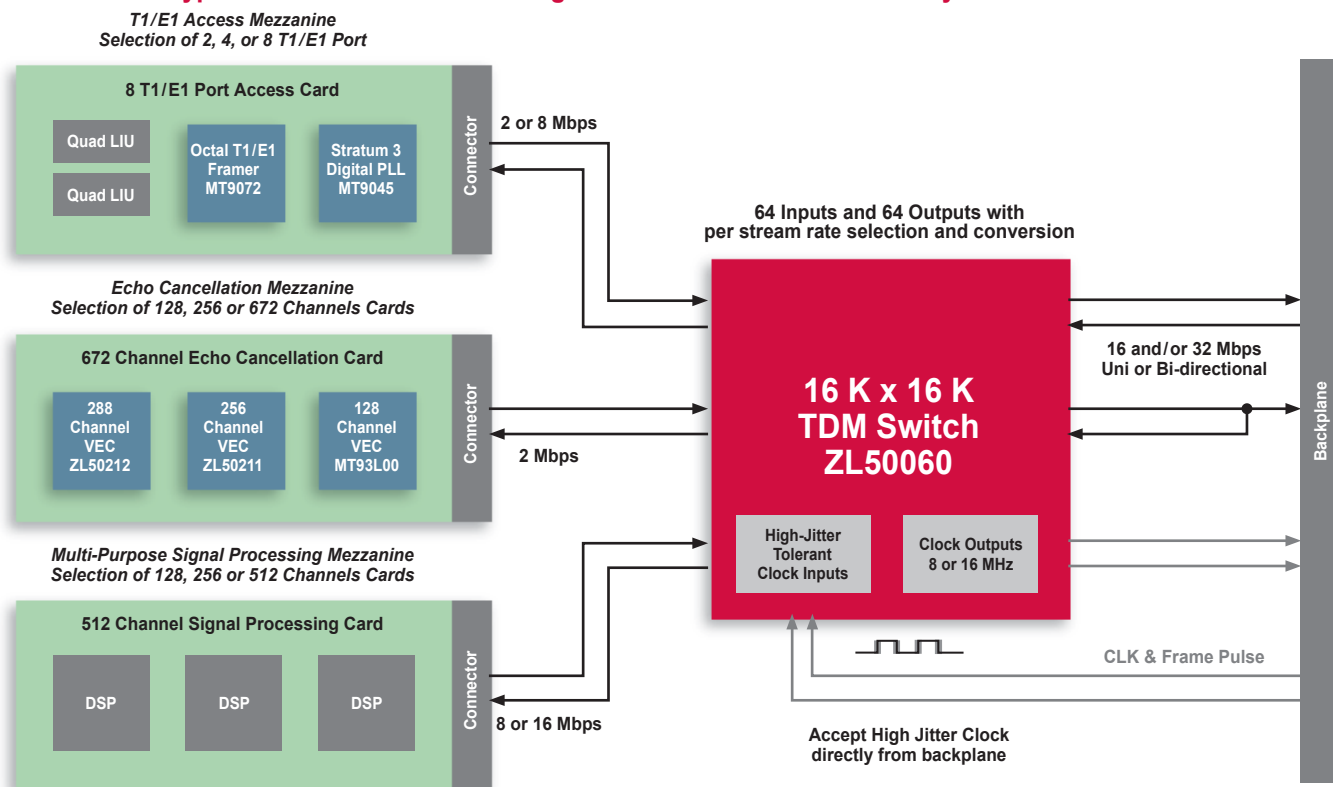
With per-stream rate selection and conversion, the ZL50060 is capable of simultaneously interfacing with the T1/E1 access card running at 8 Mbps, a DSP mezzanine card running at 16 Mbps and an echo cancellation mezzanine card running at 2 Mbps. When a mezzanine card is replaced with a different density card, the data stream rate can simply be re-programmed to the appropriate rate. The ability to support different rates up to 32 Mbps on each input and output stream eliminates the need for external circuitry normally required for rate conversion.

Zarlink's ZL50060 further enhances design flexibility, because it is able to interface with a wide range of timing sources. Featuring exceptional jitter tolerance, the device can be timed directly off the backplane's clock and frame pulse signals or from a low cost digital PLL when reference switching or holdover functionality is required. As a result, designers can use the most cost-effective timing architecture for their application.

This fully featured switching IC also ensures frame integrity, by providing a low latency of 2 frames constant delay between input and output streams. With per-stream Input delay and Output advancement, the device eliminates the need for glue logic that provides external buffer control when required and aligns data streams.

As illustrated, with the industry's widest range of programmable features, the ZL50060 improves flexibility, simplifies design and reduces cost of carrier access equipment.

Typical Carrier Access Switching Line Card with Scalable Density Mezzanine Cards



Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively Zarlink) is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee expressed or implied is made regarding the capability, performance or suitability of any product or service.

ZARLINK, ZL, and the Zarlink logo are trademarks of Zarlink Semiconductor Inc. Copyright 2003, Zarlink Semiconductor Inc. All Rights Reserved.

Publication Number PP5860