PLL
MT90401

The MT90401 is a digital phase locked loop (DPLL) that synchronizes SONET (Synchronous Optical Network) and SDH (synchronous Digital Hierarchy) network equipment. The device uses an integrated approach to ease system design and reduce board space compared to traditional clock design or clock modules.

The MT90401 is compliant to the Telcordia and ITU-T specifications for SONET and SDH systems, ensuring precise system timing at all nodes in the network, even in the presence of disturbances on the incoming synchronization signals.

At a Glance

- Package: 80-pin LQFP
- Volume Production: Now

Applications

- SONET/SDH add/drop Multiplexers
- SONET/SDH Uplinks
- Terminal Multiplexers
- Integrated Access Devices
- ATM Edge Switches

High Performance

- Synchronization reference status indications include primary or secondary reference out of range of +/-12 ppm, and holdover indication for loss of active reference.
- Holdover accuracy of 0.02 ppm ensures synchronization even when the timing source is down.

Flexible for Multiple System Requirements

- Supports free-run, locked or holdover modes.
- Selectable loop filter corner frequency supports SONET or SDH operation with or without microprocessor control.
- OC-3/STM-1, DS3, E3, 19.44MHz, DS2, E1, T1, and TDM bus clock outputs to 16.384MHz.
- Accepts two independent reference inputs selectable to 1.544MHz, 2.048MHz, 19.44MHz, or 8kHz frequencies.
- Output clock supports master-slave arrangements.

Simplifies Design

- Hardware or software control options.
- External 20MHz oscillator operates as the master clock.
- Eliminates requirements for external loop filter components, reducing board space and cost.

Standards Compliant

- Telcordia GR-253-CORE for SONET Stratum 3 and SONET minimum clock.
- Telcordia GR-1244-CORE for Stratum 3 clocks.
- ITU-T G.813 option 1 and option 2 for SDH clocks.

Customer Support

The MT90401 is supported by a customer evaluation board as well as with extended in-house support.

Applications

As shown in the diagram below, the MT90401 can be implemented at every node in the system where transmit data must be synchronized to a master system reference clock.

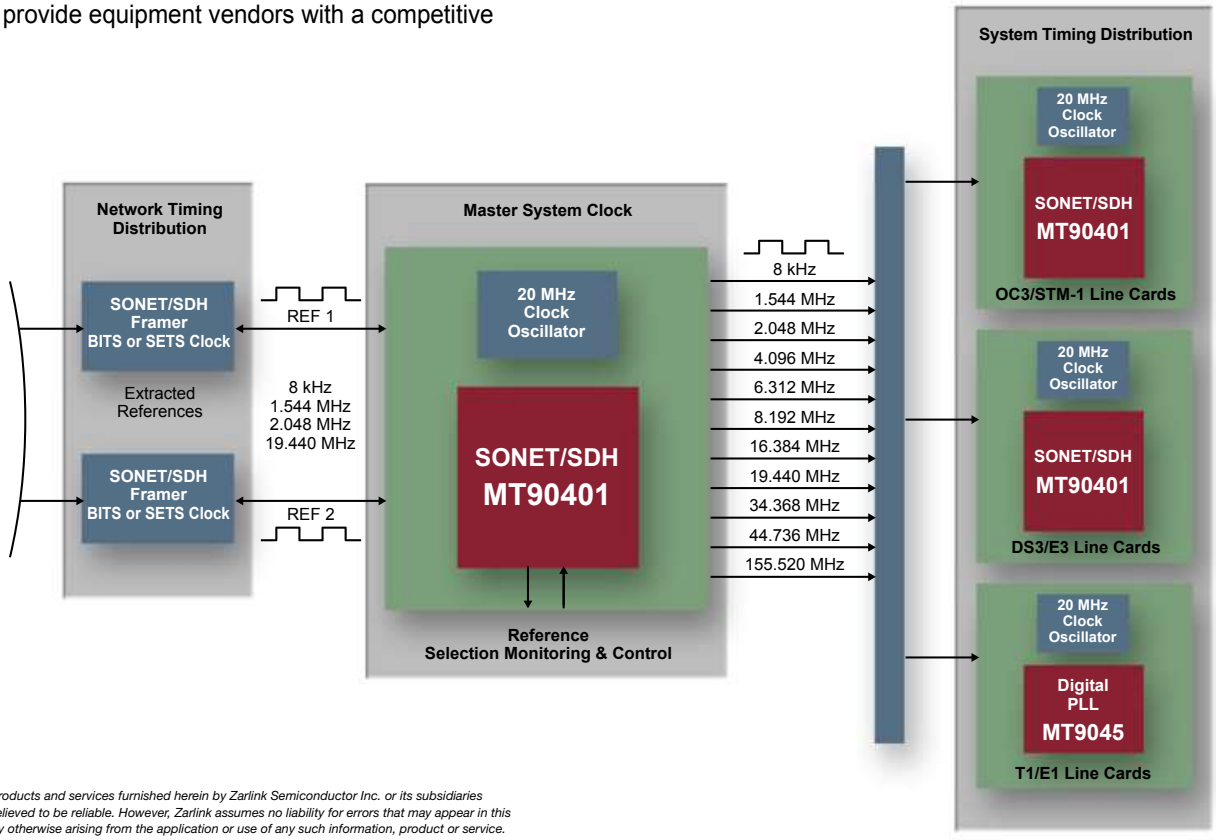
The MT90401 is used extensively in master/slave timing cards to ensure precise synchronization of network equipment to the BITS (in SONET) or SETS (in SDH) clock. With a holdover accuracy of 0.02 ppm the MT90401 allows network equipment to continue to send and receive data even when the source of network synchronization is occasionally interrupted or changed.

The MT90401 is also used extensively on system line cards to improve reliability. The MT90401 is capable of hitless reference switching, changing its source of network synchronization from one interface to another while suppressing undesirable phase transients, enhancing clock quality.

Network synchronization is a complex and necessary function, but does not provide equipment vendors with a competitive advantage. The MT90401 allows our customers to avoid designing their own clocks or using more costly modules, and focus their resources on features that differentiate their products from the competition.

The integrated architecture simplifies system design and reduces board space requirements by up to 80% compared to proprietary clock designs or module based solutions.

Designers can utilize the MT90401 with a high performance oscillator to build a complete SONET or SDH network clock. When used on SONET/SDH line cards, the MT90401 performs most synchronization functions – including hitless reference switching—with an inexpensive 20MHz (megahertz) oscillator as the master clock, avoiding the need for the larger and more costly oscillators required in network clocks.



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