ZL38012
Design Manual

Part Number:	**ZL38012**
Revision Number:	**3.0**
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Microsemi®

ZL38012
Voice Processor with Dual Narrow Band Codecs
Design Manual

November 2012

Ordering Information

ZL38012LDG1	56 Pin QFN*

*Pb Free Matte Tin

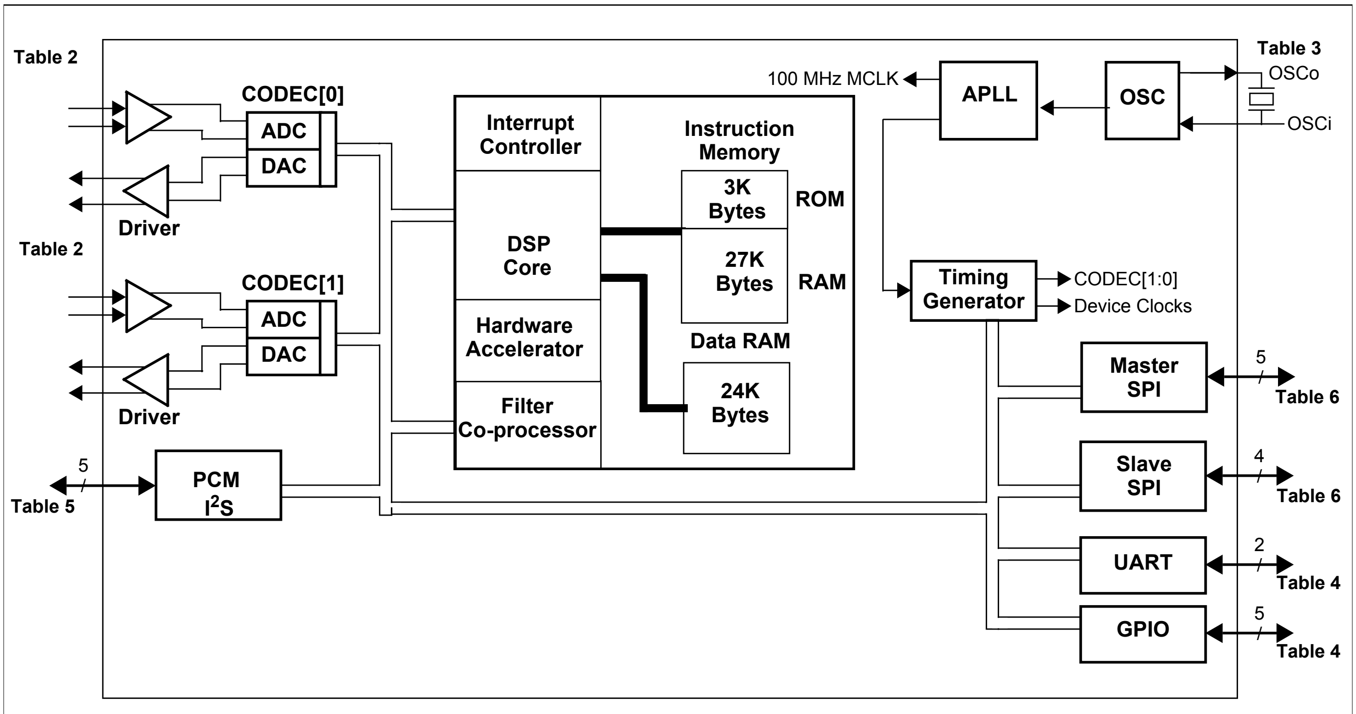
-40°C to +85°C

Features

- 100 MHz (200 MIPs) Microsemi voice processor with hardware accelerator.
- Dual 8 kHz sampling ΔΣ ADCs with input buffer gain selection
- Dual 8 kHz ΔΣ DACs with internal output driver
- Dual function Inter-IC Sound (I^2S) port or TDM Port
- PCM port supports TDM (ST BUS, GCI or McBSP framing) or SSI modes at bit rates of 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 Kb/sec
- Separate slave (microcontroller) and master (Flash) SPI ports, maximum clock rate = 25 MHz
- 5 General Purpose Input/Output (GPIO) pins
- General purpose UART port
- Bootloadable for future Microsemi software upgrades
- External oscillator or crystal/ceramic resonator
- 1.2 V Core; 3.3 V IO with 5 V-tolerant inputs

Applications

- Hands-free car kits
- Full duplex speaker-phone for digital telephone
- Echo cancellation for video conferences
- Intercom Systems
- Security Systems



See Table 7 for Supply and Ground, Table 1 for Reset, and Table 9 for IC and NC pin descriptions.

Figure 1 - Functional Block Diagram

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Change Summary

Changes from March 2011 issue to November 2012 issue. Page, section, figure and table numbers refer to this current issue.

Page	**Item**	**Change**
Multiple	Zarlink logo and name reference	Updated to Microsemi logo and name.

Changes from September 2010 issue to March 2011 issue. Page, section, figure and table numbers refer to this current issue.

Page	**Item**	**Change**
46	“DC Electrical Characteristics“	Removed Theta JA
73	Figure 56	Corrected crystal frequency options
74	Figure 57	Corrected crystal frequency options.

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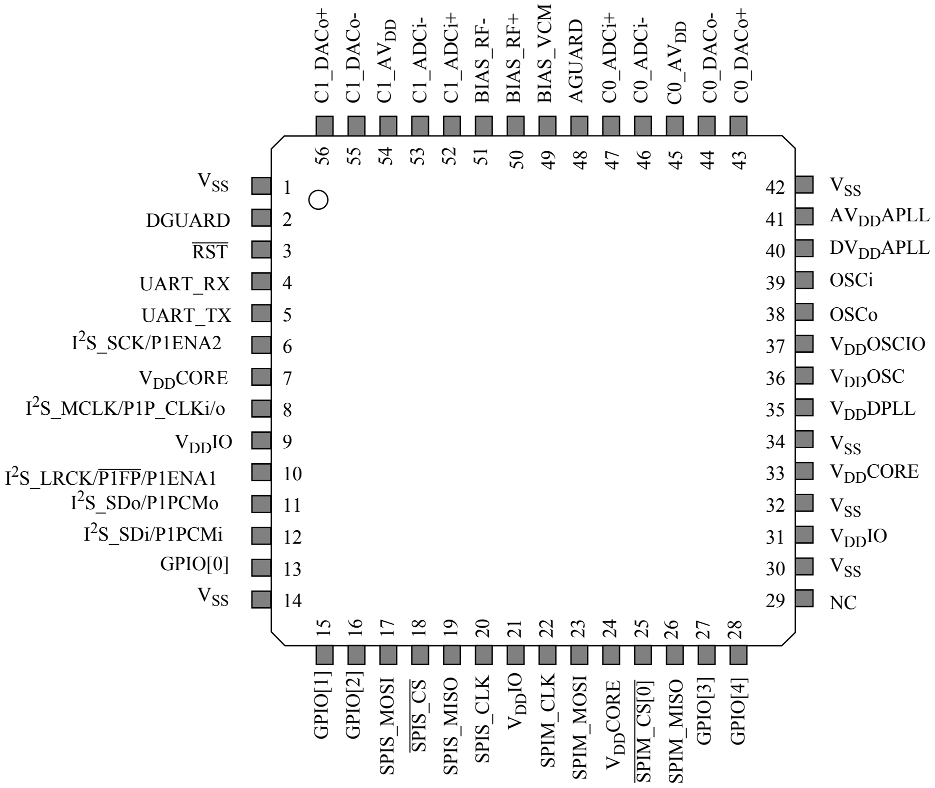


Figure 2 - ZL38012 56-Lead QFN 8 mm x 8 mm, 0.5 mm pitch, JEDEC MO-026 (Top View)

Pin Description

QFN Pin #	Name	Description
3	$\overline{\text{RST}}$	**Reset (Schmitt Trigger Input).** When low this device is in its reset state and all tristate outputs will be in a high impedance state. This input must be high for normal device operation. In order to properly initialize this device during power-on reset this input must be held low for the duration of the core power supply voltage rise to normal operating levels plus 0.5 msec. After the power-on reset this device may be asynchronously reset by making this input low for a minimum of 0.5 msec.

Table 1 - JTAG and Reset Pin Description

QFN Pin #	Name	Description
2	DGUARD	**Digital Guard Ring.** Codec digital substrate isolation. Connect to digital ground.
43	C0_DACo+	**Codec Zero Digital-to-Analog Converter Out Plus (Analog Output).** This is the positive output signal of the differential analog output buffer for DAC zero. The complementary output signal of this differential pair is C0_DACo-. This output should be AC coupled to a maximum load (minimum impedance) of 10 KΩ.
44	C0_DACo-	**Codec Zero Digital-to-Analog Converter Out Minus (Analog Output).** This is the negative output signal of the differential analog output buffer for DAC zero. The complementary output signal of this differential pair is C0_DACo+. This output should be AC coupled to a maximum load (minimum impedance) of 10 KΩ.
46	C0_ADCi-	**Codec Zero Analog-to-Digital Converter In Minus (Analog Input).** This is the negative input signal of the differential analog input buffer for ADC zero. The complementary input signal of this differential pair is C0_ADCi+. This input should be AC coupled. In MIC mode on-chip resistors are used to set the gain of this buffer stage.
47	C0_ADCi+	**Codec Zero Analog-to-Digital Converter In Plus (Analog Input).** This is the positive input signal of the differential analog input buffer for ADC zero. The complementary input signal of this differential pair is C0_ADCi-. This input should be AC coupled. In MIC mode on-chip resistors are used to set the gain of this buffer stage.
48	AGUARD	**Analog Guard Ring.** Codec analog substrate isolation. Connect to analog ground.
49	BIAS_VCM	**Bias Voltage Common Mode (Analog Output).** Common mode bias voltage output signal for the DAC output buffers. This signal is to be decoupled through a 0.1 μF ceramic capacitor to analog ground. This output signal should not be used to bias external circuits. See 8.0, “Applications“ on page 70 of this design manual.
50	BIAS_RF+	**Bias Reference Plus (Analog Output).** Analog-to-digital converter reference voltage. Connect a 0.1 μF ceramic capacitor between this signal and BIAS_RF-. Additionally, this signal may also be decoupled through a 0.1 μF ceramic capacitor to analog ground. See 8.0, “Applications“ on page 70 of this design manual.
51	BIAS_RF-	**Bias Reference Minus (Analog Output).** Analog-to-digital converter reference voltage. Connect a 0.1 μF ceramic capacitor between this signal and BIAS_RF+. Additionally, this signal may also be decoupled through a 0.1 μF ceramic capacitor to analog ground. See 8.0, “Applications“ on page 70 of this design manual.

Table 2 - Codec[1:0] Pin Description

QFN Pin #	Name	Description
52	C1_ADCi+	**Codec One Analog-to-Digital Converter In Plus (Analog Input).** This is the positive input signal of the differential analog input buffer for ADC one. The complementary input signal of this differential pair is C0_ADCi-. This input should be AC coupled. In MIC mode on-chip resistors are used to set the gain of this buffer stage.
53	C1_ADCi-	**Codec One Analog-to-Digital Converter In Minus (Analog Input).** This is the negative input signal of the differential analog input buffer for ADC one. The complementary input signal of this differential pair is C0_ADCi+. This input should be AC coupled. In MIC mode on-chip resistors are used to set the gain of this buffer stage.
55	C1_DACo-	**Codec One Digital-to-Analog Converter Out Minus (Analog Output).** This is the negative output signal of the differential analog output buffer for DAC one. The complementary output signal of this differential pair is C1_DACo+. This output should be AC coupled to a maximum load (minimum impedance) of 10 KΩ.
56	C1_DACo+	**Codec One Digital-to-Analog Converter Out Plus (Analog Output).** This is the positive output signal of the differential analog output buffer for DAC one. The complementary output signal of this differential pair is C1_DACo-. This output should be AC coupled to a maximum load (minimum impedance) of 10 KΩ.

Table 2 - Codec[1:0] Pin Description

QFN Pin #	Name	Description
38	OSCo	**Oscillator Output (Output).** Drive output for an external crystal to form a crystal oscillator circuit with the internal driver. The crystal is to be connected between OSCo and OSCi. This pin should be left open when an external oscillator is used instead of an external crystal. This signal is not tristated by the device $\overline{\text{RST}}$ function. See 8.2.1, “Crystal Oscillator Specification“ on page 73.
39	OSCi	**Oscillator Input (Input).** Input for an external crystal to form a crystal oscillator circuit with the internal driver. The crystal is to be connected between OSCo and OSCi. This pin is the oscillator input when an external 3.3 V +/-10% oscillator is used instead of an external crystal. See 8.2.2, “Clock Oscillator“ on page 74 and 8.2.1, “Crystal Oscillator Specification“ on page 73.

Table 3 - Clock and Oscillator Pin Description

QFN Pin #	Name	Description
4	UART_Rx	**Universal Asynchronous Receiver/Transmitter Receive (Schmitt Trigger Input).** Receive serial data in. In slave mode this port (UART_Tx/Rx) functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device. The MiniCore3 may use this port in master mode to access external peripherals.
5	UART_Tx	**Universal Asynchronous Receiver/Transmitter Transmit (Tristate Output).** Transmit serial data out. In slave mode this port (UART_Tx/Rx) functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device. The MiniCore3 may use this port in master mode to access external peripherals.
13, 15, 16, 27, 28	GPIO[0:4]	**General Purpose I/O Zero (Input Internal Pull-Down/Tristate Output).** This pin can be configured as an input or output and is intended for low-frequency signalling. GPIO [1:4] must be pulled low on power up.

Table 4 - UART and GPIO Pin Description

QFN Pin #	Name	Description
6	I^2S_SCK/ P1ENA2	**Inter-IC Sound Port Serial Clock (Schmitt Trigger Input/Tristate Output).** This is the I^2S port bit clock and operates at selectable rates of 256, 512, 1024, 1411.2 and 1536 kHz, which is 32 x f_S (sampling frequency) of the peripheral converter. In I^2S port master mode this clock is an output and drives the bit clock input of slave mode peripheral converters. In I^2S port slave mode this clock is an input and is driven from a converter operating in master mode. After power-up this signal is in I^2S slave mode, an input. **Port One SSI Enable Strobe Two (Input/Tristate Output).** This is an 8/16 kHz 8/16-bit wide enable strobe that operates in SSI mode only. This signal is an enable strobe input for applications where the Port 1 PCM Bus interface must be frame aligned to an external frame signal (slave mode). In master mode this signal is an enable strobe output. The default state of this signal is input after power up reset.
8	I^2S_MCLK/ P1P_CLKi/o	**Inter-IC Sound Port Master Clock (Schmitt Trigger Input/Tristate Output).** For I^2S port master mode operation this is the master clock output for external codec or ADC's MCLK input. I^2S_MCLK clock rates are selectable to be 2.048, 4.096, 8.192, 11.2896 and 12.288 MHz, which is 256 x f_S (sampling frequency) of the peripheral converter. When the I^2S port is in slave mode, this signal is in a high impedance state. **Port One PCM Clock Input/Output.** When secondary TDM operation is selected this clock operates at 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 kHz and will be either equal or twice the data rate of signals SPCMi/o. In TDM master mode this clock is an output and in TDM slave mode this clock is an input.
10	I^2S_LRCK/ $\overline{\text{P1FP}}$/ P1ENA1	**Inter-IC Sound Port Left/Right Clock (Input/Tristate Output**). This is the I^2S port left or right word select clock and operates at selectable rates of 8, 16, 32, 44.1 and 48 kHz, which is equal to the f_S (sampling frequency) of the peripheral converter. In I^2S port master mode this clock is an output and drives the left/right clock input of slave mode peripheral converters. In I^2S port slave mode this clock is an input and is driven from a converter operating in master mode. After power-up this signal is in I^2S slave mode, an input. **Port One PCM Bus Frame Pulse/Port One Enable Strobe One.** This is an 8/16 kHz TDM frame alignment reference signal in TDM (ST BUS, GCI or McBSP framing) and in SSI modes. In SSI mode this signal is a 8/16 bit wide enable strobe. This signal may be used as a PCM frame reference input for applications where the PCM bus interface must be frame aligned to an external frame signal (slave mode). In master mode this signal is a frame pulse output. The default state of this signal is input after power up reset.
11	I^2S_SDo P1PCMo	**Inter-IC Sound Port Serial Data Output (Tristate Output).** This is the I^2S port data input signal when the port is in master mode and configured to work with two ADC's. This is the I^2S port data output signal when the port is in master mode and configured to work with a single codec. **Port One PCM Serial Stream Output.** This serial data stream operates in either TDM (ST BUS, GCI or McBSP framing) or SSI modes at data rates of 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 Kb/s. Each 8 kHz frame supports 16, 32, 64, 128, 256, 512, 1024 or 2048 channels of 8 bits or half as many 16 bit channels. Two 8 or 16 bit channels may be processed per frame.

QFN Pin #	Name	Description
12	I^2S_SDi/ P1PCMi	**Inter-IC Sound Port Serial Data Input (Input).** This is the I^2S port serial data input. **Port One PCM Serial Stream Input (Input).** This serial data stream operates in either TDM (ST BUS, GCI or McBSP framing) or SSI modes at data rates of 128, 256, 512, 1024, 2048, 4096, 8192 or 16384 Kb/s. Each 8 kHz frame supports 16, 32, 64, 128, 256, 512, 1024 or 2048 channels of 8 bits or half as many 16 bit channels. Two 8 or 16 bit channels may be processed per frame.

Table 5 - Inter-IC Sound and PCM Port One Pin Description

QFN Pin #	Name	Description
17	SPIS_MOSI	**Serial Peripheral Interface Slave Port Data Input (Input).** Data input signal for the Slave SPI port.
18	$\overline{\mathrm{SPIS\_CS}}$	**Serial Peripheral Interface Slave Chip Select (Input).** This active low chip select signal activates the Slave SPI port. This port functions as a peripheral interface for an external controller and supports access to the internal registers and memory of the device.
19	SPIS_MISO	**Serial Peripheral Interface Slave Port Data Output (Tristate Output).** Data output signal for the Slave SPI port.
20	SPIS_CLK	**Serial Peripheral Interface Slave Port Clock (Schmitt Trigger Input).** Clock input for the Slave SPI port. Maximum frequency = 25 MHz.
22	SPIM_CLK	**Serial Peripheral Interface Master Port Clock (Tristate Output).** Clock output for the Master SPI port. Maximum frequency = 25 MHz.
23	SPIM_MOSI	**Serial Peripheral Interface Master Port Data Input (Tristate Output).** Data output signal for the Master SPI port.
25	$\overline{\mathrm{SPIM\_CS[0]}}$	**Serial Peripheral Interface Master Port Select Zero (Tristate Output).** This active low chip select is normally used to access an external peripheral such as FLASH memory.
26	SPIM_MISO	**Serial Peripheral Interface Master Port Data Output (Input).** Data input signal for the master SPI port.

Table 6 - Master and Slave SPI Port Pin Descriptions

QFN Pin #	Name	Description
1, 14, 30, 32, 34, 42	V_{SS}	**Core Ground.** Connect to digital ground.
7, 24, 33	V_{DD}CORE	**Core Supply.** Connect to +1.2 V ±5% core supply.

Table 7 - Supply and Ground Pin Description

QFN Pin #	Name	Description
9, 21, 31	V_{DD}IO	**I/O Supply.** Connect to +3.3 V ±10% supply for Input/Output drivers.
35	V_{DD}DPLL	**Digital PLL Supply.** Connect to +1.2 V ±5% DPLL supply.
36	V_{DD}OSC	**Oscillator Supply.** Connect to +1.2 V ±5% oscillator supply.
37	V_{DD}OSCIO	**Oscillator I/O Supply.** Connect to +3.3 V ±10% supply for oscillator Input/Output drivers.
40	DV$_{DD}$APLL	**Analog PLL Digital Supply.** Connect to +1.2 V ±5% APLL digital supply.
41	AV$_{DD}$APLL	**Analog PLL Analog Supply.** Connect to +1.2 V ±5% APLL analog supply.
45	C0_AV$_{DD}$	**Codec Zero Analog Supply.** Connect to +1.2 V ±5% voice codec [0] analog supply.
54	C1_AV$_{DD}$	**Codec One Analog Supply.** Connect to +1.2 V ±5% voice codec [1] analog supply.
29	NC	**No Connection.** These pins are to be left unconnected.

Table 7 - Supply and Ground Pin Description

1.0 Functional Description

The ZL38012 is a hardware platform designed to support advanced acoustic echo canceller (with noise reduction) firmware applications available from Microsemi. These applications are resident in external memory and are downloaded by the ZL38012 resident boot code during initialization.

The firmware products and manuals available at the release of this data sheet are: ZLS385xx: Acoustic Echo Canceller with Noise Reduction for Hands-Free Car Kits. If these applications do not meet your requirements, please contact your local Microsemi CMPG Sales Office for the latest firmware releases.

The ZL38012 Advanced Acoustic Echo Canceller with Noise Reduction platform integrates Microsemi’s Voice Processor (ZVP) DSP Core with a number of internal peripherals. These peripherals include the following:

- Two independent ΔΣ CODECs
- PCM ports - ST BUS, GCI, McBSP or SSI operation/^{2}S interface port
- A 2048 tap Filter Co-processor (LMS, FIR and FAP realizations)
- Two Auxiliary Timers and a Watchdog Timer
- 5 GPIO pins
- A UART interface
- A Slave SPI port and a Master SPI port
- A timing block that supports master and slave operation
- An IEEE - 1149.1 compatible JTAG port

The DSP Core can process up to two 8-bit audio channels or two 16-bit audio channels. These audio channels may originate and terminate with the ΣΔ CODECs, or be communicated to and from the DSP Core through the PCM/ the I^{2}S port.

2.0 Core DSP Functional Block

The ZL38012 DSP Core functional block, illustrated in Figure 1, is made up of a DSP Core, Interrupt Controller, Data RAM, Instruction RAM, BOOT ROM and a ButterFly Hardware Accelerator. This block controls the timing (APLL and Timing Generator), peripheral interfaces and Filter Co-processor through a peripheral address/data/control bus.

The ZL38012 implementation of DSP core and Filter Co-processor have been optimized to efficiently support voice processing applications. These applications are described in detail in the Firmware Manuals associated with this hardware platform.

2.1 DSP

The Core DSP is a 100 MIPS processor realized with two internal memory busses (Harvard architecture) to allow multiple accesses during the same instruction cycle. Instruction memory space consists of a 1 k x 24 bit Boot ROM (3 k bytes) and 8 k x 24 bits of RAM (24 k bytes). Data memory space consists of 1 k x 32 bits of register space (16 k bytes), plus 2 k x 16 bits and 2 k x 24 bits of RAM (26 k bytes) dedicated for the filter co processor that can be reused for different applications. Data memory RAM is 16/32 bit addressable.

The Filter Co-Processor is used by the application firmware to realize the LMS filters up to a maximum of 2048 coefficients (taps).

3.0 Codec[1:0]

The ZL38012 has two 16-bit fully differential ΔΣ CODECs (CODEC 0/1) that meet G.712 requirements at 8 kHz sampling, see Figure 3. The ADC path consists of input signal pins C0/1_ADCi+ and C0/1_ADCi- which feed selectable Microphone Amplifier. Once past the buffer the analog signal goes through a low pass antialiasing filter and to a 4th order feed-forward ΔΣ Modulator that produces a Pulse Density Modulated (PDM) signal. Next the PDM signal goes through a Low Pass Decimation Filter and then is converted into a 16-bit parallel word that can be read by the ZL38012 DSP (ADCout[15:0], Figure 3).

The ZL38012 DSP will send 16-bit parallel word samples (DACin[15:0], Figure 3) to the DAC where they are converted to serial data and passed through an interpolation filter followed by a digital ΔΣ Modulator. The ΔΣ Modulator generates PDM data, which then passes through a 32-tap FIR reconstruction filter. The reconstructed analog signal is then passed to a unity voltage gain differential output driver and to pins C0/1_DACo+ and C0/1_DACo-.

The CODEC bias voltages are generated by an internal bandgap circuit (BIAS_VCM, BIAS_RF+ and BIAS_RF-). See 8.0, “Applications“ on page 70 of this design manual for external circuit requirements.

Each ZL38012 CODEC has two loopbacks, see Firmware Manual. When activated, the input analog signal on pins C0/1_ADC+/- is looped around to C0/1_DAC+/-. Pulse Density Modulated (PDM) serial data from the ADC Analog ΔΣ Modulator output is looped around to the input of the DAC Reconstruction Filter. At the same time 16-bit parallel data is looped around from DACin[15:0] to ADCout[15:0]. PDM serial data from the DAC Digital ΔΣ Modulator is looped around to the input of the ADC Digital Low Pass Decimation Filter.

When the Parallel Loopback is activated the input analog signal on pins C0/1_ADC+/- is looped around to the C0/1_DAC+/- output. 16-bit parallel data from the ADC Digital Low Pass Decimation Filter is looped around to the DAC Digital Low Pass Interpolation Filter. This data may be read by the DSP, but parallel data written to the DAC by the DSP will be lost.

CODEC0 and CODCE1 of the ZL38012 may be powered down if they are not required. See Firmware Manual.

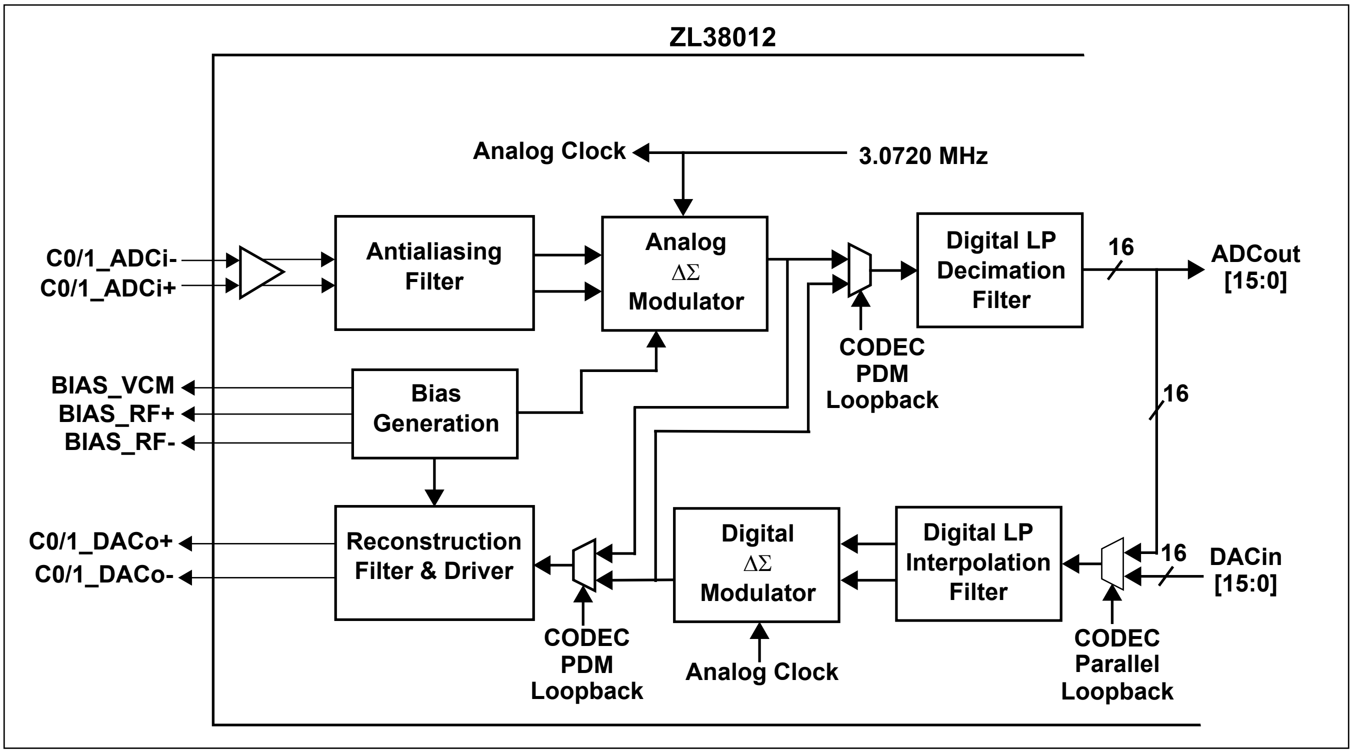
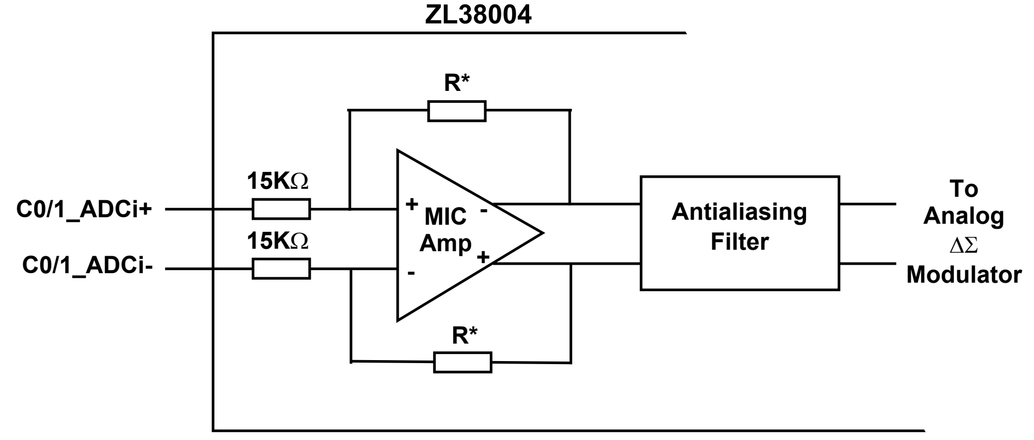


Figure 3 - CODEC Block Diagram

3.1 Input Buffer

The internal differential input buffer of the ZL38004 CODECs is configured with a Microphone Amplifier interface with internal gain. The internal feedback resister (R) is programmable for gain settings of 0, 6.02, 12.04, 18.06, 24.08 and 30.10 dB for an input maximum differential voltage of 800 to 25 mVppd. Full scale ADC input voltage is 800 mVppd (9 dBm0), which represents full scale 2s complement codes of ±32767. In this application C0/1_BFo+/- outputs should be left open and C0/1_ADCi+/- are to be capacitively coupled.



* Internal gain is set through the Microphone Gain Register - see firmware manual.

Figure 4 - CODEC 0/1 ADC Microphone Amplifier Selected

3.2 Reconstruction Filter and Driver (DAC Output)

The full scale DAC output voltage is 1200 mVppd (9 dBm0), which represents full scale 2s complement codes of ±32767 when driving a minimum load of 10 KΩ. See section 8.0, “Applications“ on page 70 of this design manual for details.

The DAC reconstruction filter reduces the out of band noise at the DAC output caused by the DAC delta-sigma modulator. The modulator contributes very little noise up to 30 kHz. However, even with the reconstuction filter, the DAC output will look noisy when view on an oscilloscope due to residual out of band modulator noise. At 1 MHz, the noise contained within a 300 Hz band is less than -40 dBm0.

4.0 PCM Port

4.1 PCM Port

The PCM port support data communication between an external peripheral device and the ZL38012 DSP Core using separate input (PCMi) and output (PCMo) serial streams with TDM (i.e., ST-BUS, GCI or McBSP) or SSI interface timing. Access to the control and status registers associated with these ports is through the Slave SPI port (Pin Description Table 6) or UART (Pin Description Table 4). The PCM Port pin functions are described in Table 5. These port signals are either in their input or high impedance states after a power-on reset and outputs signals PCMo may be put in a high impedance state at any time during normal operation. Refer to the associated Firmware Manual for PCM port control, status and mode selection.

Figure 5 illustrates the signals associated with the Master and Slave timing modes of operation for PCM Port. Insert A: PCM port Master TDM (Mode 0), shows data clock (PCM_CLKo) and frame pulse ($\overline{\text{PCMFP}}$) as outputs derived from the ZL38012 internal PLL. PCM_CLKo clocks data into the ZL38012 on PCMCMi and out of the ZL38012 on PCMo, and $\overline{\text{PCMFP}}$ delineates the 8 kHz frame boundaries for these signals. Insert B: PCM Master SSI (Mode3), functions the same way as the TDM Master except that selected channels are defined by enable outputs P0ENA1 and P0ENA2.

With slave operation the source of timing is not the ZL38012, so PCM_CLKi is the input clock and $\overline{\text{PCMFP}}$ is the 8 kHz input frame pulse. This is illustrated by Figure 5 C: PCM Port Slave TDM (Modes 1 & 2) and D: PCM Port Slave SSI (Modes 4, 5 & 6). See 4.2, “PCM Port Modes of Operation“ for port mode descriptions.

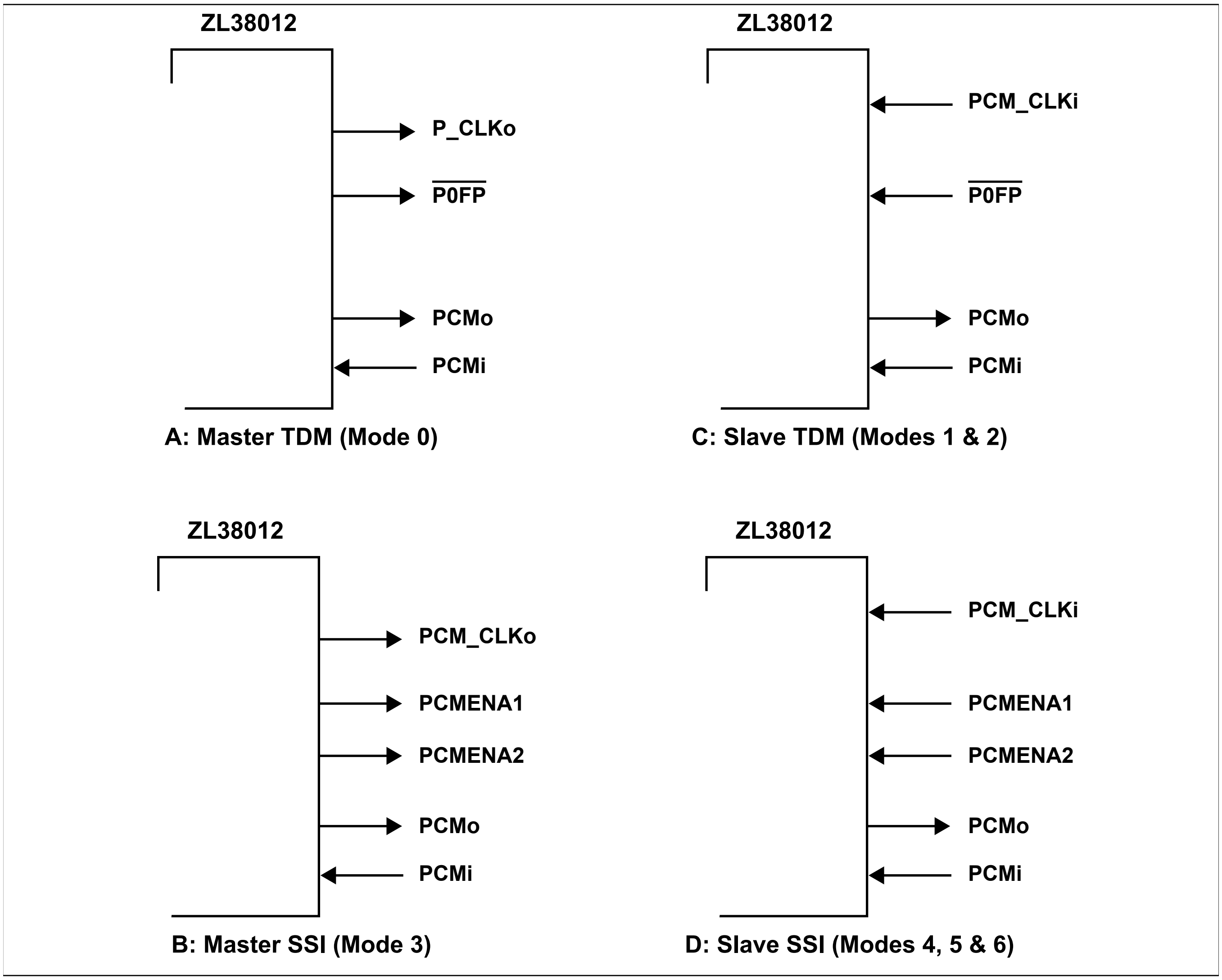


Figure 5 - PCM Port Signal Configurations for Master/Slave Operation

The ZL38012 will process audio channels of up to 16 bits in length. Audio channel sizes are designated as either 8-bit (Short) or 16-bit (Long) on the PCM interfaces. With TDM operation each audio channel is mapped on to one or more 8-bit time slots that are defined by the associated frame alignment signal. Each PCM port (0 & 1) supports from 1 to 4 Short Channels; 1 or 2 Short Channels and 1 Long (16-bit) Channel; or 2 Long Channels. Audio channels are defined as First and Second Long, and First, Second, Third and Fourth Short, see the Firmware Manual for assignment details. These channels may be assigned to different time slots on the input and output streams.

In SSI mode each PCM port supports 1 or 2 Short or Long channels, which are defined on PCMi/0 by the position and length of enable signals P0ENA1 and P0ENA2. Audio channels are defined as First and Second Long, and First and Third Short, see the Firmware Manual for assignment details. Channel positions and length are common to input and output signals.

The data clock rate (PCM_CLKi) of the PCM interface may be selected to be either true and inverted polarity, see Figure 6. The frame rate is 8 kHz.

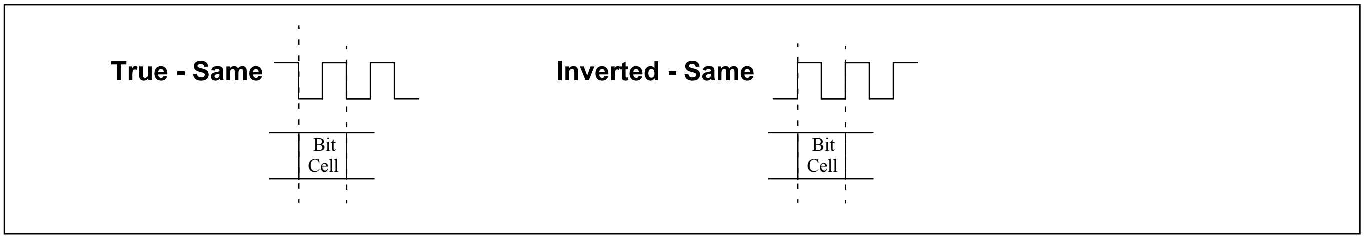


Figure 6 - Clock Polarity versus Data Rate

Audio channel data clocked in on PCMi may be sampled at either the 1/2 or 2/2 bit positions.

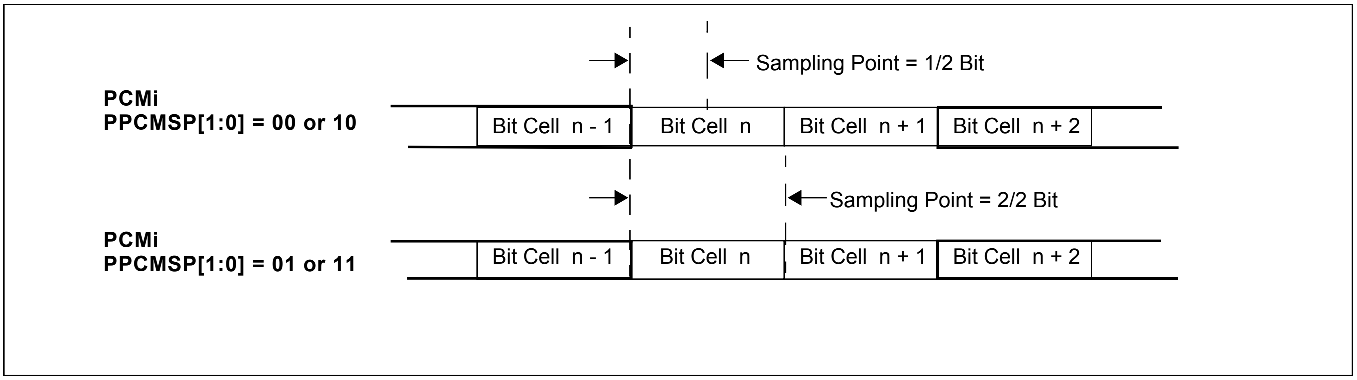


Figure 7 - PCM Serial Data Input Sampling Points

The PCM Ports support two loopbacks, which function in both TDM and SSI modes of operation. That is, a PCM Port Loopack that loops the assigned input audio channels on PCMi to the assigned output audio channels on PCMo, see Figure 8. Throughput delay for specific audio channel bits from PCMi to PCMo is two frames when the data clock rate is twice the data rate and the number of clock cycles/frame ≥ 42 or when the clock rate is the same as the data rate and the number of clock cycles/frame ≥ 21, otherwise throughput delay is three frames. Audio channel data is also passed to the DSP Core input. The DSP Loopback loops the audio channel data output from the DSP Core to the DSP Core input. Audio channel data is also passed to the PCMo output.

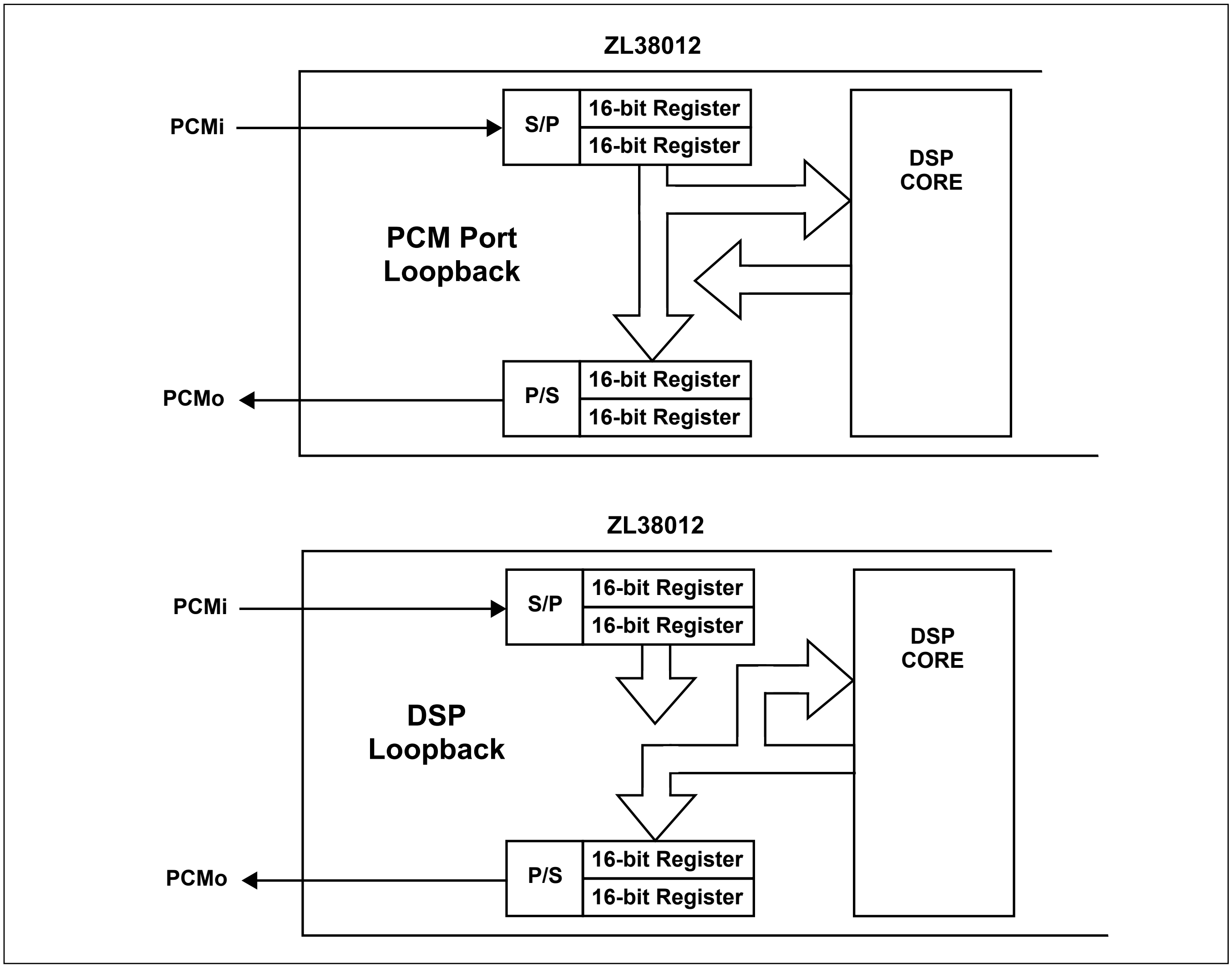


Figure 8 - PCM and DSP Loopbacks

The bit sequence used for 8 and 16-bit audio channels may be reversed (swapped) between the PCM inputs/outputs and the DSP Core. Table 8 shows that when bit swapping is activated and b_{15}/b_7 is the bit transmitted first (MSB) on PCMi/o, the DSP Core will process audio channels as if b_0 is the Most Significant Bit (MSB).

Bit Swapping	Audio Channel Length (bits)	PCMi/o Transmission (First Last)	DSP Core Processing (MSB LSB)
De-activated	8	$b_7b_6b_5b_4b_3b_2b_1b_0$	$b_7b_6b_5b_4b_3b_2b_1b_0$
	16	$b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$	$b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$
Activated	8	$b_7b_6b_5b_4b_3b_2b_1b_0$	$b_0b_1b_2b_3b_4b_5b_6b_7$
	16	$b_{15}b_{14}b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$	$b_0b_1b_2b_3b_4b_5b_6b_7b_8b_9b_{10}b_{11}b_{12}b_{13}b_{14}b_{15}$

Table 8 - PCM Port Bit Swapping

4.2 PCM Port Modes of Operation

PCM ports 0 and 1 can function in any of seven operational modes numbered 0 to 6. These modes may be grouped into modes with pre-defined time slots (Modes 0, 1, 3 & 4), modes with flexible timing (Modes 2 & 5) and an automatic rate detection mode (Mode 6).

The modes with pre-defined time slots are TDM Master (0), TDM Slave (1), SSI Master (3) and SSI Slave (4), where Master/Slave refers to timing. The data rates, frame rates, bits/frame and 8-bit time slot numbering (TDM modes only) for these modes are listed in Table 9. In the TDM modes each short channel must be assigned to one of these unassigned 8-bit time slots. Each long channel must be assigned to two 8-bit unassigned contiguous time slots in SSI modes, or two 8-bit unassigned contiguous or non-contiguous time slots that do not straddle the physical frame boundaries defined by the frame pulse alignment signals $\overline{\text{PCMFP}}$ in TDM modes.

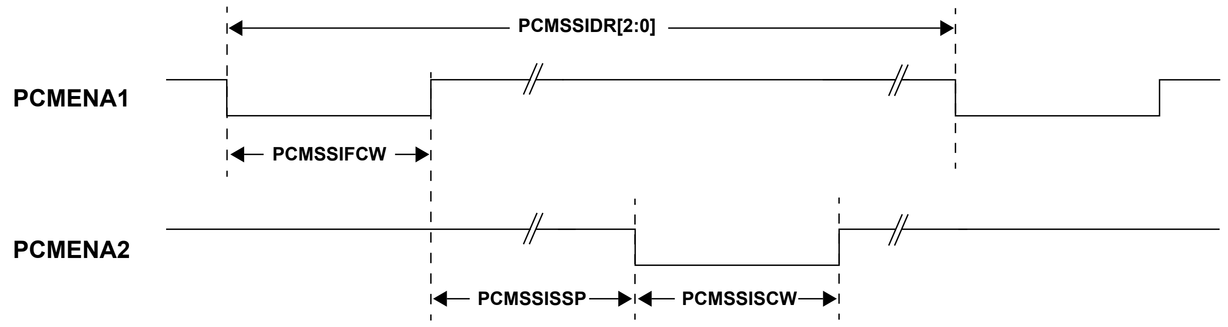
Data Rate (kb/sec)	8-Bit Time Slot Numbering (Bits/frame)
	$\overline{\text{PCMFP}}$ or PCMENA1/2 = 8 kHz
128	0 - 1 (16)
256	0 - 3 (32)
512	0 - 7 (64)
1024	0 - 15 (128)
2048	0 - 31 (256)
4096	0 - 63 (512)
8192	0 - 127 (1024)
16384	0 - 255 (2048)

Table 9 - Stream Data Rates and Associated 8-Bit Time Slot Numbering

Mode 2 is defined as TDM Slave operation with Flexible Clocks and mode 5 is SSI Slave operation with Flexible Clocks. In these modes the number of bits in an 8 kHz frame is programmable. When the data rate is the same as the clock rate on inputs PCM_CLKi the number of clock/cycles per frame can be any number between 8 to 2047 inclusive. The number of clock/cycles per frame can be any even number between 16 and 2046 when the data rate is half the clock rate.

With mode 6, SSI Slave with Automatic Rate Detection, the clock rate must be programmed to be equal to the data rate. Other options that must be programmed are clock polarity, enable signal polarity and the input bit sampling points on PCMi. The ZL38012 will automatically detect the number of clock cycles between consecutive active states of PCMENA1, the width of the active state of ENA1 to be either 8 or 16 bits, the width of the active state of PCMENA2 to be either 8 or 16 bits, and the number of bits between the end of the active state of PCMENA1 and the beginning of the active state of PCMENA2. This is illustrated by Figure 10. These variables are reported in the SSI Status registers for verification purposes and do not need to be written to other registers for normal mode 6 operation.

In SSI mode applications PCMENA1 must always be used. If two audio channels are to be processed, then PCMENA1 and PCMENA2 will both be used.



PCM Port and 1 SSI Status Register

PCMSSIDR[2:0] - SSI Data Rate - number of bits between consecutive active states of PCMENA1

PCMSSIFCW - SSI First Channel Width - 1 for 16 bits; 0 for 8 bits

PCMSSISSP - SSI Second Strobe Position - indicates the distance between PCMENA1 and PCMENA2 in 8 bit increments (0 - 512)

PCMSSISCW - SSI Second Channel Width - 1 for 16 bits; 0 for 8 bits

Figure 10 - Mode 6 - SSI Slave with Automatic Rate Detection

Table 10 shows the Control bit states that select each of the PCM modes. Refer to the Firmware Manual for programming specifics.

Mode	PCM Port Timing Mode Description	PCM Port Control Register			
		Mstr/$\overline{\text{Slv}}$	SSI Md	SSI Reg	Flx Clk
0	TDM Master	1	0	X	0
1	TDM Slave	0	0	X	0
2	TDM Slave with Flexible Clocks - see Table 13 to select number of clock cycles per frame.	0	0	X	1
3	SSI Master	1	1	1	0
4	SSI Slave - see Table 15 for bits/frame	0	1	1	0
5	SSI Slave with Flexible Clocks - see Table 13 to select number of clock cycles per frame.	0	1	1	1
6	SSI Slave with Automatic Rate Detection - see Table 16 for expected bits/frame.	0	1	0	0
Not recommended; not considered normal operation.		Remaining bit combinations			

Table 10 - PCM Port Mode Description

It should be noted that the control bit PPCMRst (PCM Reset) should be programmed from low to high as the last register write when any of the control bits associated with the respective PCM ports is changed. See Firmware Manual for more details.

Mode 0 (TDM Master) - in this mode $\overline{\text{PCMFP}}$ and PCM_CLKo are output signals sourced from the ZL38012 internal timing block. They provide TDM frame, bit alignment and clocking for the time slots of signals PCMPCMi/o. PCMENA2 are in a high impedance state.

In this mode the PCM Port Control Register bits PPCMDR[2:0] is used to establish the PCM data rates of PCMi/o, frame pulse rate of $\overline{\text{PCMFP}}$ and clock rate of PCM_CLKo. See Table 11 below.

Port PCM Control Register - Firmware Manual		
PPCMDR [2:0]	**Number of bits/frame**	**PCM_CLKo Clock Rates**
000	16*	128
001	32	256
010	64	512
011	128	1024
100	256	2048
101	512	4096
110	1024	8192
111	2048	16384

Table 11 - PCM Timing Mode 0 Output Clock and Data Rate Selection

* It should be noted that when 8 bits/frame operation is selected only one short virtual channel can enabled; when 16 bits/frame operation is selected only two short or one long virtual channel can be enabled.

Mode 1 (TDM Slave) - in this mode $\overline{\text{PCMFP}}$ is an input, one of the PCM_CLKi inputs is used as a clock signal (see Pin Description Table 3), and PCMi/o transports PCM data. PCMENA2 and PCM_CLKo are in a high impedance state. The functional relationship between control bits PCMDR[2:0] and clock signals PCM_CLKi are shown in Table 12. The frame pulse input must be 8 kHz.

Port PCM Control Register - Firmware Manual		
PPCMDR [2:0]	**Number of bits/frame**	**PCM_CLKi Clock Rates**
000	16*	NA
001	32	NA
010	64	NA
011	128	NA
100	256	2048
101	512	4096
110	1024	8192
111	2048	16384

Table 12 - PCM Timing Mode 1 Required Clock Rates for Port Inputs

* It should be noted that when 8 bits/frame operation is selected only one short virtual channel can enabled; when 16 bits/frame operation is selected only two short or one long virtual channel can be enabled.

Mode 2 (TDM Slave with Flexible Clocks) - in this mode $\overline{\text{PCMFP}}$ in an input, one of the or PCM_CLKi inputs is used as a clock signal, and PPCMi/o transports PCM data. PENA2 and PPCM_CLKo are in a high impedance state.

In this mode Port PCM Control Register bits PPCMDR[2:0] have no function. PCMi/o data rates are determined from the CCPF[10:0] control bits, the frame signal input $\overline{\text{PCMFP}}$ and input clocks PCM_LBi or PCM_CLKi. See Table 13 below.

The CCPF[10:0] can be any number from 8 to 2047 (00000008_H to $000007FF_H$), see Table 13.

CCPF[10:0] (Clock Cycles/ Frame)	(Mode 2) Input Signal $\overline{\text{PCMFP}}$ = 8 kHz/ (Mode 5) Input Signal PCMENA1/2 = 8 kHz		
	PCMi/o (Kb/sec)	PCM_LBi (kHz)	PCM_CLKi (kHz)
8	64	64	NA
9	72	72	NA
10	80	80	NA
. . .	. . .	. . .	. . .
127	1016	1016	NA
128	1024	1024	1024
129	1032	1032	NA
. . .	. . .	. . .	. . .
255	2040	2040	NA
256	2048	2048	2048
257	2056	2056	NA
. . .	. . .	. . .	. . .
511	4088	4088	NA
512	4096	4096	4096
513	4104	4104	NA
. . .	. . .	. . .	. . .
1023	8184	8184	NA
1024	8192	8192	8192
1025	8200	8200	NA
. . .	. . .	. . .	. . .
2046	16368	16368	NA
2047	16376	16376	NA

Table 13 - PCM Timing Mode 2, Required Frame Signal and Clock Rates for Clock = Data Rates

Mode 3 (SSI Master) - in this mode PCMENA1/2 and PCM_CLKo are output signals sourced from the ZL38012 internal timing block and PCMi/o transport PCM data, see Table 14. PCMENA1 and PCMENA2 are enable outputs that determine the positions of either 8 or 16 bit audio channels in the PCMi/o streams, see Firmware Manual for programming.

PCM port Control Register - Firmware Manual		
PPCMDR [2:0]	**Number of bits/frame**	**PCM_CLKo Clock Rates (kHz)**
000	16*	128
001	32	256
010	64	512
011	128	1024
100	256	2048
101	512	4096
110	1024	8192
111	2048	16384

Table 14 - PCM Timing Mode 3 Output Clock and Data Rate Selection

* It should be noted that when 8 bits/frame operation is selected only one short virtual channel can enabled; when 16 bits/frame operation is selected only two short or one long virtual channel can be enabled.

Mode 4 (SSI Slave) - in this mode PCMENA1/2 are inputs, one of the PCM_CLKi inputs for PCM Port are used as clock signals (see Pin Description table), and PCMi/o transport PCM data. PCM_CLKo is in a high impedance state. The frame pulse input is 8 kHz.

PCM Port Control Register - Firmware Manual		
PPCMDR [2:0]	**Number of bits/frame**	**PCM Port Clocks**
		PCM_CLKi (kHz)
000	16*	NA
001	32	NA
010	64	NA
011	128	NA
100	256	2048
101	512	4096
110	1024	8192
111	2048	16384

Table 15 - PCM Timing Mode 4 Required Clock Rates for PCM Port Inputs

* It should be noted that when 8 bits/frame operation is selected only one short virtual channel can enabled; when 16 bits/frame operation is selected only two short or one long virtual channel can be enabled.

In this mode the SSIDR[2:0] bits of the SSI Status Register (See Firmware Manual) can be used to monitor the number of bits per frame with 8 kHz strobe signals.

Mode 5 (SSI Slave with Flexible Clocks) - in this mode PCMENA1/2 are inputs, one of the or PCM_CLKi inputs for PCM Port are used as clock signals (see Pin Description table), and PCMi/o transport PCM data. PPCM_CLKo is in a high impedance state.

In this mode PCM Port Control Register bits PPCMDR[2:0] have no function. PCMi/o data rates are determined from the CCPF[10:0] control bits (see Firmware Manual), the frame signal input ENA1, and input clocks PCM_LBi and PCM_CLKi. The PCMENA2 strobe input is used to delineate the second SSI short or long audio channel on PCMi/o. See Table 13.

Mode 6 (SSI Slave with Automatic Rate Detection) - in this mode PCMENA1/2 are inputs, one of the or PCM_CLKi inputs for PCM Port is used as a clock signal (see Pin Description table), and PCMi/o transports PCM data. PCM_CLKo is in a high impedance state. In this mode the PCM interface port will automatically detect the data rate, strobe positions, clock rate and virtual channel sizes. PPCMDR[2:0] have no function. It should be noted that the relationship between the Number of bits/frame and Clock Rates shown in Table 16 is only true when the PCMENA1 input strobe is 8 kHz. When the PCMENA1 input signal is neither 8 kHz, the SSIDR[2:0] status register will indicate the number of bits (clock cycles) per frame.

PCM Port Control Register - Firmware Manual ZL38500		
SSIDR [2:0]	**Number of bits/frame**	**PCM_CLKi (kHz)**
000	16*	NA
001	32	NA
010	64	NA
011	128	NA
100	256	2048
101	512	4096
110	1024	8192
111	2048	16384

Table 16 - PCM Timing Mode 6 Measured Clock Rate of PCM_CLKi Input

* It should be noted that when 8 bits/frame operation is selected only one short virtual channel can enabled; when 16 bits/frame operation is selected only two short or one long virtual channel can be enabled.

4.3 TDM - ST-BUS, GCI & McBSP Operation

Default frame pulse position is ST-BUS format with the active phase straddling the frame boundary, see Table 17. The frame pulse may also be programmed to have its active phase complete on the frame boundary for McBSP format; and to have its active phase begin on the frame boundary for GCI format. See Firmware Manual for the selection of frame pulse PCMfpS[1:0], clock polarity PCLKP, frame pulse polarity PCMfpP and data rate PPCMDR[2:0].

Frame Pulse PCMfpS[1:0]	Bus Format	Description
00	ST-BUS	Active phase straddles frame boundary.
01	GCI	Active phase starts at the frame boundary.
10	McBSP	Active phase starts one TDM clock cycle before the frame boundary.
11	Reserved	Reserved.

Table 17 - TDM Frame Pulse Selection

Figure 11 illustrates the ST-BUS format with master or slave timing (see Table 10). This requires selecting the frame pulse as ST-BUS, the frame pulse polarity must be active low (PCMfpP = 0), the PCM clock polarity must be set so the clock falling edge occurs on the frame boundary (PCLKP = 0). In this format frames are delineated by the last falling edge of the bit clock that occurs during the active low frame pulse, see AC Electrical Characteristics. The frame pulse rate is 8 kHz. This programming is shown in Table 18.

Bus Format	PCMfpS[1:0]	PCMfpP	PCLKP
ST-BUS	00	0	0
GCI	01	1	1
McBSP	10	1	1

Table 18 - TDM - ST-BUS, GCI and McBSP Selection

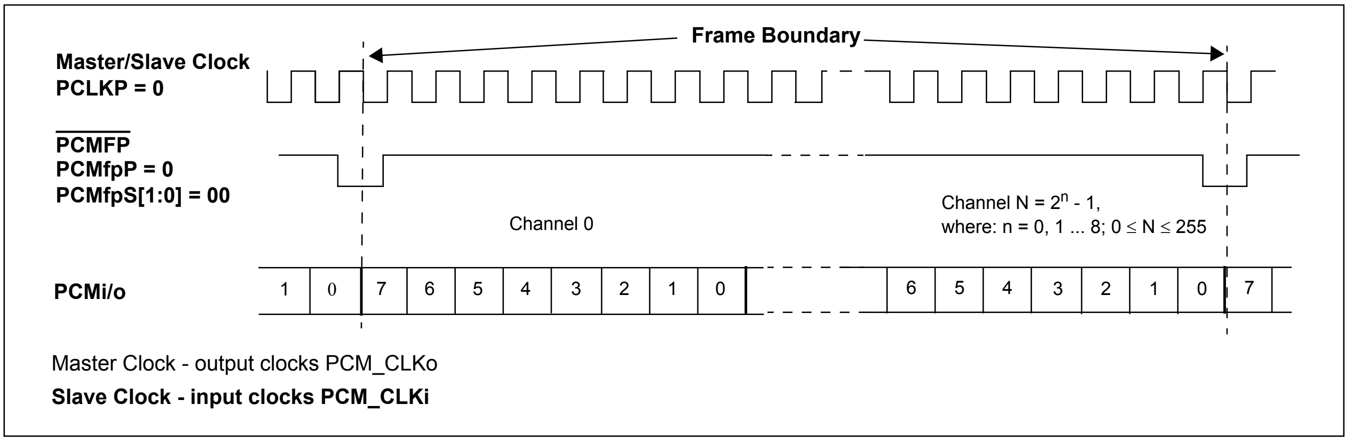


Figure 11 - TDM - ST-BUS Slave/Master Functional Timing Diagram

Figure 12 illustrates the GCI format with slave timing (see Table 10). This requires selecting the frame pulse as GCI, the frame pulse polarity must be active high (PCMfpP = 1), the PCM clock polarity must be set so the clock rising edge occurs on the frame boundary (PCLKP = 1). In this format frames are delineated by the rising edge of the bit clock that occurs immediately before the first falling edge of the bit clock during the active high frame pulse, see AC Electrical Characteristics. The frame pulse rate is 8 kHz. This programming is shown in Table 18.

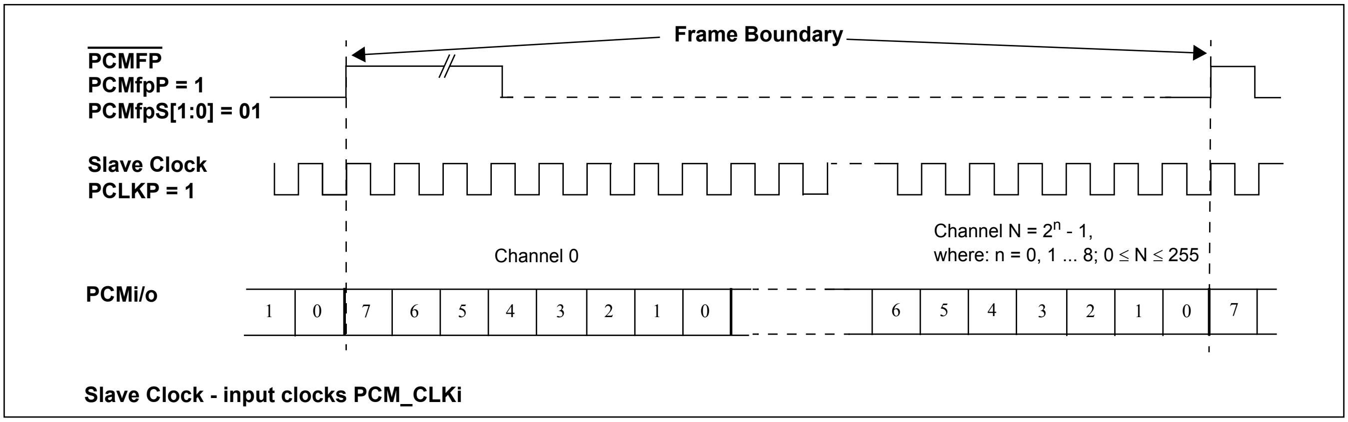


Figure 12 - TDM - GCI Slave Functional Timing Diagram

Figure 13 illustrates the GCI format with master timing (see Table 10). This requires selecting the frame pulse as GCI, the frame pulse polarity must be active high (PCMfpP = 1), the PCM clock polarity must be set so the clock rising edge occurs on the frame boundary (PCLKP = 1). In this format frames are delineated by the rising edge of the bit clock that coincides with the rising edge of the active high frame pulse, see AC Electrical Characteristics. This programming is shown in Table 18.

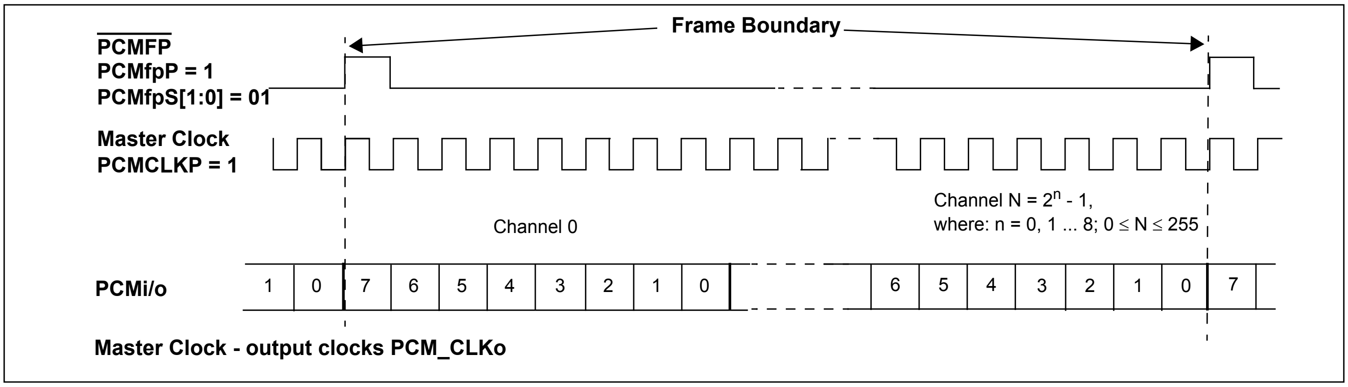


Figure 13 - TDM - GCI Master Functional Timing Diagram

Figure 14 illustrates the McBSP format with master and slave timing (see Table 10). This requires selecting the frame pulse as McBSP, the frame pulse polarity must be active high (PCMfpP = 1), the PCM clock polarity must be set so the clock rising edge occurs on the frame boundary (PCLKP = 1). In this format frames are delineated with slave timing by the last rising edge of the bit clock that occurs immediately after the last falling edge of the bit clock during the active high frame pulse. Frames are delineated in with master timing by the rising edge of the bit clock that coincides with the falling edge of the active high frame pulse, see AC Electrical Characteristics. This programming is shown in Table 18.

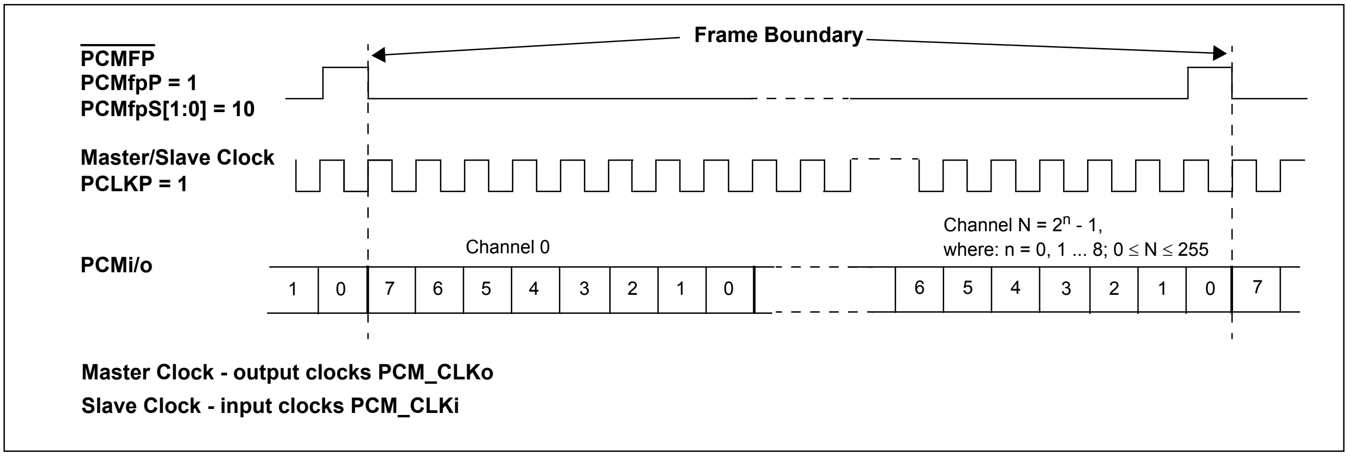


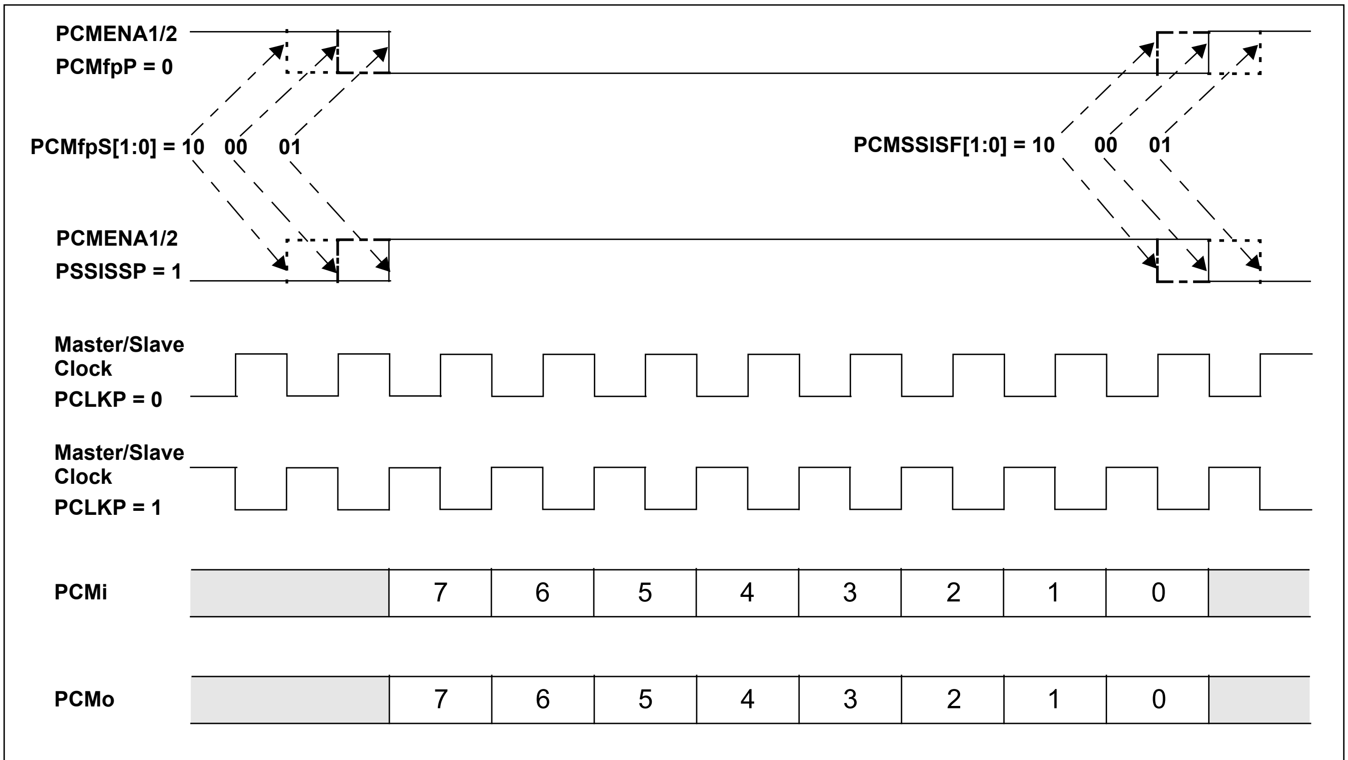
Figure 14 - TDM - McBSP Slave/Master Functional Timing Diagram

4.4 SSI Operation

Figure 15 illustrates the timing options for the SSI format enable signals PCMENA1 and PCMENA2, as well as the bit clock options. Programming for these options is shown in Table 19, the Firmware Manual. The polarity of the active portion of PCMENA1 is selected by control bit PCMfpP (1 for high; 0 for low) and the polarity of the active portion of PCMENA2 is selected by control bit PSSISSP (1 for high; 0 for low). Bit clock polarity is determined by control bit PCLKP.

PCMfpS [1:0]	Enable Active	PCMSSISF[1:0]	Enable Inactive
00	1/2 clock cycle before beginning of bit cell	00	Coincident with end of bit cell
01	1 clock cycle before beginning of bit cell	01	1/2 clock cycle after end of bit cell
10	Coincident with beginning of bit cell	10	1/2 clock cycle before end of bit cell
11	Reserved	11	Reserved

Table 19 - SSI Enable Start; Enable Finish Position Selection

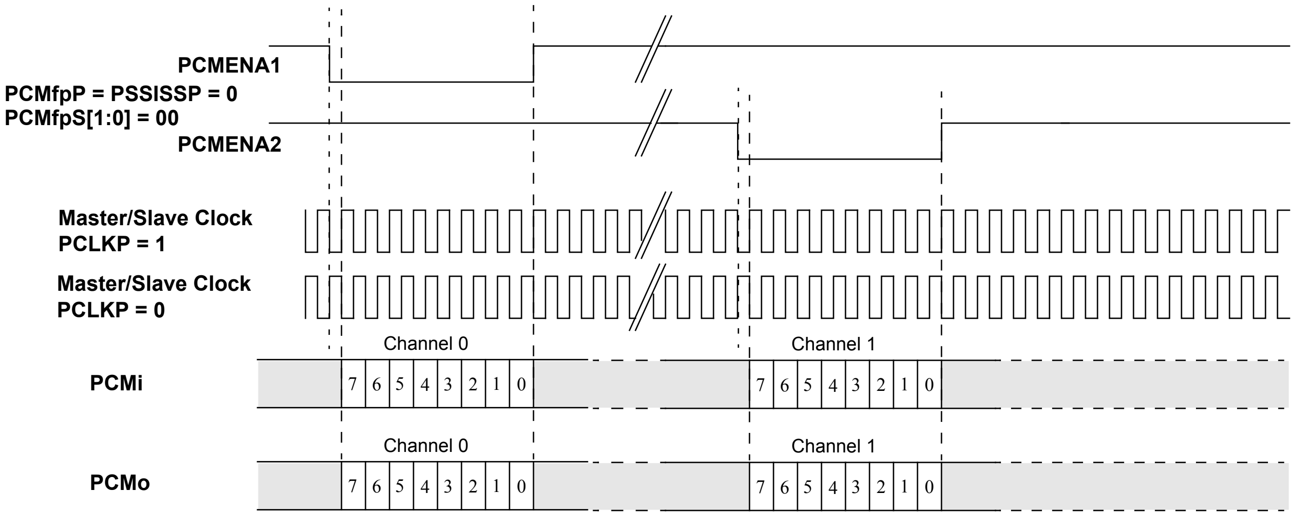


Master Clock - output clocks PCM_CLKo
Slave Clock - input clocks PCM_CLKi

Note: PCMi/o are shown as 8-bit audio channels; however, the timing options illustrated here are applicable to 16-bit audio channels as well

Figure 15 - SSI Slave/Master Enable and Bit Clock Functional Timing

Figures 16 illustrates the SSI functional timing used when the two enable strobes (audio channels) are separated by a non-zero number of bit clock cycles. Here the enable signal polarities are active low (PCMfpP = PSSISSP = 0), either bit clock polarity may be selected (PCLKP = 1/0). In this format frames are delineated by the active edge of PCMENA1 minus 1/2 bit clock cycle. See Firmware Manual to program the positions of the Audio Channels within the 8 kHz frame.



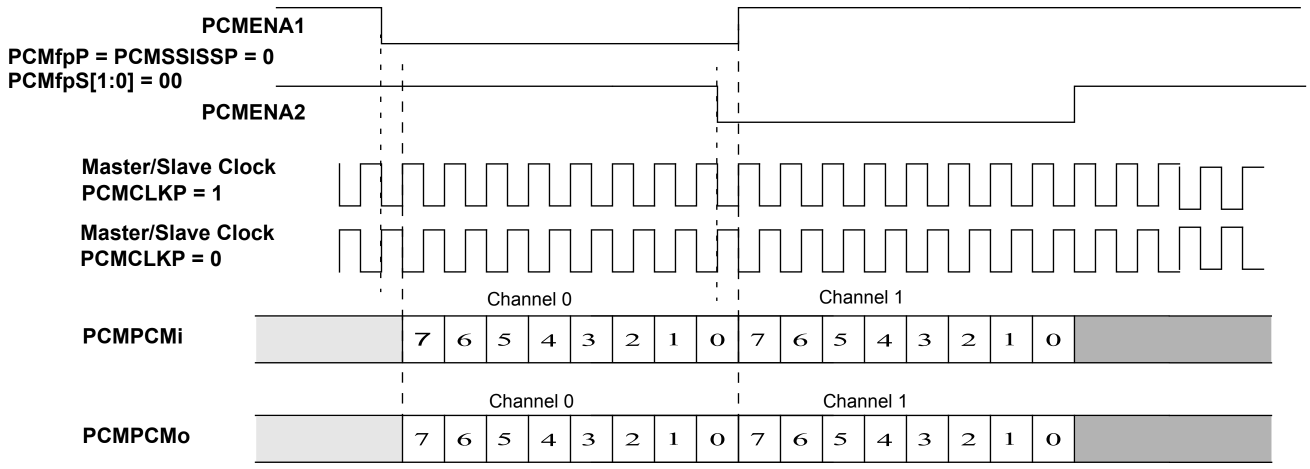
Master Clock - output clocks PCM_CLKo

Slave Clock - input clocks PCM_CLKi

Note: PCMi/o are shown as 8-bit audio channels; however, the timing options illustrated here are applicable to 16-bit audio channels as well

Figure 16 - SSI Mode: Separated Channels Functional Timing

Figure 17 is similar to Figure 16 except for the audio channel positioning. Here the audio channels are adjacent and the associated enable signals overlap, see PCMfpS[1:0] and PCMSSISF[1:0] programming Table 19.



Master Clock - output clocks PCM_CLKo

Slave Clock - input clocks PCM_CLKi

Note: PCMi/o are shown as 8-bit audio channels; however, the timing options illustrated here are applicable to 16-bit audio channels as well

Figure 17 - SSI Mode: Adjacent Channels Functional Timing

4.5 I^{2}S Port Description

The I^{2}S (Inter-IC Sound) port and PCM Port share the same physical pins of the ZL38012. Selection of either I^{2}S port operation or PCM Port One operation is done through FW load. See Firmware Manual.

The I^{2}S port can be used to connect external Analog-to-Digital Converters or CODECs to the internal DSP. This port can operate in master mode, where the ZL38012 is the source of the port clocks, or slave mode, where the bit and sampling clocks (I^{2}S_SCK and I^{2}S_ LRCK) are inputs to the ZL38012. The master clock (I^{2}S_MCLK) is always an output. In I^{2}S port master mode the clock signal at output pin I^{2}S_LRCK is the sampling frequency (f_S), the clock signal at output I^{2}S_SCK is 32 x f_S, and the clock signal at output I^{2}S_MCLK is 256 x f_S. In I^{2}S port slave mode the relationship between the clock signal at input pin I^{2}S_LRCK and the clock signal at input I^{2}S_SCK must be 32 x f_S. In slave mode the 256 x f_S relationship between f_S and the I^{2}S_MCLK is not mandatory, and the I^{2}S_MCLK output pin will be in a high impedance state (see pin description Table 5). This is illustrated in Table 20. See Firmware Manual for I^{2}S programming options.

Master Mode Operation			Slave Mode Operation	
I^{2}S_LRCK output (f_S kHz)	I^{2}S_SCK output (32f_S kHz)	I^{2}S_MCLK output (256f_S kHz)	I^{2}S_LRCK input (f_S kHz)	I^{2}S_SCK input (32f_S kHz)
8	256	2048	8	256

Table 20 - I^{2}S Port Clock Rate and Mode Selection

The I^{2}S interface supports one dual channel CODEC (Figure 18).

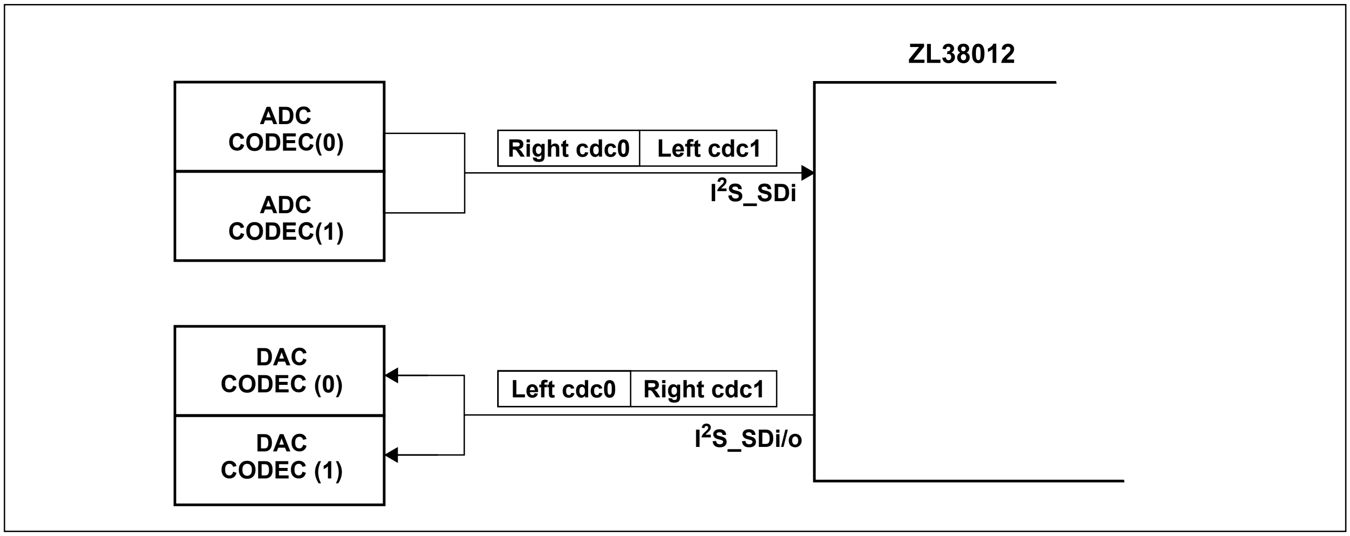


Figure 18 - Dual CODEC Configuration

See section 8.0, “Applications“ on page 70 of this design manual for more information about interfacing to specific external converters.

The format of the I^{2}S bus port can be configured in one of two ways. Figure 19 illustrates the first format, which is left channel first associated with I^{2}S_LRCK (Left/Right Clock signal) low, followed by the right channel associated with I^{2}S_LRCK high (control bit I^{2}SBF = 1). The MSB of the data is clocked out starting on the second falling edge of I^{2}S_SCK (bit clock signal) following the I^{2}S_LRCK transition and clocked in starting on the second rising edge of I^{2}S_SCK (bit clock) following the I^{2}S_LRCK transition. See Firmware Manual for I^{2}S port setup.

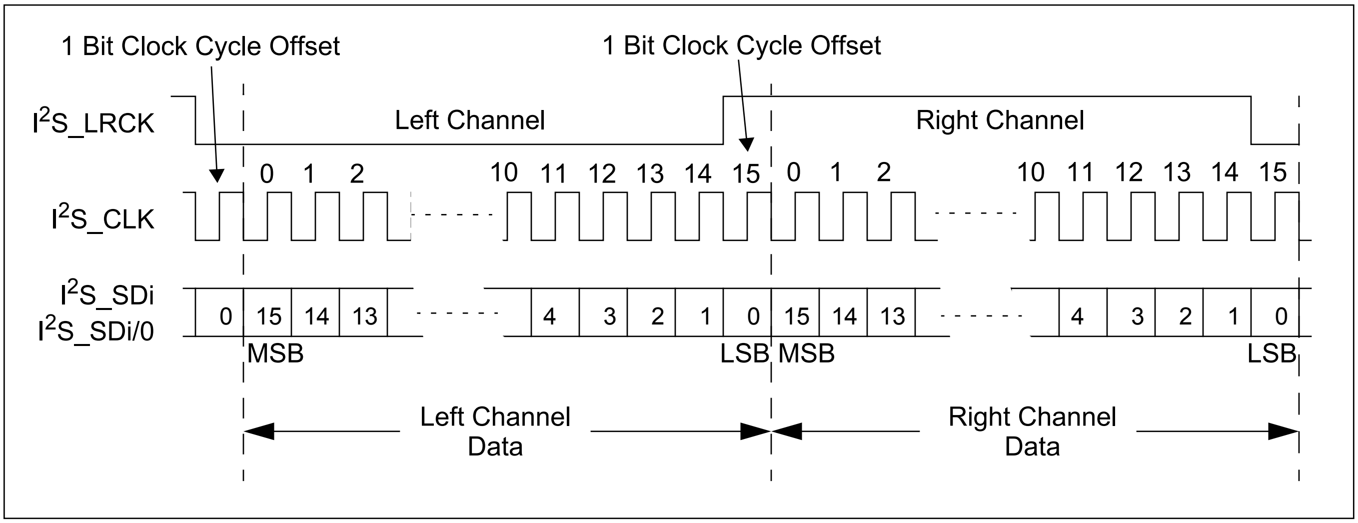


Figure 19 - I^{2}S Audio Interface with Left Channel Enable Low/Right Channel Enable High

The alternate format of the I^2S bus (Figure 20) is left channel first associated with I^2S_LRCK (Left/Right Clock signal) high, followed by the right channel associated with I^2S_LRCK low (control bit I^2SBF = 0). The MSB of the data is clocked out starting on the falling edge of I^2S_SCK (bit clock signal) associated with the I^2S_LRCK transition and clocked in starting on the first rising edge of I^2S_SCK (bit clock) following the I^2S_LRCK transition. See Firmware Manual for I^2S port setup.

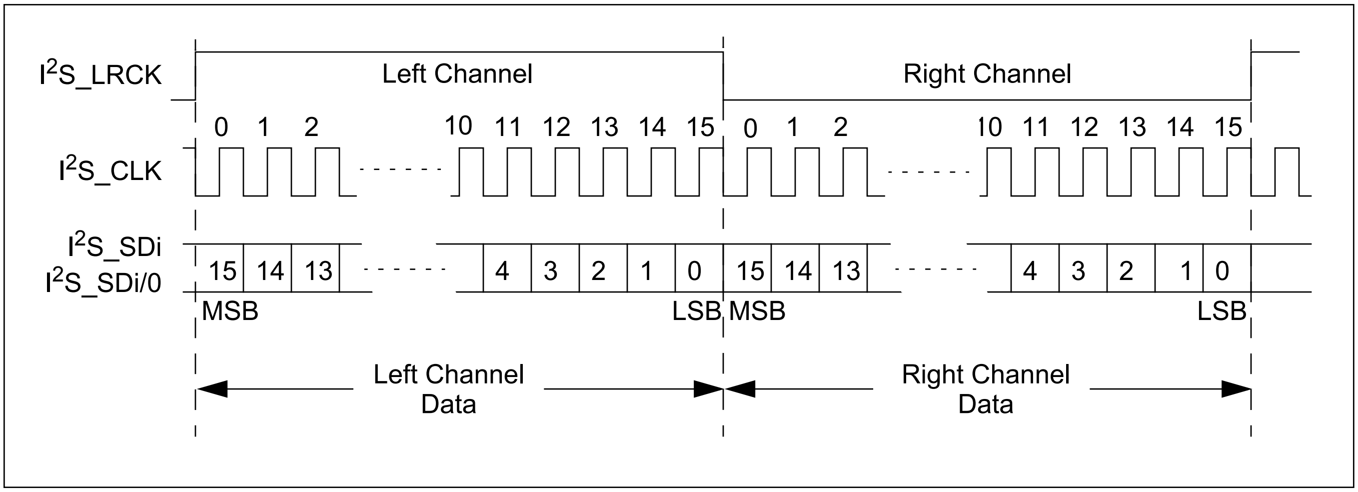


Figure 20 - I^2S Audio Interface with Left Channel Enable High/Right Channel Enable Low

Figure 21 shows the activated I^2S Loopback. In this state audio channel data output from the DSP Core is looped around to the DSP Core input (control bit I^2SLp = 1). Audio channel data is also passed to the I^2S_SDi/o pin, which must be configured as an output (control bit $I^2SSDi/oSel$ = 1). I^2S_SDi has no function when this loopback is activated. See Firmware Manual for I^2S port setup.

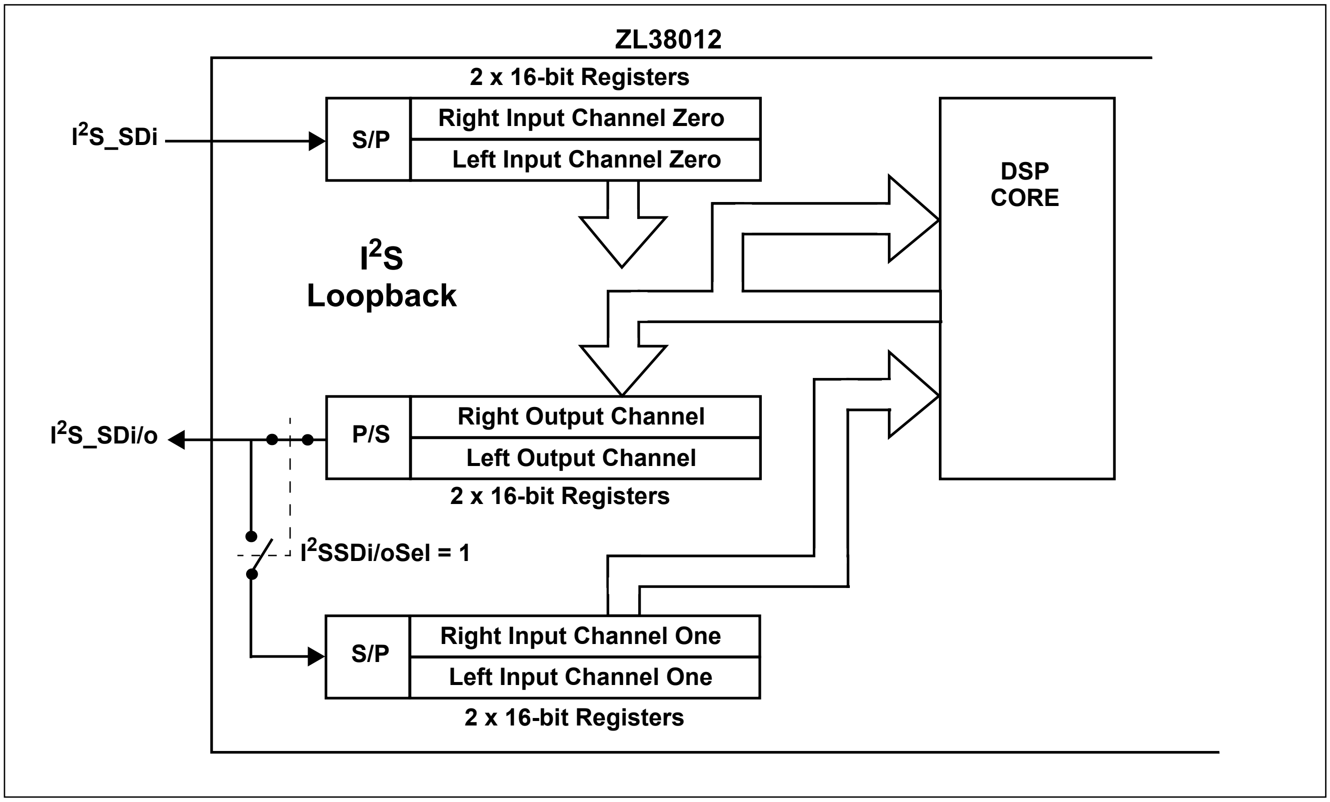


Figure 21 - Inter-IC Sound (I^2S) Loopback

5.0 Host Microprocessor and Peripheral Interfaces

5.1 Master SPI (FLASH Port)

The Master SPI port is used by the ZL38012 to access one or two peripheral devices (chip select signals SPIM_CS[1:0]). It supports both SPI and MICROWIRE modes of operation and can write up to 40 bits or read up to 32 bits in a single access. The Chip Select output signals may be programmed for a single access or burst access. All communication is MSB first and all pins of the master SPI port are outputs controlled by the ZL38012, except SPIM_MISO, see Pin Description Table 6.

The functional timing of the Master SPI port is illustrated in Figure 22. Port reads and writes are similar to those described in the Slave SPI section of this design manual. That is, a write access consists of a port write Command + address/data/control (Figure 26), and a read access consists of a port write Command and port read dummy byte/bits + data (Figures 27 and 28).

The number of clock cycles that is transmitted by the master SPI on SPIM_CLK to communicate with a particular peripheral device is programmable. The total number of clock cycles for a port write and port read are as follows:

port write clocks cycles = (MSUpEn + MSTxWL[1:0] + 1) x 8, and

port read clocks cycles = (MSUpEn + MSTxWL[1:0] + 1 + MSRxWL) x 8 + MSMWR,

where: all variables are decimal equivalents of the binary values programmed in these registers.

See the Firmware Manual for details on programming the Master SPI port and the variables in the equations above. See section 8.0, “Applications“ on page 70 of this design manual for further information on interfacing flash memory to the Master SPI port.

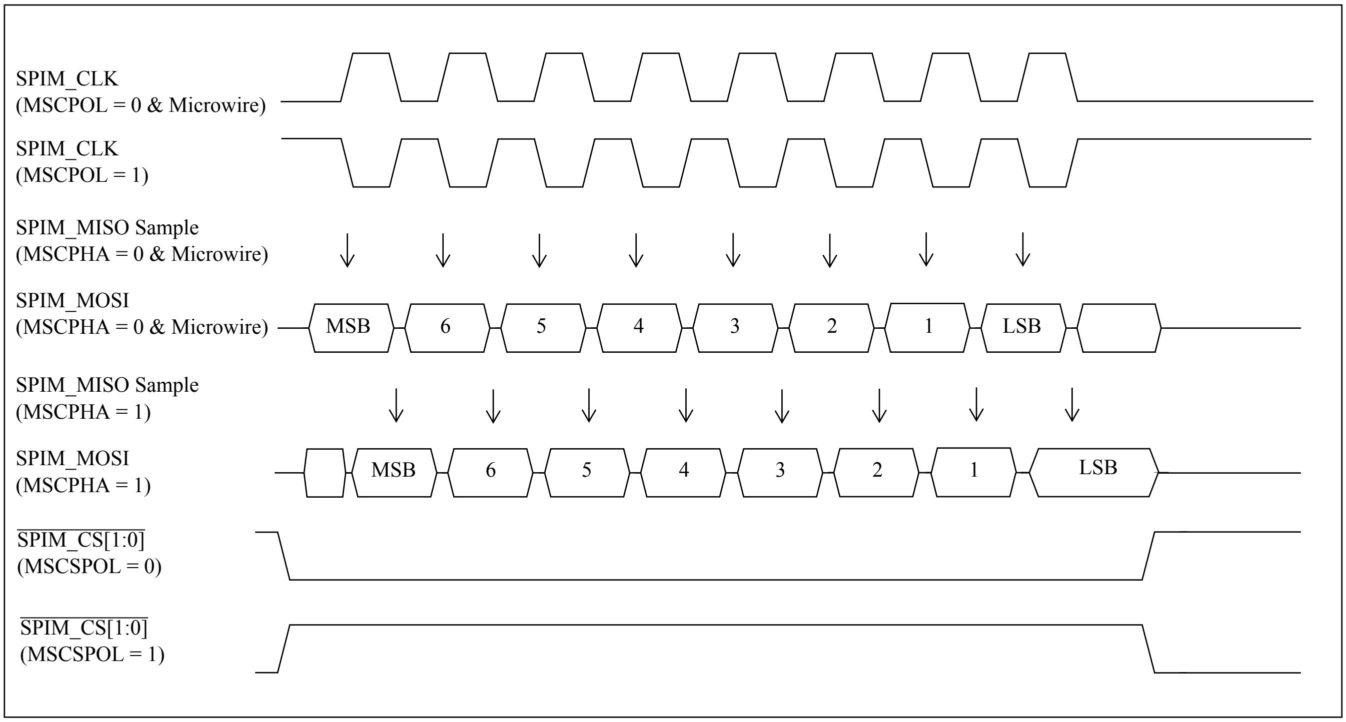


Figure 22 - Master SPI and Microwire Port Functional Timing

5.2 Slave SPI (Host Port)

The slave SPI port may be used by an external host microprocessor to access (Read/Write) the ZL38012 internal control/status registers and memory. Access is initiated when the external host makes signal $\overline{\text{SPIS\_CS}}$ low and is ended when this signal goes high. The host will then apply a clock (maximum 25 MHz) to signal SPIS_CLK to clock data out of SPIS_MISO and in on SPIS_MOSI.

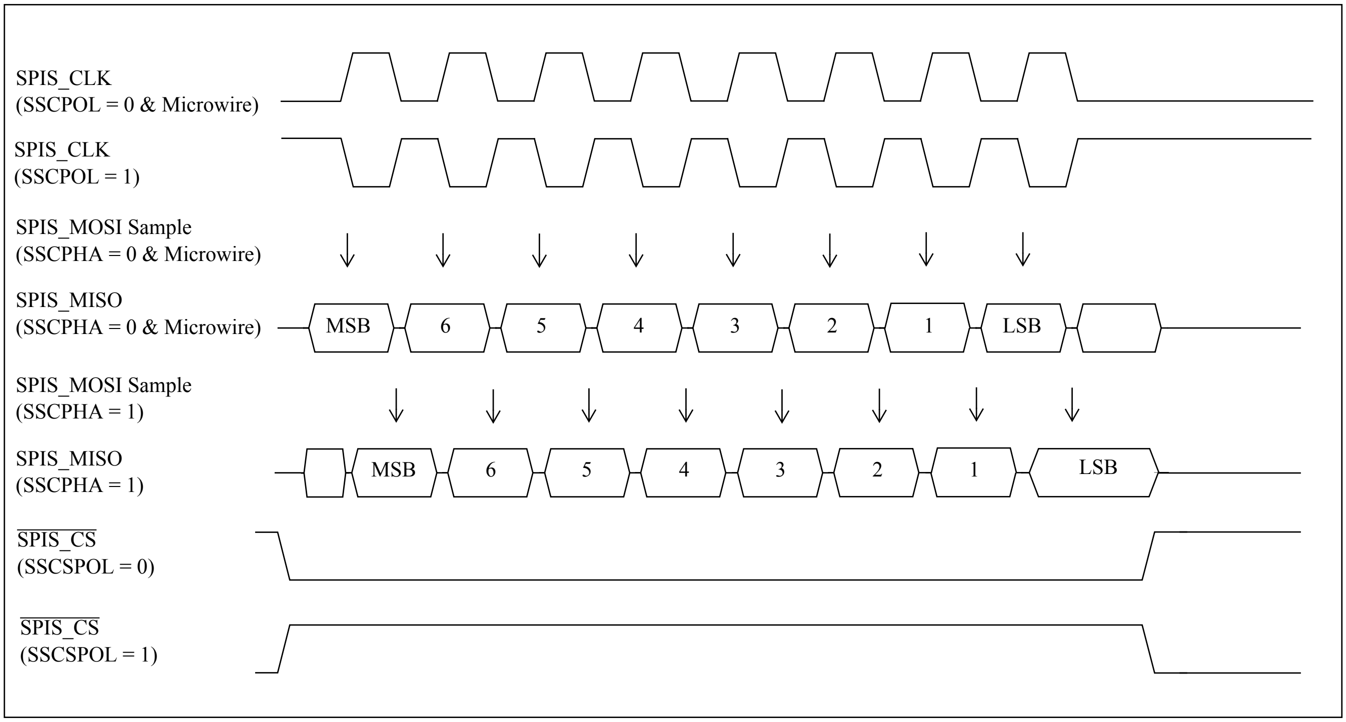


Figure 23 - Slave SPI and Microwire Port Functional Timing

Figure 23 illustrates the Slave SPI Port operation and functional timing, which is determined by the control bits of the Slave SPI Control Register (See Firmware Manual). The following paragraphs describe these options. It should be noted that most accesses will be longer than the 8-bit example shown in Figure 23. An SPI port read access consists of a Command Word being clocked into SPIS_MOSI followed by a series of data bits clocked out of SPIS_MISO, see Figure 27. It will take 8 SPIS_CLK cycles for the ZL38012 to process the read data access function so the first 8 bits clocked out on SPIS_MISO are considered dummy bits. An SPI port write access consists of a Command Word followed by a series of data bits clocked into SPIS_MOSI, see Figure 26. SPIS_CLK may be either a gated or continuous clock.

SSCPOL = SSCPHA = 0 (Microwire)

In this mode of operation data is clocked in (SPIS_MOSI) on the first rising edge of SPIS_CLK after $\overline{\text{SPIS\_CS}}$ becomes active. Data is clocked out (SPIS_MISO) on the falling edge of SPIS_CLK. When control bit SSMWR = 1 Microwire operation is activated. In Microwire operation only one dummy bit needs to be clocked out by the host between the end of the Command Word and the beginning of valid read data. When SSMWR = 0 the normal eight dummy bits need to be clocked out.

SSCPOL = 0; SSCPHA = 1

In this mode of operation data is clocked in (SPIS_MOSI) on the first falling edge of SPIS_CLK after $\overline{\text{SPIS\_CS}}$ becomes active. Data is clocked out (SPIS_MISO) on the rising edge of SPIS_CLK.

SSCPOL = 1; SSCPHA = 0

In this mode of operation data is clocked in (SPIS_MOSI) on the first falling edge of SPIS_CLK after $\overline{\text{SPIS\_CS}}$ becomes active. Data is clocked out (SPIS_MISO) on the rising edge of SPIS_CLK.

SSCPOL = SSCPHA = 1

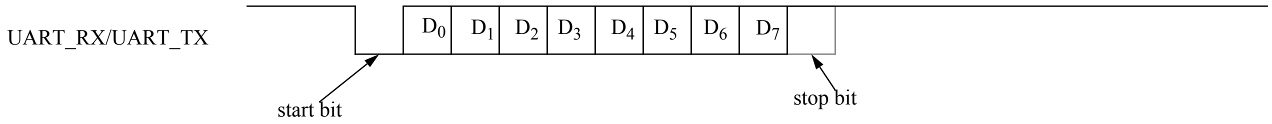
In this mode of operation data is clocked in (SPIS_MOSI) on the first rising edge of SPIS_CLK after $\overline{\text{SPIS\_CS}}$ becomes active. Data is clocked out (SPIS_MISO) on the falling edge of SPIS_CLK.

Flow and maintenance control bits, as well as status bits are described in the Firmware Manual.

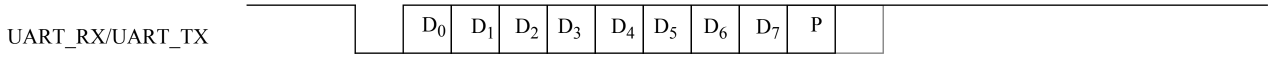
5.3 UART

The UART (Universal Asynchronous Receiver Transmitter) port may be used by an external host microprocessor to access (Read/Write) the ZL38012 internal control/status registers and memory. The ZL38012 DSP will set up the initial parameters of this port (i.e., master/slave, baud rate, stop bits, parity bit...) during the Boot process. After the device has been booted these port options can be changed as per the Firmware Manual.

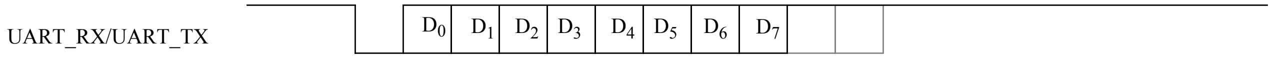
The UART port will support 8-bit data only with any combination of 1 start bit, 0 or 1 parity bit(s) and 1, 1.5 or 2 stop bit(s) as shown in Figure 24.



(a) 1 start bit, 8 data bits, no parity, 1 stop bit



(b) 1 start bit, 8 data bits, with parity, 1 stop bit



(c) 1 start bit, 8 data bits, no parity, 2 stop bits

Figure 24 - Example of Some the Supported UART Interface Timing

Flow and maintenance control and status bits are described in the Firmware Manual.

5.4 Host Interface Operation (Slave SPI and UART Ports)

The control/status registers and memory of the ZL38012 can be accessed (R/W) by an external host through the Slave SPI and the UART ports. Register/Memory read and write accesses are carried out through a series of port read and write accesses as follows:

Write Access

1. Read Control Register - determine if previous port access is complete i.e., If Start/Pending = 0 then step 2, else continue polling.
2. Write Address - this is the ZL38012 register or memory address location.
3. Write Data - this the data that will be written to the ZL38012.
4. Write Control Register - make Start/Pending = 1 to initiate the write operation.

Read Access

1. Read Control Register - determine if previous access is complete i.e., If Start/Pending = 0 then step 2, else continue polling.
2. Write Address - this is the ZL38012 register or memory address location.
3. Write Control Register - make Start/Pending = 1 to initiate the write operation.
4. Read Control Register - determine if last access is complete i.e., Start/Pending = 0.
5. Read Data - this is the data from the ZL38012 register or memory location.

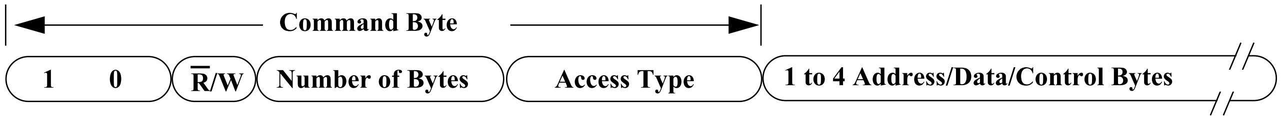
Each Slave SPI and UART port access initiated by an external host consists of an 8-bit Command Byte followed by a series of one to four Address, Data or Control Bytes. This 8-bit Command Byte refers to the port access cycle only, not to the Register/Memory access of which it is a part. The Control Byte may be either 8 or 16 bits long and refers to the Register/Memory read or write access being performed.

Figures 25 shows the structure of each port access. The first two bits of every access must be 10_B for the access to be considered valid and carried out. The next bit is $\overline{R}$/W, which defines the current port access as a read or write operation. When $\overline{R}$/W = 0 (read) the Command Byte will be clocked in and data will be clocked out of the ZL38012 during this port access. When $\overline{R}$/W = 1 (write) the Command Byte followed by the Address, Data or Control Byte will be clocked into the ZL38012 during the port access. This is illustrated in Figure 26, Figure 27 and Figure 28 for the slave SPI interface port and in Figure 29 and Figure 30 for the UART interface port.

The next two bits of the Command Byte determine the number of valid bytes that will follow the Command Byte excluding dummy bytes and bits. The last three bits of the Command Byte determine the type of data that is being transferred immediately following the Command Byte. This can be a 16-bit address, up to 32 bits of read data, up to 32 bits of write data or 8/16 bits of Control. The most significant byte of the Control Word is 0000_000M, where M = 0 selects the Data RAM and Registers or M = 1 selects the Instruction RAM. If the state of this bit (M) does not need to change, then only the least significant byte of the Control Word needs to be sent.

The Start/Pending (P) bit of the Control Word initiates a Register/Memory read or write function. The ZL38012 will make this bit zero when a Register/Memory read or write is complete. The next two bits (WW) indicate the number of data bytes that are to be written or read to complete the Register/Memory access. The R bit determines if the Register/Memory access is read or write. See SPI and UART examples in the 8.0, “Applications“ on page 70 of this design manual.

Serial Bit Sequence



1 0 - valid Command Byte.

$\overline{R}$/W - 0 for read; 1 for write.

Number of Bytes - indicates the number of Address/Data/Control Bytes that will follow the Command Byte:
00 - 8 bits
01 - 16 bits
10 - 24 bits
11 - 32 bits

Access Type - indicates the type of data that will follow the Command Byte:
001 - Control Byte (16-bit, may be 8-bit if most significant bit do not change)
010 - Address Word (16-bit)
011 - Read Data (16, 24 or 32 bit)
100 - Write Data (16, 24 or 32 bit)
000, 101, 110 & 111 - reserved.

1 to 4 Address/Data/Control Bytes:
Address - 0000_AAAA_AAAA_AAAA$_B$
Data - 16, 24 or 32 bits
Control - 16-bits - 0000_000M_0000_PBBR$_B$

where:
A - address bit
M - 0 for Data RAM and Register; 1 for Instruction RAM access
P - (Start/Pending) 1 to initiate access; 0 indicates access complete
B - number of Bytes being transferred:
00 - 8 bits
01 - 16 bits
10 - 24 bits
11 - 32 bits
R - (R/W) 1 to write; 0 to read

Control Register Bit Functions

b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0

b_0 = Memory Operation - write 0 for read; 1 for write

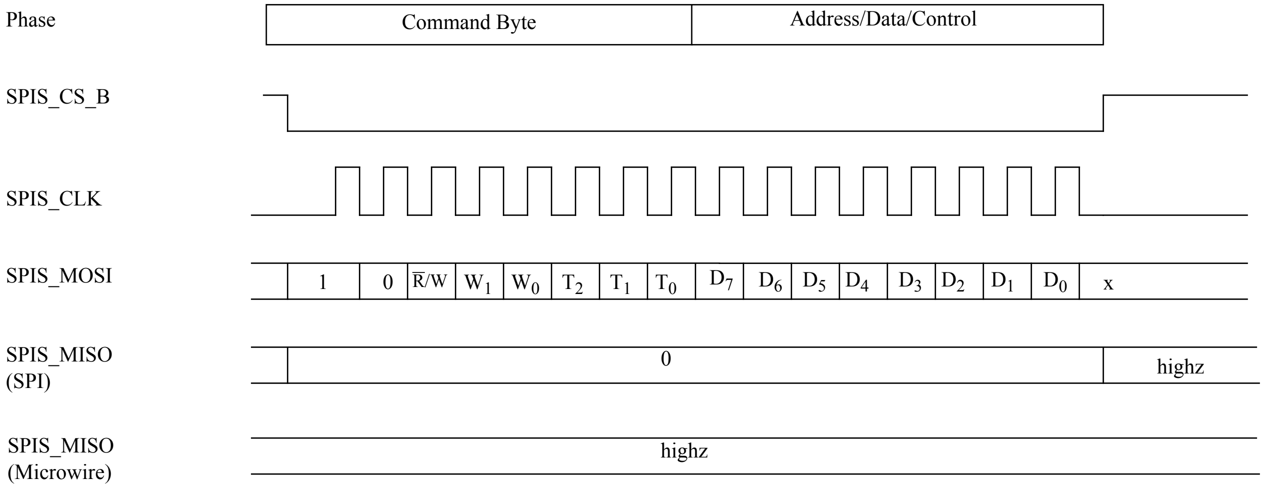
$b_2 b_1$ = Memory Width - write 00 for 8 bits; 01 for 16 bits; 10 for 24 bits and 11 for 32 bits

b_3 = Start/Pending - write 1 to start access; read 1 access pending; read 0 access is complete

b_8 = Memory Select - write 0 to access Data RAM and Registers; 1 to access Instruction RAM

Write 0 to all other bits

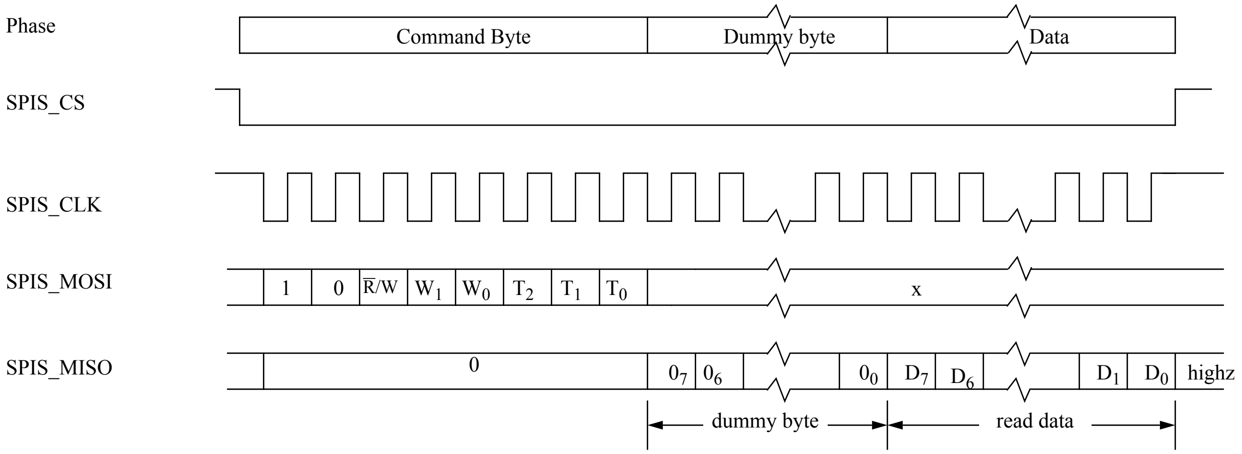
Figure 25 - Slave SPI and UART Port Access



$\overline{R}$/W: determines read or write access (1 in this example)
W_1, W_o: determines the access width (00 in this example)
T_2, T_1, T_0: indicates the type of data that follows: Address, Data or Control
D_7, D_6, ..., D_0: data or control byte to be written (could be up to 32 bits)

SSCPOL=0 / SSCPHA = 0 and Microwire

Figure 26 - Example of a Port Write Access to the Slave SPI Port (8-bit data)



R/W: determines read or write access (0 in this example)
W_1, W_o: determines the access width (00 in this example) excluding dummy byte.
T_2, T_1, T_0: indicates the type of data that follows: Address, Data or Control
0_7, 0_6, ..., 0_0: dummy byte (always 8 bits)
D_7, D_6, ..., D_0: read data byte (could be up to 32 bits)

SSCPOL=1 / SSCPHA = 1

Figure 27 - Example of a Port Read Access to the Slave SPI Port (8-bit data)

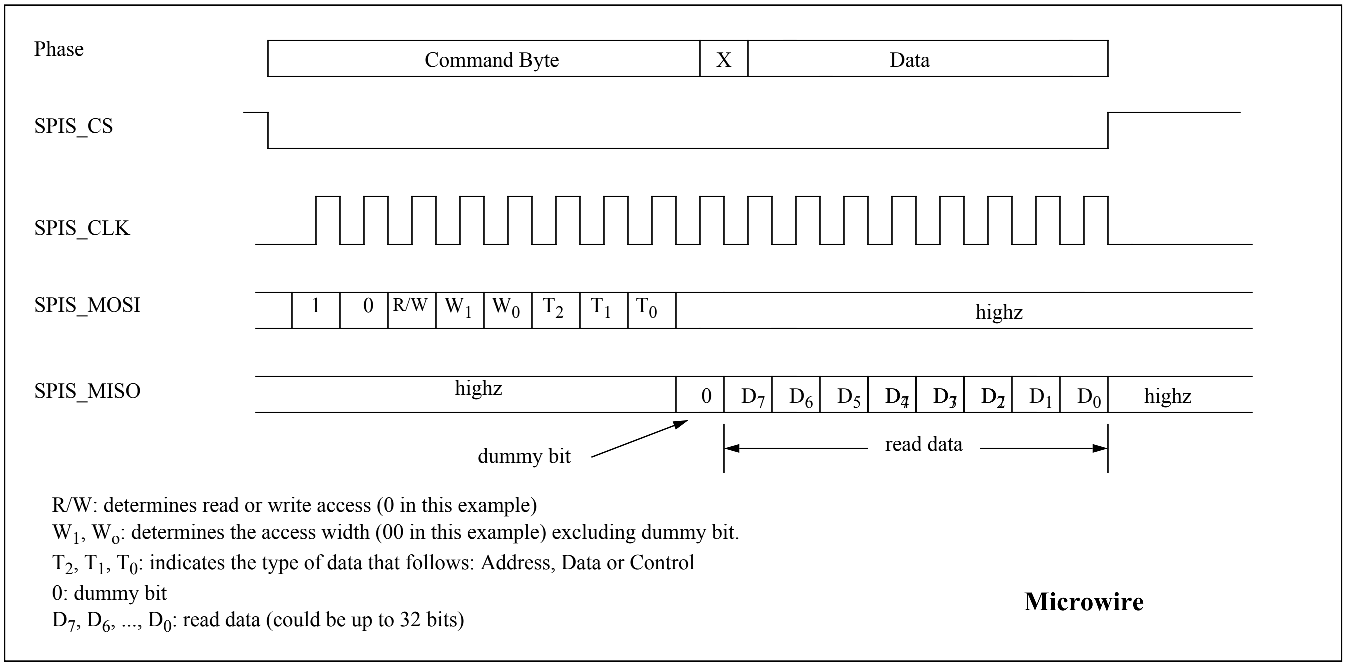
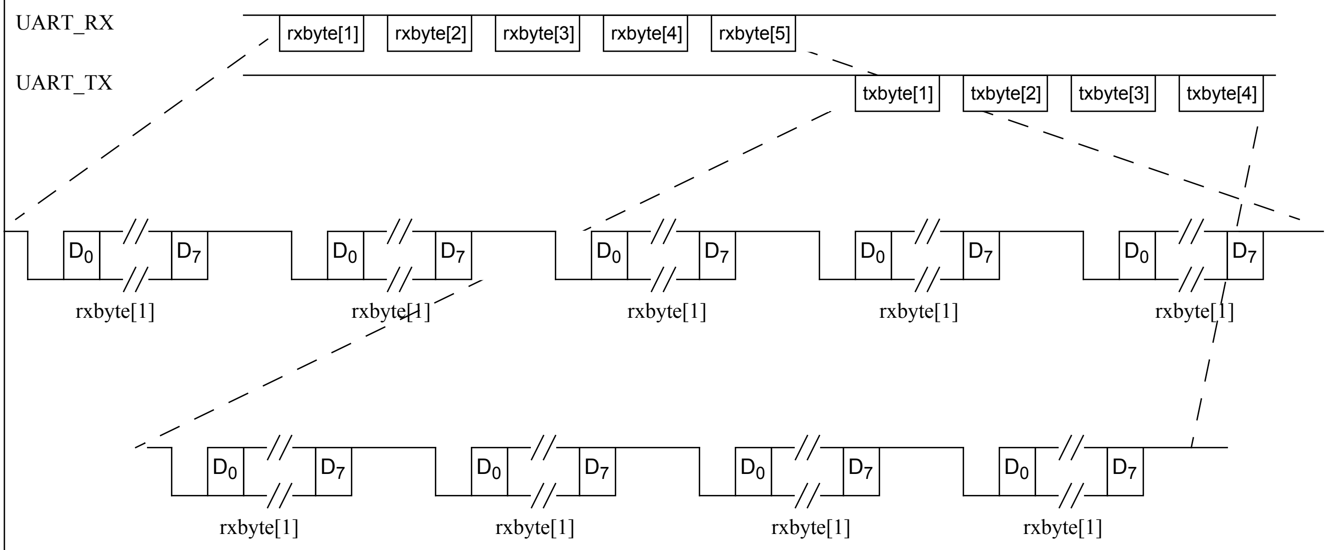


Figure 28 - Example of a Port Read Access to the Slave SPI Port (8-bit data)

When the UART port has been defined as a slave (see Firmware Manual) it can be used by an external host master to access the Data RAM, Registers and Instruction RAM. The UART interface port requires that data sampled on UART_Rx be 5 characters long and that transmit data on UART_Tx will be 4 characters long. The Command, Address, data and control bytes used with the UART interface are the same as for the SPI Slave interface, see Figure 25. Examples of UART Memory/Register read and write accesses are illustrated by Figure 29 and Figure 30. See SPI and UART examples in the 8.0, “Applications“ on page 70 of this design manual.

The UART_Rx input must synchronized on the data from the host microprocessor. This is achieved by the host sending a series of at least 5 all ones characters (idle signal) to force re-synchronization. The first zero received after this all-ones sequence will be interpreted as a start bit of a character that contains a new Command Byte.

Flow and maintenance control bits, as well as status bits are described in the Firmware Manual.



rxbyte[1]: Command Byte

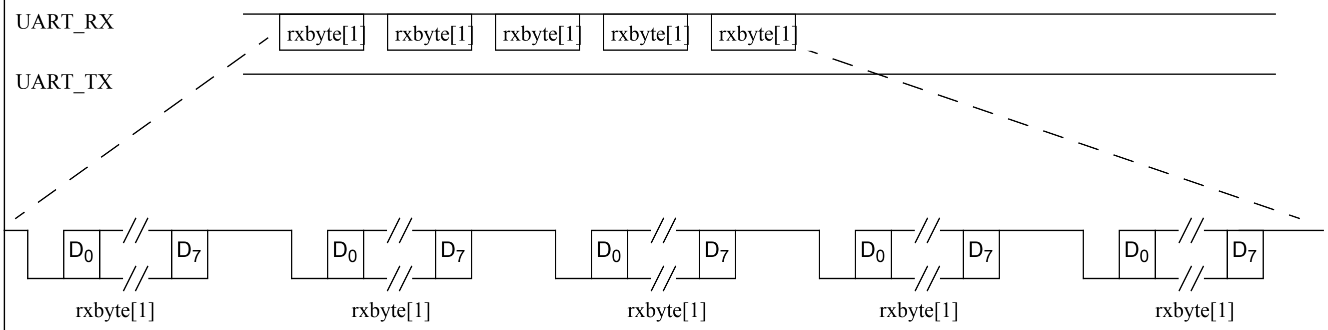
- D_7- D_6: always 10
- D_5: determines read or write access (0 in this example)
- D_4- D_3: access width (00 = 8 bits, 01 = 16 bits, 10 = 24 bits, 11 = 32 bits)
- D_2-D_0: Indicates the type of data that follows: Address, Data or Control

rxbytes[2:5]: unused for read accesses

txbytes[1:4]: read data returned

- txbyte[1]: bits<31:24>
- txbyte[2]: bits<23:16>
- txbyte[3]: bits<15:8>
- txbyte[4]: bits<7:0>

Figure 29 - Example of a Read Access to the Slave UART Port



rxbyte[1]: Command Byte

- D_7- D_6: always 10
- D_5: determines read or write access (1 in this example)
- D_4- D_3: access width (00 = 8 bits, 01 = 16 bits, 10 = 24 bits, 11 = 32 bits)
- D_2-D_0: Indicates the type of data that follows: Address, Data or Control

rxbytes[2:5]: write data

(32-bit data, where only the LSBs will be used, based on the access width)

- rxbyte[2]: bits<31:24>
- rxbyte[3]: bits<23:16>
- rxbyte[4]: bits<15:8>
- rxbyte[5]: bits<7:0>

Figure 30 - Example of a Write Access to the Slave UART Port

5.5 GPIO

The ZL38012 has 5 GPIO (General Purpose Input/Output) pins that can be individually configured as either input or output, and have associated maskable interrupts. These pins are intended for low frequency signalling.

When a GPIO pin is defined as an input the state of that input pin is sampled with the internal master clock (Mclk = 100 MHz) and latched into the GPIO Read Register.

Immediately after a power-on reset ($\overline{\text{RST}}$ pin) the GPIO pins are defined as inputs and their state is captured in the GPIO Start-Up Status Register. The state of this register is used by the Boot program to determine the base functionality and programming options of the device. See the Operations section of this design manual and the Firmware Manual for further definition.

Individual GPIO pins may also be defined as outputs with associated enable/disable (active/high impedance) control. See the Firmware Manual for control and status programming.

6.0 Device Operation

6.1 Initialization

During power-up the ZL38012 must be held in reset, through the $\overline{\text{RST}}$ pin, until after the power supplies have reached their power-on steady state, see “Power Sequencing“ in the 8.0, “Applications“ on page 70 of this design manual. Figure 31 illustrates the sequence of events beginning after the point when the $\overline{\text{RST}}$ pin state returns high. From this point in time (assuming a steady state OSCi or PCM_CLKi signal exists) the ZL38012 APLL will take approximately 500 µs to lock. The state of pins GPIO0 determine which reference clock frequency and signal is to be used by the APLL. This selection is routed directly to the APLL so PLL lock may start immediately after $\overline{\text{RST}}$ goes high. The Timing Mode Select signal latches this state into the APLL block later on in the sequence as shown in Figure 31. 1.9 µs.

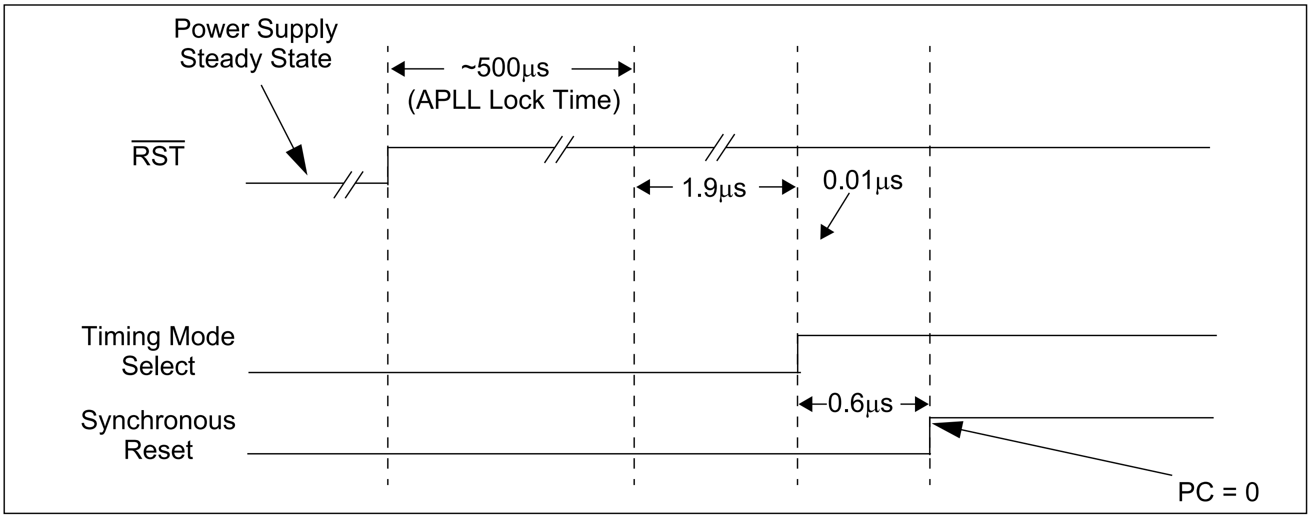


Figure 31 - Initialization Timing

0.4 µs after the GPIO latch pulse occurs the Timing Mode Select signal latches the state of pins GPIO0. 0.6 µs after this the device will come out of synchronous reset and begin executing Boot Code instructions starting at PC = 0 (Program Counter = 0). Synchronous reset will initialize all the control registers to their default values, See Firmware Manual.

It should be noted that a reset that is initiated by the expiration of the Watch Dog Time will not affect the $\overline{\text{RST}}$ or GPIO[4:0] Latch signals. Therefore, the GPIO at Start-Up Status Register will not be updated. This reset starts with the Timing Mode Select and Synchronous Reset signals.

The operation of the digital audio interfaces and CODEC[1:0] depend on clock signals from the Timing Generator. The Timing Generator contains a DPLL, which may take a maximum of 3 seconds to lock. This 3 seconds begins after the Synchronous Reset goes high.

During power-up the $\overline{\text{TRST}}$ pin of the JTAG port is to be pulled low and is to remain low for as long as the ZL38012 is in its normal operating state.

6.2 Boot

Once the ZL38012 comes out of synchronous reset it will begin executing Boot Code instructions at PC = 0. The Boot code will load the device firmware (normally stored in external Flash Memory) into the onboard instruction RAM, see “FLASH Specification“ in the 8.0, “Applications“ on page 70 of this design manual. Once this is complete the PC will jump to address 0x410 and start executing the firmware code. See Firmware Manuals for specific firmware load options at boot.

6.3 Timing Architecture and Mode Selection at Power-Up

The ZL38012 requires an external clock source connected to one of the following combinations of OSCi, OSCo and PCM_CLKi for normal operation. Figure 32 illustrates the ZL38012 functional clock architecture and examples of valid clock combinations are described as follows:

1. **ZL38012 Timing Master with external parallel mode crystal**. This option requires that a parallel mode crystal be connected across OCSi and OCSo, see “Crystal Oscillator Specification“ in the “Applications“ of this design manual. Input pin PCM_CLKi is connected to ground (logic low). All master timing originates from the crystal. PCM Port can operate with slave timing or internal master timing. PCM Port One and the I^2S port may operate with master or slave timing.
2. **ZL38012 Timing Master with external oscillator**. This option requires that an external 3.3 V TTL clock signal (V_{IH} min = 2.0 V & V_{IL} max = 0.8 V) be connected to input pin OSCi, see AC/DC Electrical Characteristics and “Clock Oscillator“ section of this design manual. Input pin PCM_CLKi is connected to ground (logic low), OSCo must be left open should be connected to ground if it is not used. All master timing originates from an external oscillator. PCM Port can operate with slave timing or internal master timing. The I^2S port may operate with master or slave timing.

In order for the ZL38012 to function normally the APLL shown in Figure 32 must be locked to a stable reference as described by the above examples. This reference comes from the OSC circuit. The OSC circuit clock signal must be one of the values listed in Table 21 for the same reason. The APLL reference and feedback divider settings are selected during the power-on reset through GPIO0. This is discussed further on in this section.

The 400 MHz APLL output clock is divided by 4 to produce the 100 MHz internal MCLK, which is used to clock the DSP Core and internal peripheral functions. The 400 MHz clock is also the reference for the Timing Generator block, which generates a master clock for the CODEC[1:0] and ZL38012 digital audio interface ports (PCM Port and I2S). The Master/Slave (M/S) selection bits for these interface ports are found in the port control register sections of the application specific Firmware Manual.

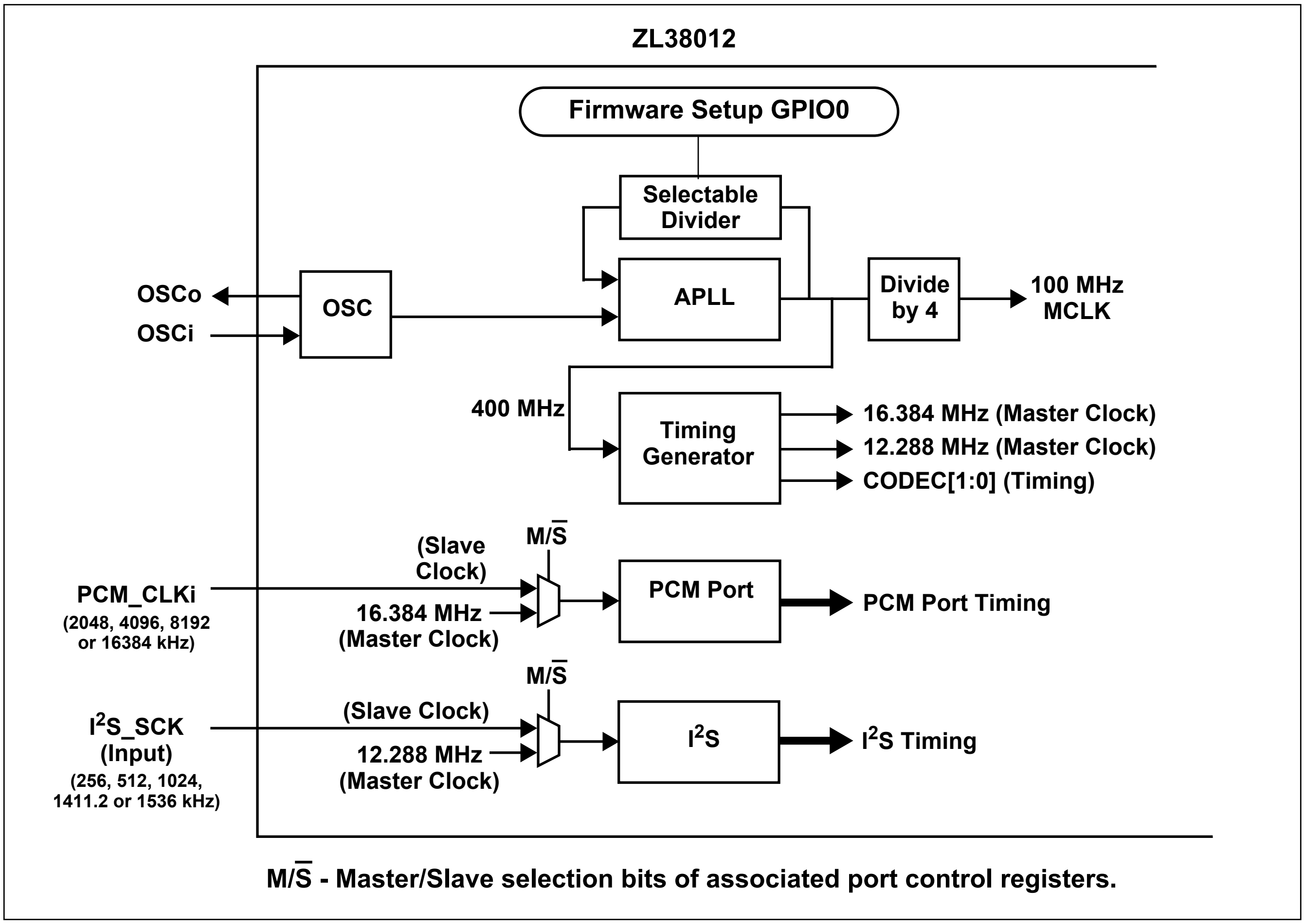


Figure 32 - ZL38012 Master/Slave Timing Selection and Clock Distribution

The state of pins GPIO0 selects the APLL timing reference for the ZL38012 immediately after power-on reset when pin $\overline{\text{RST}}$ goes high. The relationship between timing options and GPIO0 states is shown in Table 21.

GPIO[0]	Clock Source	
	Source Pin	Freq (MHz)
0	OSCi	20.0
1	OSCi	25.0

Table 21 - ZL38012 Timing Reference Selection at Power-up

7.0 AC/DC Electrical Characteristics

Absolute Maximum Ratings[1]

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage[2]	V_{DD_IOmax}	-0.5	5.0	V
2	Core Supply Voltage[3]	V_{DD_CRmax}	-0.5	1.5	V
3	Input Voltage [4]	V_i	-0.5	7.0	V
4	Continuous Current at Digital Outputs	I_o		15	mA
5	Package Power Dissipation	P_D		1	W
6	Storage Temperature	T_S	-55	+125	°C

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
2. Includes V_{DD}IO and V_{DD}OSCIO.
3. Includes V_{DD}CORE, V_{DD}OSC, AV_{DD}APLL, DV_{DD}APLL, V_{DD}DPLL, C1_AV_{DD} and C0_AV_{DD}.
4. All inputs are 5 voltage tolerant.

Recommended Operating Conditions[1]

	Characteristics	Sym.	Min.	Typ.[2]	Max.	Units
1	I/O Supply Voltages[3]	V_{DD_IO}	3.0	3.3	3.6	V
2	Core Supply Voltage[4]	V_{DD_CORE}	1.14	1.2	1.26	V
3	Codec Supply Voltage[5]	V_{DD_CODEC}	1.14	1.2	1.26	V
4	Input Voltage	V_{I_5V}	0	3.3	5.5	V
5	Operating Temperature	T_{OP}	-40	25	+85	°C

1. Voltages are referenced to their respective ground (e.g., AV_{DD}APLL w.r.t. AV_{SS}APLL) unless otherwise stated.
2. Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
3. Includes V_{DD}IO and V_{DD}OSCIO.
4. Includes V_{DD}CORE, V_{DD}OSC, AV_{DD}APLL, DV_{DD}APLL and V_{DD}DPLL.
5. Includes C1_AV_{DD} and C0_AV_{DD}.

DC Electrical Characteristics [1]

	Characteristics	Sym.	Min.	Typ.[2]	Max.[7]	Units	Notes/Conditions
1	I/O Supply Current	I_{DD_IO}		4	5	mA	Outputs unloaded
2	Core Supply Current	I_{DD_CORE}		8	11	mA	Based on 30% DSP load
3	APLL Supply Current	I_{DD_APLL}		2.5	3	mA	
4	Codec Supply Current	I_{DD_CODEC}		5	6	mA	
5	Power Consumption	P_C		55	73	mW	PCM Ports 0 & 1 Slaves at 2048 KB/s
6	Input High Voltage	V_{IH}	2.0			V	All digital input
7	Input Low Voltage	V_{IL}			0.8	V	All digital inputs
8	Input Leakage (input pins) [3]	I_{IL}			5	µA	$0 \le V_{IN} \le 3.6$ V
9	Input Leakage (Bidirectional pins)[3]	I_{BL}			5	µA	$0 \le V_{IN} \le 3.6$ V
10	Weak Pull-up Current	I_{PU}		-65		µA	Input at 0 V
11	Weak Pull-down Current	I_{PD}		65		µA	Input at VDD_IO
12	Input Pin Capacitance	C_I		5		pF	
13	Output High Voltage	V_{OH}	2.4			V	At 2 mA [4] At 4 mA [5] At 8 mA [6]
14	Output Low Voltage	V_{OL}			0.4	V	At 2 mA[4] At 4 mA[5] At 8 mA[6]
15	Output High Impedance Leakage	I_{OZ}			5	µA	$0 \le V_{IN} \le 3.6$ V
16	Output & Input/Tristate Output Pin Capacitance	C_O		5		pF	

1. Voltages are referenced to their respective ground (e.g., AV_{DD}APLL w.r.t. AV_{SS}APLL) unless otherwise stated.
2. Typical figures are at 25°C at typical recommended voltages and are for design aid only: not guaranteed and not subject to production testing.
3. Maximum leakage on pins (input, output or high impedance state) is over an applied voltage (V_{IN}).
4. 2 mA drive rating on JTAG output, TDO.
5. 4 mA drive rating on GPIOs and UART.
6. 8 mA drive rating on PCM Port interfaces, Master and Slave SPI interfaces, and I^2S interface.
7. Worst case is max V_{DD} and +85°C

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: When the Mic Amp is enabled, the total ADC path accuracy is the sum of the ΣΔ converter accuracy (LA_{ADC}) and the Mic Amp gain accuracy (GA_{M1} or GA_{M2}).

AC Electrical Characteristics - CODEC ADC Parameters†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	ADC ΔΣ converter full scale input level (9 dBm0)	V_{iFS}		806.4		mVppd	ADC code = ±32767 linear.
2	ADC ΔΣ converter 0 dBm0 input level	V_{i0L}		286.1		mVppd	ADC code = ±11626 linear.
3	ADC ΔΣ converter 0dBm0 level accuracy (Notes 1 & 2)	LA_{ADC}	-0.4		+0.4	dB	Excludes Mic Amp gain accuracy. 1020 Hz test tone.
4	Mic Amp gain	G_M		0 6.0 12.0 18.0 24.0 30.0		dB	
5	Mic Amp Gain Accuracy for gains of 0, 6 and 12 dB	GA_{M1}	-0.25		+0.25	dB	See Note 1. 1020 Hz test tone.
6	Mic Amp Gain Accuracy for gains of 18, 24 and 30 dB	GA_{M2}	-0.40		+0.40	dB	See Note 1. 1020 Hz test tone.
7	Mic Amp mode input resistance to ground	R_i	11.4	15	19.2	KΩ	At each of C0/1_ADCi+/-.
8	Input Capacitance to ground	C_i		16		pF	At each of C0/1_ADCi+/-.
9	Allowable capacitive load to ground	C_L			25	pF	At each of C0+/-.
10	Input common-mode voltage tolerance	V_{CMT}			250	mVpp	Mic gains = 0 to 12 dB. 180 Hz test tone.
11	Power supply rejection ratio (Note 2)	PSSR		70		dB	20 Hz - 100 kHz, 100 mVpp positive supply noise.

Note 2: The voltage measured across BIAS_RF+/- and tolerance on this voltage are included in the ADC ΔΣ converter 0 dBm0 level and accuracy parameters, as well as the DAC 0 dBm0 output level and accuracy parameters. This parameter is not production tested.

AC Electrical Characteristics - CODEC ADC Parameters†

	Characteristic (Note 1)	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	Sample Rate	f_S		8		KS/s	3.072 MHz CODEC Clock.
2	Frequency Response:	f_R				dB	Gain relative to absolute gain at 1020 Hz. Analog input = 0 dBm0. High Pass Filter Enable bit C0/1AHFEn = 1. DC Blocking Frequency bits C0/1ADCB[1:0] = 10 or 11. Includes external AC decoupling.
	0 to 60 Hz				-30		
	100 to 199 Hz				0		
	200 Hz		-3		0		
	201 to 299 Hz		-3		0.25		
	300 to 3000 Hz		-0.25		0.25		
	3001 to 3200 Hz		-0.25		0.25		
	3201 to 3399 Hz		-0.35		0.25		
	3400 Hz		-0.35		0		
	3600 Hz				0		
	4000 Hz				-14		
	4600 to 72000 Hz				-32		
3	Group Delay	GD			360	µs	Analog input = -10 dBm0. Measured at frequency of minimum delay.
4	Group Delay Distortion:	GDD				µs	Analog input = -10 dBm0. Relative to frequency of minimum delay. Includes external AC decoupling.
	500 to 600 Hz				750		
	600 to 1000 Hz				380		
	1000 to 2600 Hz				130		
	2600 to 2800 Hz				750		
5	Total Idle Channel Noise	N_{IC}					Analog input = 0 Vrms Input buffer gain = 0 to 12 dB. DAC input is G.711 quiet code with fixed sign bit.
	µ-law C-message			-85		dBm0C	
	A-law Psophometric			-80		dBm0p	
6	Single Tone Idle Channel Noise:	N_{ST}					Analog input = 0 Vrms Input buffer gain = 0 to 30 dB. DAC input is G.711 quiet code with fixed sign bit.
	300 to 3400 Hz Psophometric			-94	-75	dBm0p	
	10 to 4000 Hz unweighted			-94	-66	dBm0	
7	Single Frequency Distortion	D_{SF}		-94	-80	dB	Analog input = 0 dBm0, single frequency 700 to 1100 Hz. Input buffer gain = 0 to 12 dB. Digital output 300 to 3400 Hz each frequency other than input frequency.
8	Signal to total distortion:	STD				dB	Analog input = 1020 Hz. Input buffer gain = 0 to 12 dB. Total distortion measured using psophometric weighting. Digital input is G.711 quiet code.
	Analog input = -45 dBm0		24				
	Analog input = -40 dBm0		29				
	Analog input = -30 dBm0		35				
	Analog input = 0 dBm0		35				

AC Electrical Characteristics - CODEC ADC Parameters†

	Characteristic (Note 1)	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
9	Gain tracking: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0	G_T	 -0.1 -0.1 -0.35		 0.1 0.1 0.35	dB	Relative to digital output for analog input = -10 dBm0. Analog input = 1020 Hz. Input buffer gain = 0 to 12 dB.
10	Intrachannel crosstalk	XT_{IA}		-90	-70	dB	From DAC of same CODEC. Aggressor digital input = 0 dBm0 at 1020 Hz. Victim analog input = 0 Vrms, input buffer gain = 30 dB. Unrelated CODEC analog input = 0 Vrms, digital input is G.711 quiet code.
11	Interchannel crosstalk from ADC of other CODEC	XT_{IR1}		-90	-70	dB	Aggressor CODEC: ADC input = 0 dBm0 at 1020 Hz, 0 dB input buffer gain; DAC input is G.711 quiet code. Victim CODEC: ADC input = 0 Vrms with 30 dB input buffer gain; DAC input is G.711 quiet code.
12	Interchannel crosstalk from DAC of other CODEC	XT_{IR2}		-90	-70	dB	Aggressor CODEC: DAC input = 0 dBm0 at 1020 Hz, ADC input = 0 Vrms with 0 dB input buffer gain. Victim CODEC: ADC input = 0 Vrms with 30 dB input buffer gain; DAC input is G.711 quiet code.

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Note 1: ADC 16-bit output is converted to 8-bit G.711 A-law or μ-law.

AC Electrical Characteristics - CODEC DAC Parameters†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	DAC full scale output level (9 dBm0)	V_{DACFS}		1200		mVppd	DAC code = ±32767 linear.
2	DAC 0 dBm0 output level	V_{DAC0}		425.8		mVppd	DAC code = ±11626 linear.
3	DAC 0dBm0 output level accuracy (Note 1)	LA_{DAC}	-0.5		+0.5	dB	DAC code =
4	Load Resistance	R_L	10			KΩ	Between C0/1_DACo+ and C0/1_DACo-. See Figures 60 and 61.
5	Allowable capacitive load to ground	C_L			25	pF	At each of C0/1_DACo+/-. Mic or Line Amp mode.
6	Power supply rejection ratio	PSSR	50	75		dB	20 Hz - 100 kHz, 100 mVpp positive supply noise.
7	Bias Reference Voltage	V_{Bias}		839		mV	Measured across pins BIAS_RF+ and BIAS_RF+.
8	Common Mode Bias Voltage	V_{CMB}		556		mV	Measured across pins BIAS_VCM and C0_AV_{SS}.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: The total DAC path level accuracy is the sum of the converter gain accuracy (LA_{DAC}) and the gain accuracy resulting from external component variations. See Figure 61.

AC Electrical Characteristics - CODEC DAC Parameters†

	Characteristic (Note 1)	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	Sample Rate	f_S		8		KS/s	3.072 MHz CODEC Clock.
2	Frequency response: 0 to 200 Hz 201 to 3000 Hz 3001 to 3200 Hz 3201 to 3399 Hz 3400 Hz 3600 Hz 4000 Hz 4600 to 72000 Hz	f_R	 -0.20 -0.3 -0.15 -0.3		 0 0.20 0.25 0.15 0 0 -14 -28	dB	Gain relative to the 1020 Hz absolute gain. Digital input = 0 dBm0. Includes external AC coupling. If AC coupling is excluded, the response is low pass.
3	Group delay	GD			240	μs	Digital input = -10 dBm0. Measured at frequency of minimum delay.
4	Group delay distortion: 500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz	GDD			 750 380 130 750	μs	Digital input = -10 dBm0. Relative to frequency of minimum delay. Includes external AC coupling.
5	Total idle channel noise: μ-law C-message A-law Psophometric	N_{IC}		 -80 -80		 dBm0C dBm0p	Digital input = G.711 quiet code with fixed sign bit. Analog input = 0 Vrms.
6	Single tone idle channel noise: 300 to 3400 Hz C-message 300 to 3400 Hz Psophometric	N_{ST}		 -83 -83	 -73 -50	 dBm0C dBm0p	Digital input = G.711 quiet code with fixed sign bit. Analog input = 0 Vrms.
7	Single frequency distortion	D_{SF}		-50	-46	dBm0	Digital input = 0 dBm0 at 700 to 1100 Hz. Analog output = 300 to 3400 Hz each frequency other than input frequency.
8	Signal to total distortion: Analog input = -45 dBm0 Analog input = -40 dBm0 Analog input = -30 dBm0 Analog input = 0 dBm0	STD	 24 29 35 35			dB	Digital input = 1020 Hz. Measure total distortion in the analog output using psophometric weighting.
9	Gain tracking: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0	G_T	 -0.1 -0.2 -0.2		 0.1 0.2 0.2	dB	Relative to the analog output for digital input = -10 dBm0. Digital input = 1020 Hz.

AC Electrical Characteristics - CODEC DAC Parameters†

	Characteristic (Note 1)	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
10	Intrachannel crosstalk	XT_{IA}		-104	-80	dB	From ADC of same CODEC. Aggressor analog input = 0 dBm0 at 1020 Hz with input buffer gain = 0 dB. Victim digital input is G.711 quiet code with fixed sign bit. Unrelated CODEC analog input = 0 Vrms, digital input = G.711 quiet code with fixed sign bit.
11	Interchannel crosstalk from ADC of other CODEC	XT_{IR1}		-109	-85	dB	Aggressor analog input = 0 dBm0 at 1020 Hz with 0 dB gain. Victim CODEC analog input = 0 Vrms with 0 dB gain. All digital inputs are G.711 quiet code with fixed sign bit.
12	Interchannel crosstalk from DAC of other CODEC	XT_{IR2}		-111	-85	dB	Aggressor digital input = 0 dBm0 at 1020 Hz. Victim CODEC digital input is G.711 quiet code with fixed sign bit. All analog inputs are 0 Vrms with 0 dB gain.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: DAC input is converted from 8-bit A/μ-law to 16 bits.

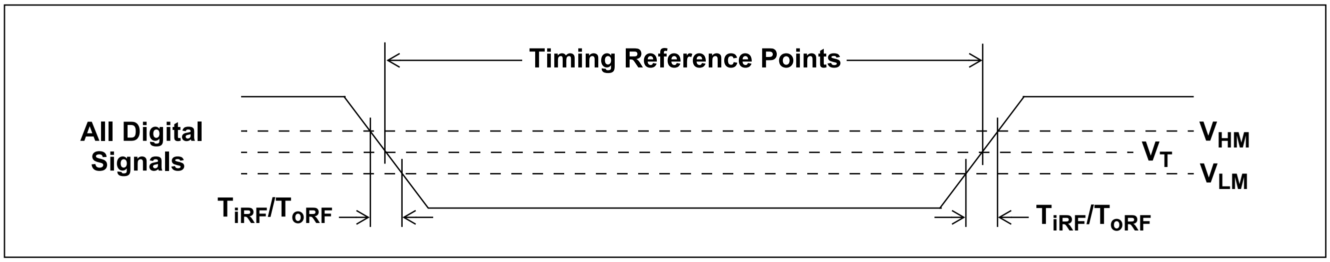


Figure 33 - Timing Parameter Measurement Digital Voltage Levels

AC Electrical Characteristics - External Oscillator Requirements†

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes/Conditions
1	External Oscillator Frequency Accuracy	A_{OSC}	-50		50	ppm	
2	External Oscillator Duty Cycle	DC_{OSC}	40		60	%	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics - Output Jitter Generation (Unfiltered)†

	Characteristics	Max.	Units	Notes/Conditions
1	Jitter on PPCM_CLKo & SPCM_CLKi/o	4	ns_{pp}	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics - PCM Port SSI Slave Mode timing†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	PCM_CLKi, Input Clock Period	t_{SCPS}	54			ns	
2	PCM_CLKi, Input Clock High Time	t_{SCHS}	27			ns	
3	PCM_CLKi, Input Clock Low Time	t_{SCLS}	27			ns	
4	PCMENA1/2 Input Strobe Start Delay	t_{SSSDS}	-10		10	ns	See Note 1
5	PCMENA1/2 Input Strobe Finish Delay	t_{SSFDS}	-10		10	ns	
6	PCMi Input Data Sampling Setup	t_{SDSS}	2			ns	
7	PCMi Input Data Sampling Hold	t_{SDHS}	5			ns	
8	PCMo Output Data Delay (Active to Active)	t_{SDDS}	0		10	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: When PCM Port 1 Control Register bits PCMfpS[1:0] = 00 (active frame pulse straddles the frame boundary) subtract 0.5*PCM_CLK period from the parameter value. When PCM Port Control Register bits PCMfpS[1:0] = 10 (active frame pulse starts one PCM clock cycle before the frame boundary) subtract a PCM_CLK period from the parameter value.

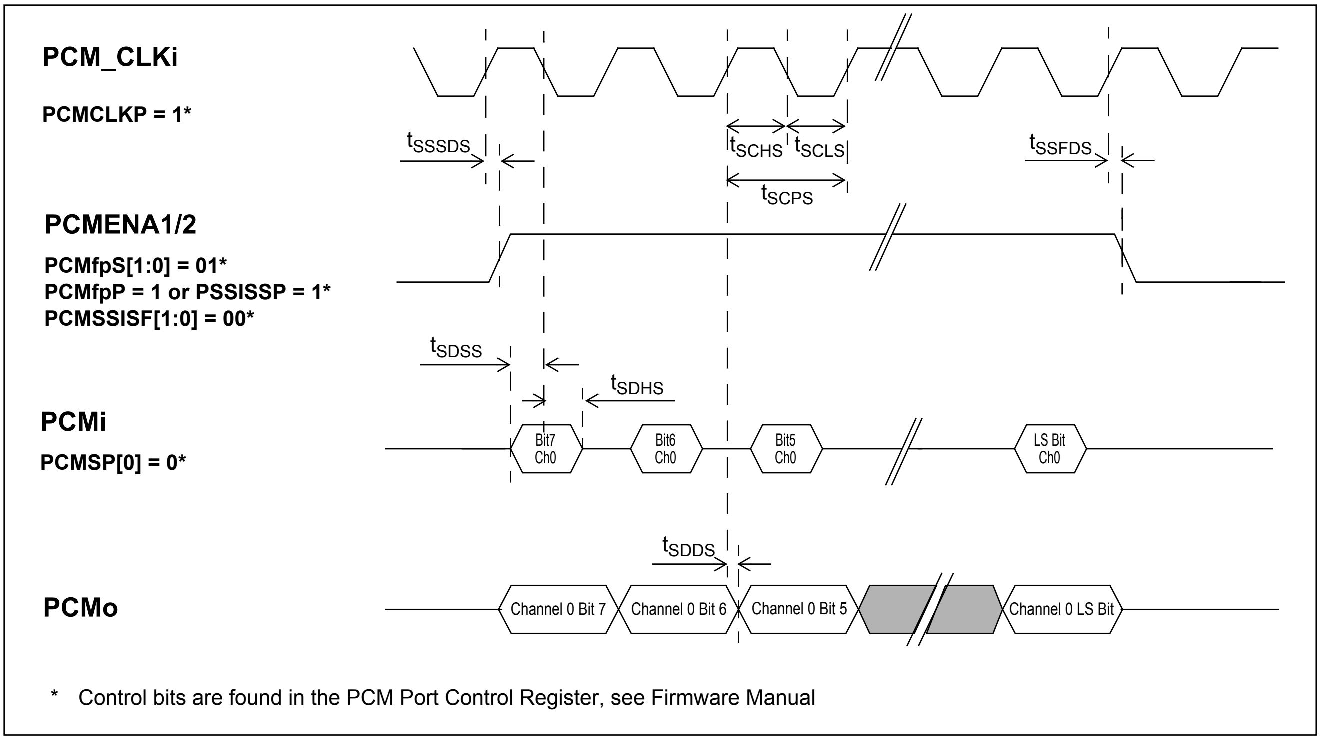


Figure 34 - PCM SSI Slave Mode Timing Diagram

AC Electrical Characteristics - PCM Port SSI Master Mode Timing†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	PCM_CLKo Output Clock Period	t_{SCPM}	53		7820	ns	
2	PCM_CLKo Output Clock High Time	t_{SCHM}	25			ns	
3	PCM_CLKo Output Clock Low Time	t_{SCLM}	25			ns	
4	PCMENA1/2 Output Strobe Start Delay	t_{SSSDM}	-3.5		7.5	ns	See Note 1
5	PCMENA1/2 Output Strobe Finish Delay	t_{SSFDM}	-3.5		7.5	ns	See Note 2
6	PCMi Input Data Sampling Setup	t_{SDSM}	13			ns	
7	PCMi Input Data Sampling Hold	t_{SDHM}	4			ns	
8	PCMo Output Data Delay (Active to Active)	t_{SDDM}	-6		6	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: When PCM Port Control Register bits PCMfpS[1:0] = 00 (active frame pulse straddles the frame boundary) subtract 0.5*PCM_CLK period from the parameter value. When PCM Port Control Register bits PCMfpS[1:0] = 10 (active frame pulse starts one PCM clock cycle before the frame boundary) subtract a PCM_CLK period from the parameter value.

Note 2: When PCM Port Control Register bits PCMSSISF[1:0] = 01 (strobe inactive 1/2 clock cycle after the last data bit is inactive) add 0.5*PCM_CLK period from the parameter value. When PCM Port Control Register bits PCMSSISF[1:0] = 10 (strobe inactive 1/2 clock cycle before the last data bit is inactive) subtract 0.5*PCM_CLK period the parameter value.

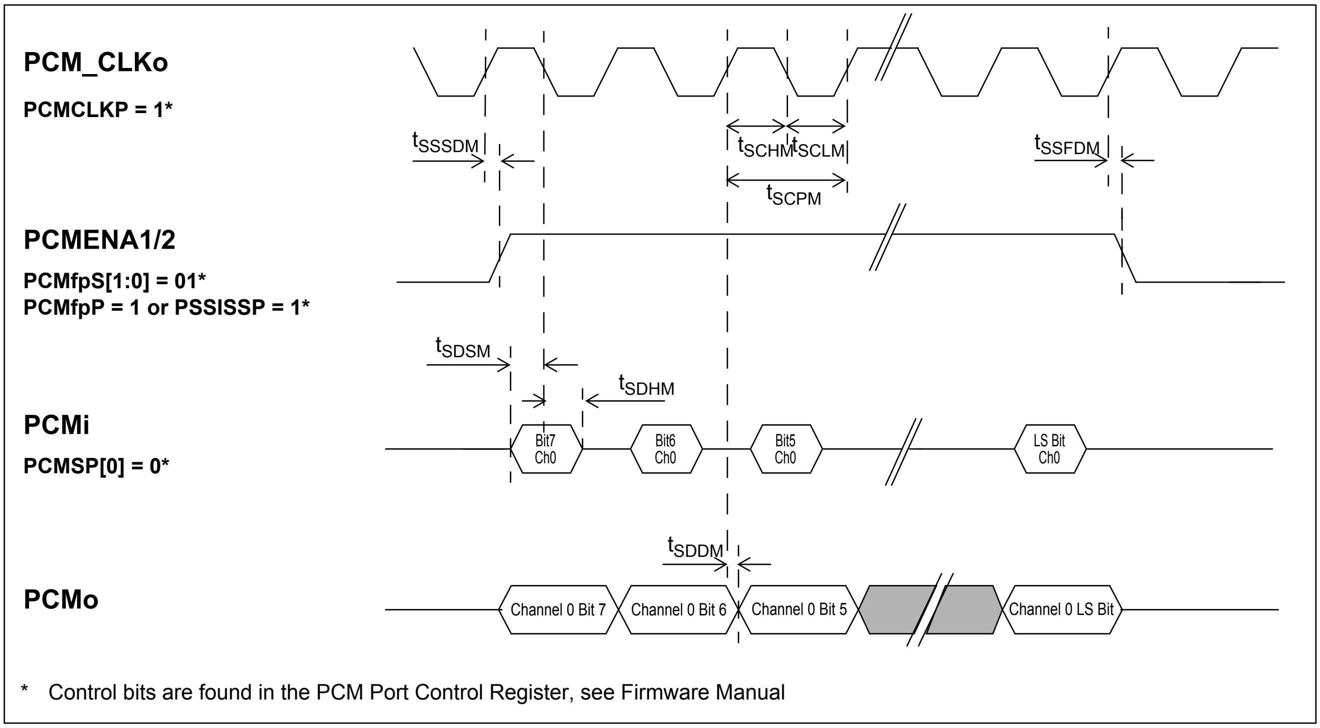


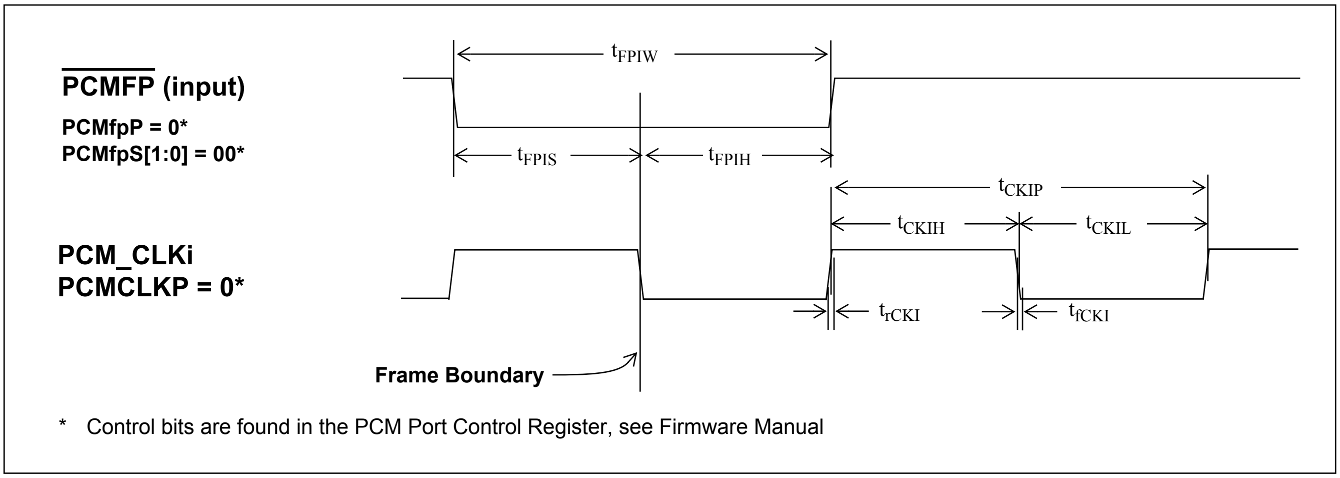
Figure 35 - PCM SSI Master Mode Timing Diagram

AC Electrical Characteristics - PCM Port PCMFP and PCM_CLKi in TDM Slave Mode[†]

	Characteristic	Sym.	Min.	Typ.[‡]	Max.	Units	Notes/Conditions
1	$\overline{\text{PCMFP}}$ Input Frame Pulse Width	t_{FPIW}	50			ns	
2	$\overline{\text{PCMFP}}$ Input Frame Pulse Setup Time	t_{FPIS}	2			ns	
3	$\overline{\text{PCMFP}}$ Input Frame Pulse Hold Time	t_{FPIH}	5			ns	
4	PCM_CLKi, Input Clock Period	t_{CKIP}	54			ns	
5	PCM_CLKi, Input Clock High Time	t_{CKIH}	27			ns	
6	PCM_CLKi, Input Clock Low Time	t_{CKIL}	27			ns	

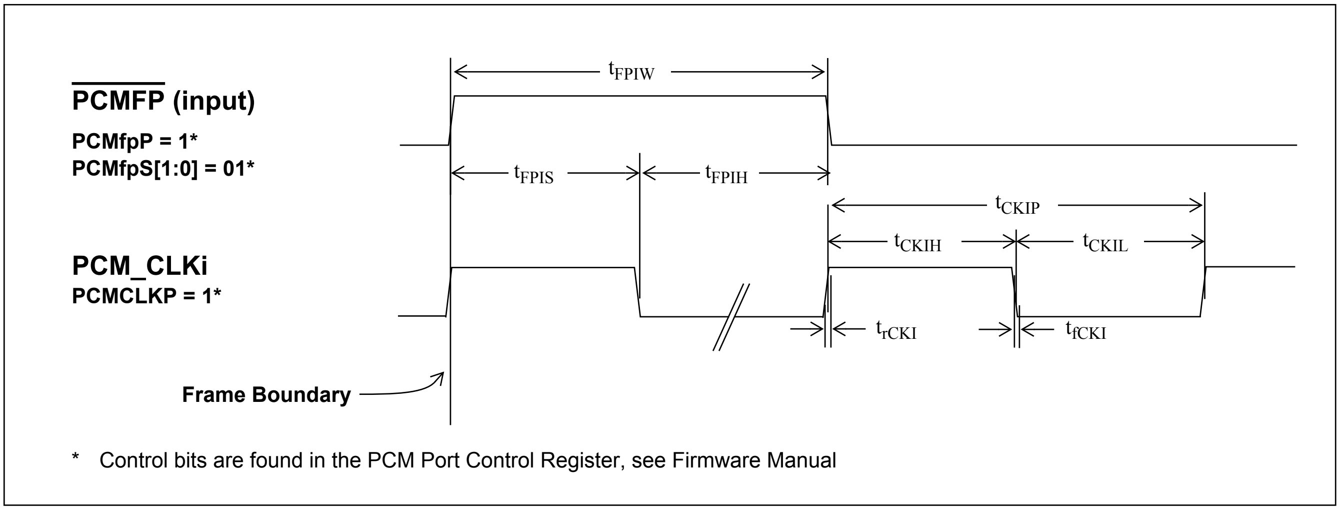
† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



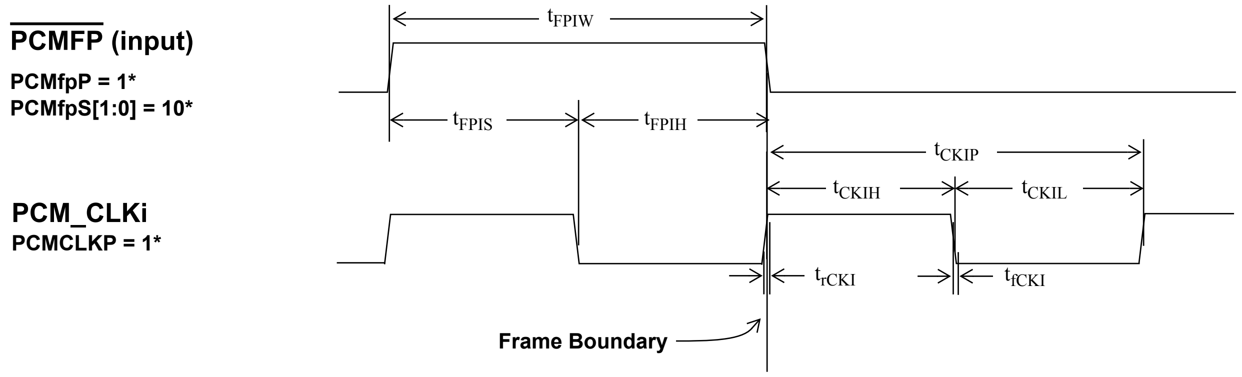
* Control bits are found in the PCM Port Control Register, see Firmware Manual

Figure 36 - TDM - ST-BUS $\overline{\text{PCMFP}}$ and PCM_CLKi Input Timing



* Control bits are found in the PCM Port Control Register, see Firmware Manual

Figure 37 - TDM - GCI $\overline{\text{PCMFP}}$ and PCM_CLKi Input Timing



* Control bits are found in the PCM Port Control Register, see Firmware Manual

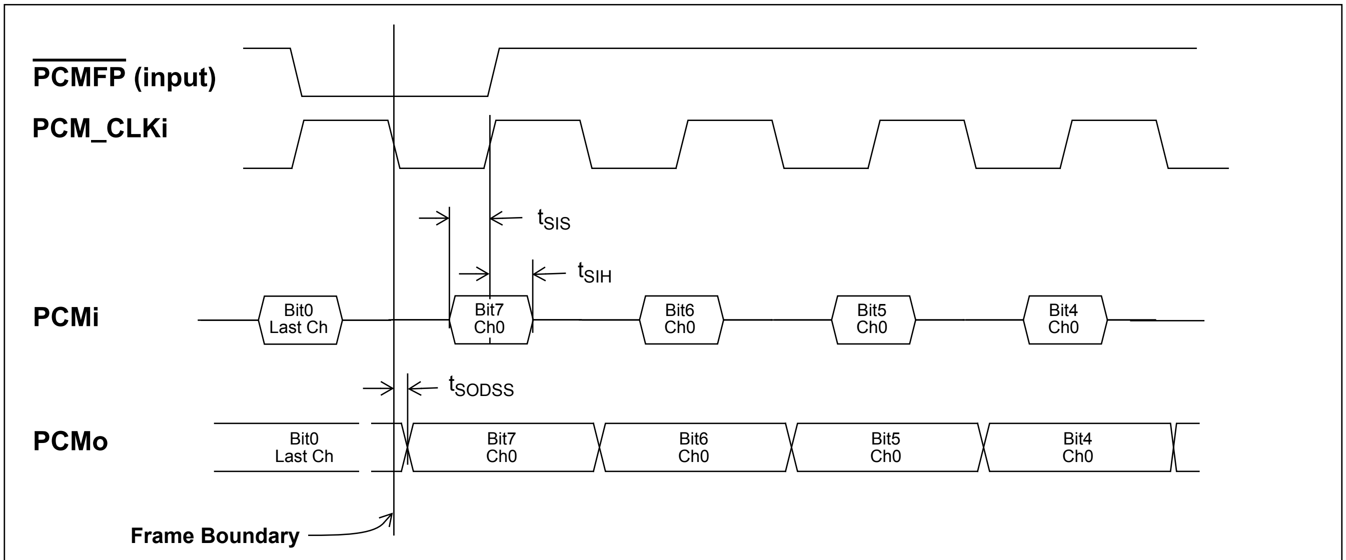
Figure 38 - TDM - McBSP $\overline{\text{PCMFP}}$ and PCM_CLKi Input Timing

AC Electrical Characteristics - PCM Port TDM Slave Mode Timing†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	PCMi Setup Time	t_{SIS}	2			ns	
2	PCMi Hold Time	t_{SIH}	5			ns	
3	PCMo Output Data Delay (Active to Active)	t_{SODSS}	0		10	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



* Control bits are found in the PCM Port Control Register, see Firmware Manual

Figure 39 - TDM Slave Mode Timing Diagram (clock rate equals data rate)

AC Electrical Characteristics - PCM Port TDM Master Mode Timing†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	PCMi Setup Time	t_{SIS}	15			ns	
2	PCMi Hold Time	t_{SIH}	15			ns	
3	PCMo Output Data Delay (Active to Active)	t_{SODSM}	-6		6	ns	C_L = 30 pF

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

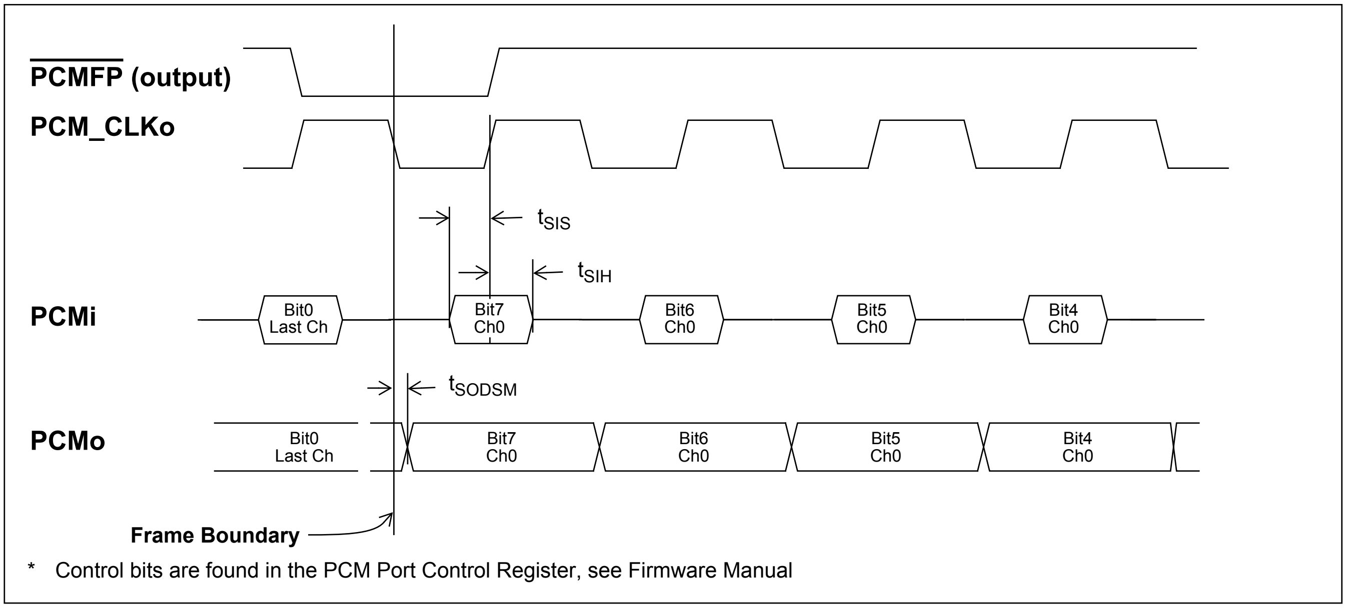


Figure 40 - TDM Master Mode Timing Diagram (clock rate equals data rate)

AC Electrical Characteristics - PCM Port TDM Mode Output Tristate Timing†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	PCMo Delay - Active to High-Z PCMo Delay - High-Z to Active Slave Mode	t_{DZS} t_{ZDS}	0 0		15 15	ns ns	R_L = 1 k, C_L = 30 pF, See Note 1.
2	PCMo Delay - Active to High-Z PCMo Delay - High-Z to Active Master Mode	t_{DZM} t_{ZDM}	-6 -6		6 6	ns ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: High impedance is measured by pulling the voltage to the appropriate rail with R_L, with timing corrected to remove the effect of C_L.

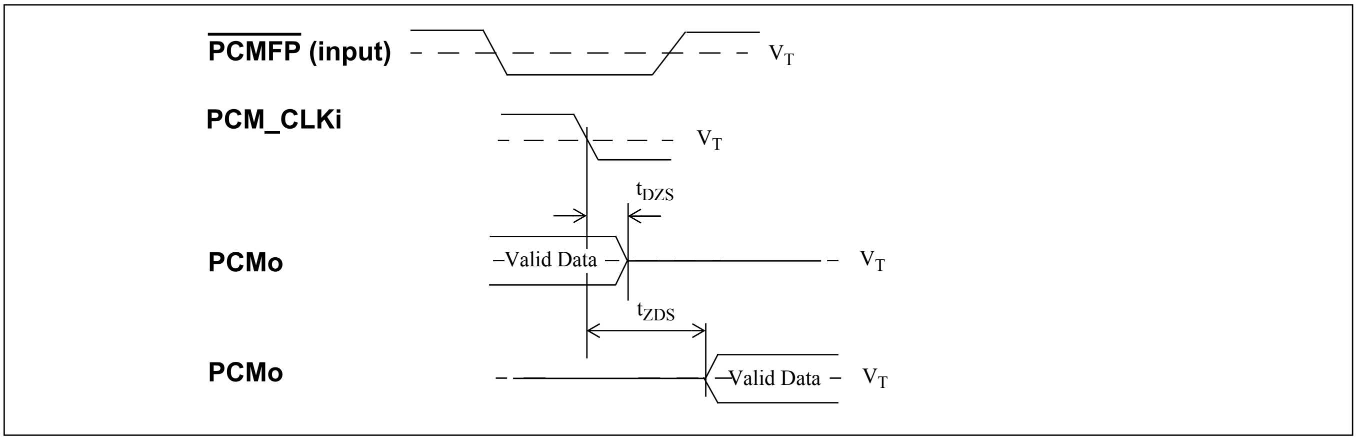


Figure 41 - Output Tristate Timing in TDM Slave Mode

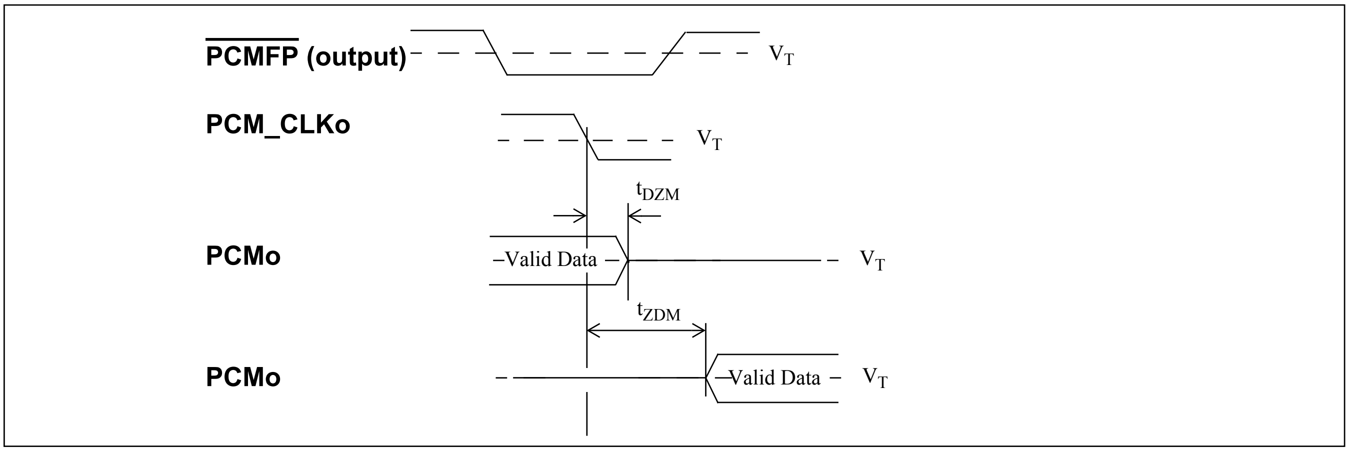


Figure 42 - Output Tristate Timing in TDM Master Mode

AC Electrical Characteristics - PCM Port $\overline{\text{PCMFP}}$ and Output Clocks (TDM Master)†

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	$\overline{\text{PCMFP}}$ Output Pulse Width PCM_CLKo = 16384 kHz PCM_CLKo = 8192 kHz PCM_CLKo = 4096 kHz PCM_CLKo = 2048 kHz PCM_CLKo = 1024 kHz PCM_CLKo = 512 kHz PCM_CLKo = 256 kHz PCM_CLKo = 128 kHz	t_{FPWO}	56 177 239 483 971 1948 3901 7807	61 122 244 488 977 1953 3906 7813	66 127 249 493 981 1958 3911781 7	ns	C_L = 30 pF
2	$\overline{\text{PCMFP}}$ Output Delay from the $\overline{\text{PCMFP}}$ falling edge to the frame boundary PCM_CLKo = 16384 kHz PCM_CLKo = 8192 kHz PCM_CLKo = 4096 kHz PCM_CLKo = 2048 kHz PCM_CLKo = 1024 kHz PCM_CLKo= 512 kHz PCM_CLKo = 256 kHz PCM_CLKo = 128 kHz	t_{FODFO}	25 56 117 239 483 971 1948 3901		36 66 127 249 493 981 1958 3911	ns	C_L = 30 pF
3	$\overline{\text{PCMFP}}$ Output Delay from the frame boundary to the $\overline{\text{PCMFP}}$ rising edge PCM_CLKo = 16384 kHz PCM_CLKo = 8192 kHz PCM_CLKo = 4096 kHz PCM_CLKo = 2048 kHz PCM_CLKo = 1024 kHz PCM_CLKo = 512 kHz PCM_CLKo = 256 kHz PCM_CLKo = 128 kHz	t_{FODRO}	25 56 117 239 483 971 1948 3901		36 66 127 249 493 981 1958 3911	ns	C_L = 30 pF
4	PCM_CLKo Output Clock Period PCM_CLKo = 16384 kHz PCM_CLKo = 8192 kHz PCM_CLKo = 4096 kHz PCM_CLKo = 2048 kHz PCM_CLKo = 1024 kHz PCM_CLKo = 512 kHz PCM_CLKo = 256 kHz PCM_CLKo = 128 kHz	t_{CKPO}	56 177 239 483 971 1948 3901 7807	61 122 244 488 977 1953 3906 7813	66 127 249 493 981 1958 3911781 7	ns	C_L = 30 pF

AC Electrical Characteristics - PCM Port $\overline{\text{PCMFP}}$ and Output Clocks (TDM Master)[†] (continued)

	Characteristic	Sym.	Min.	Typ.[‡]	Max.	Units	Notes
5	PCM_CLKo Output High Time	t_{CKHO}				ns	C_L = 30 pF
	PCM_CLKo = 16384 kHz		25		36		
	PCM_CLKo = 8192 kHz		56		66		
	PCM_CLKo = 4096 kHz		117		127		
	PCM_CLKo = 2048 kHz		239		249		
	PCM_CLKo = 1024 kHz		483		493		
	PCM_CLKo = 512 kHz		971		981		
	PCM_CLKo = 256 kHz		1948		1958		
	PCM_CLKo = 128 kHz		3901		3911		
6	PCM_CLKo Output Low Time	t_{CKLO}				ns	C_L = 30 pF
	PCM_CLKo = 16384 kHz		25		36		
	PCM_CLKo = 8192 kHz		56		66		
	PCM_CLKo = 4096 kHz		117		127		
	PCM_CLKo = 2048 kHz		239		249		
	PCM_CLKo = 1024 kHz		483		493		
	PCM_CLKo = 512 kHz		971		981		
	PCM_CLKo = 256 kHz		1948		1958		
	PCM_CLKo = 128 kHz		3901		3911		
7	PCM_CLKo Output Rise/Fall Time	$t_{r/fCKO}$	3		7	ns	C_L = 30 pF

[†] Characteristics are over recommended operating conditions unless otherwise stated.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

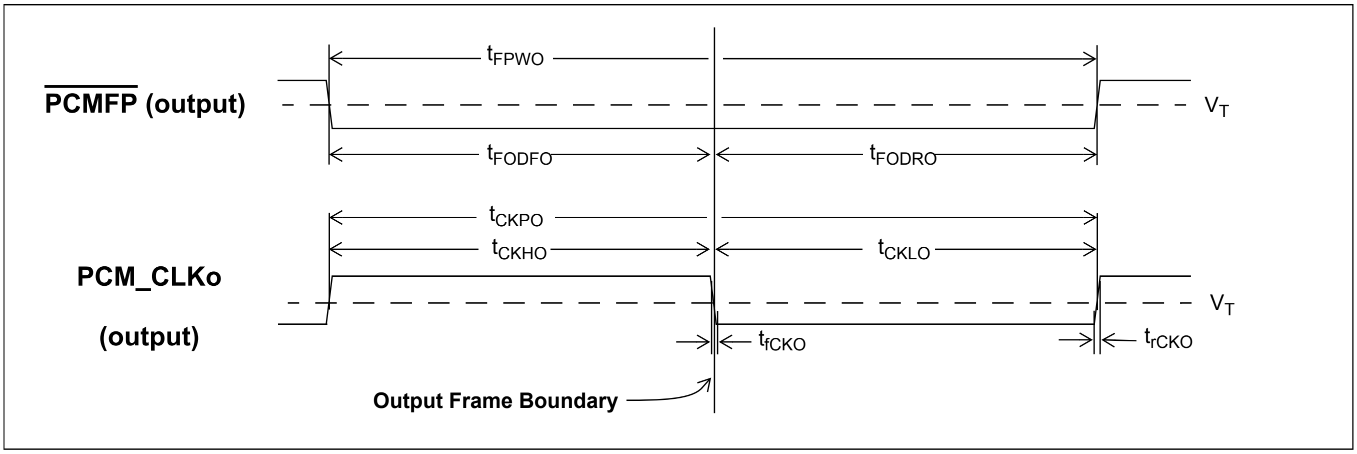


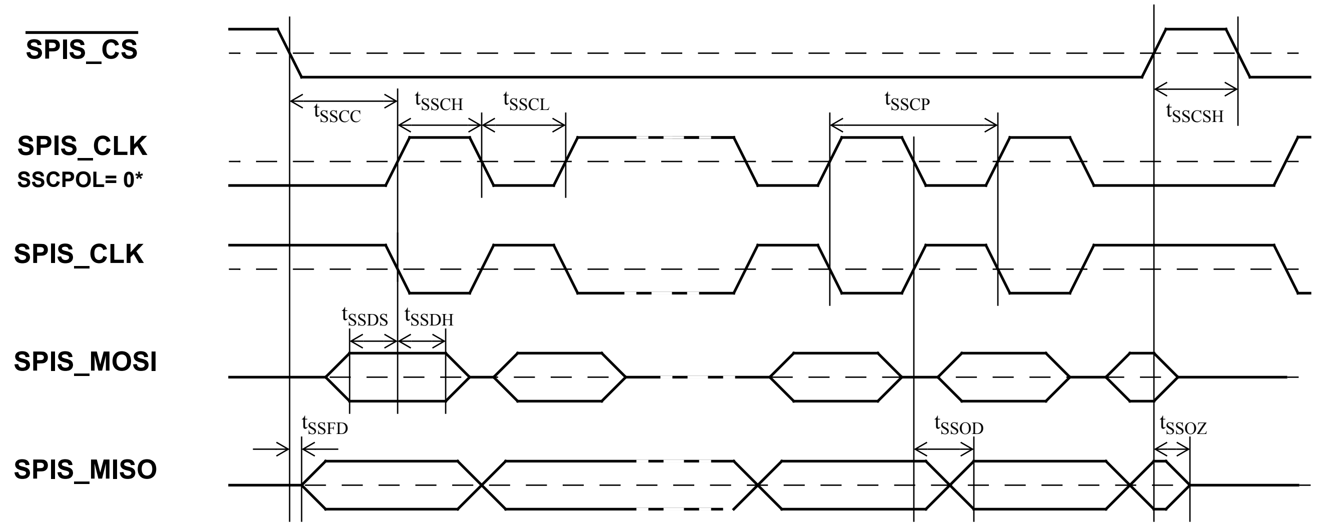
Figure 43 - $\overline{\text{PCMFP}}$ and PCM_CLKo TDM Master Mode Timing

AC Electrical Characteristics - Slave SPI Port Timing (see Figures 44, 45 and 46)†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	SPIS_CLK Clock Period	t_{SSCP}	40			ns	
2	SPIS_CLK Pulse Width High	t_{SSCH}	20	$t_{SSCP}/2$		ns	
3	SPIS_CLK Pulse Width Low	t_{SSCL}	20	$t_{SSCP}/2$		ns	
4	SPIS_MOSI Setup Time	t_{SSDS}	2			ns	
5	SPIS_MOSI Hold Time	t_{SSDH}	5			ns	
6	$\overline{\text{SPIS\_CS}}$ Asserted to SPIS_CLK Sampling Edge	t_{SSCC}	18	$t_{SSCP}/2$		ns	
7	SPIS_SCLK Driving Edge to SPIS_MISO Valid	t_{SSOD}			10	ns	C_L = 30 pF
8	SPIS_SCLK Driving Edge to SPIS_MISO Driven	t_{SSZD}	3		10	ns	C_L = 30 pF
9	$\overline{\text{SPIS\_CS}}$ Falling Edge to SPIS_MISO Driven	t_{SSFD}	3		10	ns	C_L = 30 pF
10	$\overline{\text{SPIS\_CS}}$ De-asserted to SPIS_MISO Tristate	t_{SSOZ}	1		10	ns	C_L = 30 pF
11	$\overline{\text{SPIS\_CS}}$ Pulse High	t_{SSCSH}	20	$t_{SSCP}/2$		ns	

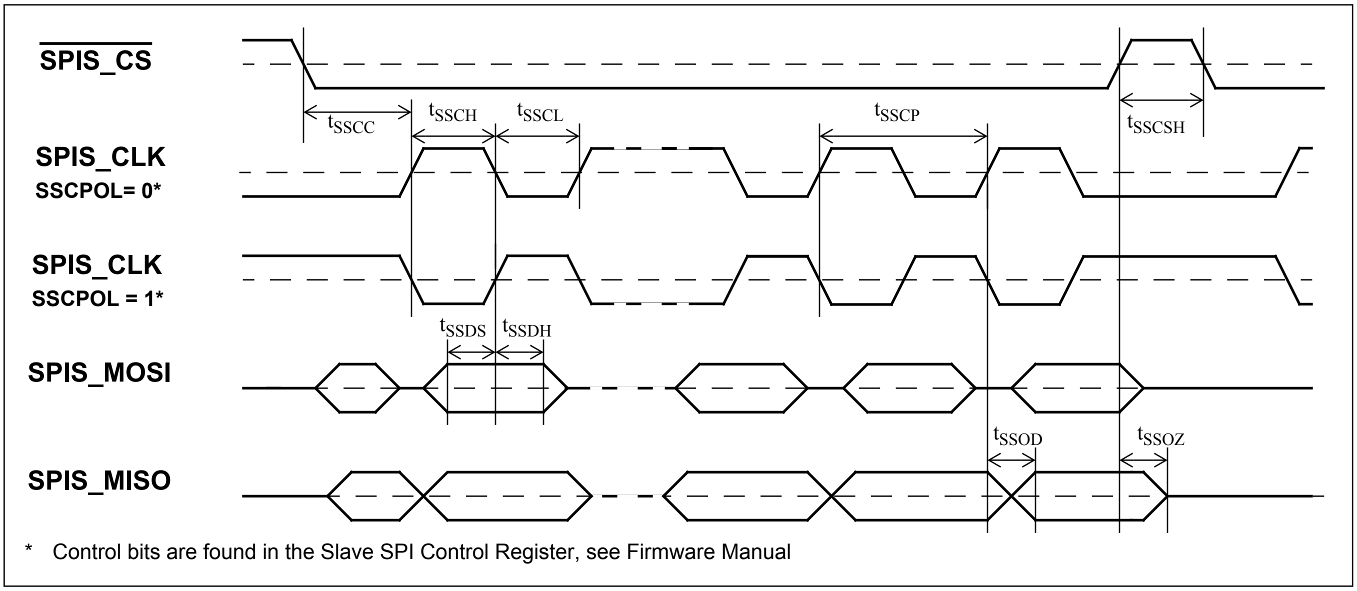
† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



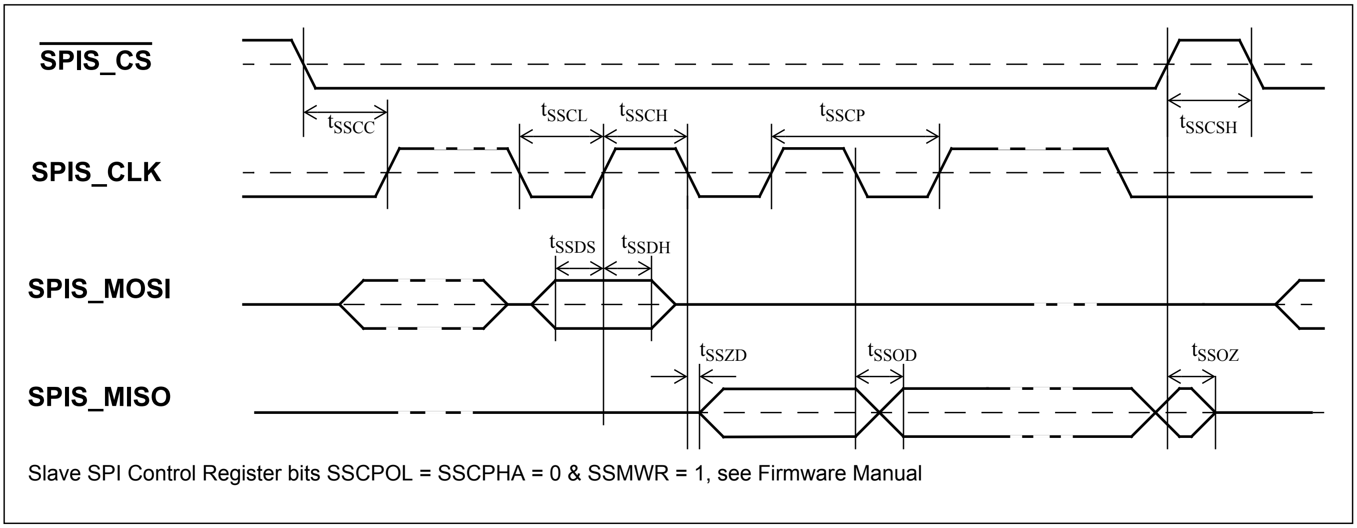
* Control bits are found in the Slave SPI Control Register, see Firmware Manual

Figure 44 - Slave SPI Timing (SSCPHA = 0)



* Control bits are found in the Slave SPI Control Register, see Firmware Manual

Figure 45 - Slave SPI Timing (SSCPHA = 1)



Slave SPI Control Register bits SSCPOL = SSCPHA = 0 & SSMWR = 1, see Firmware Manual

Figure 46 - Slave SPI Timing (Microwire mode)

AC Electrical Characteristics- Master SPI Timing (see Figures 47, 48)†

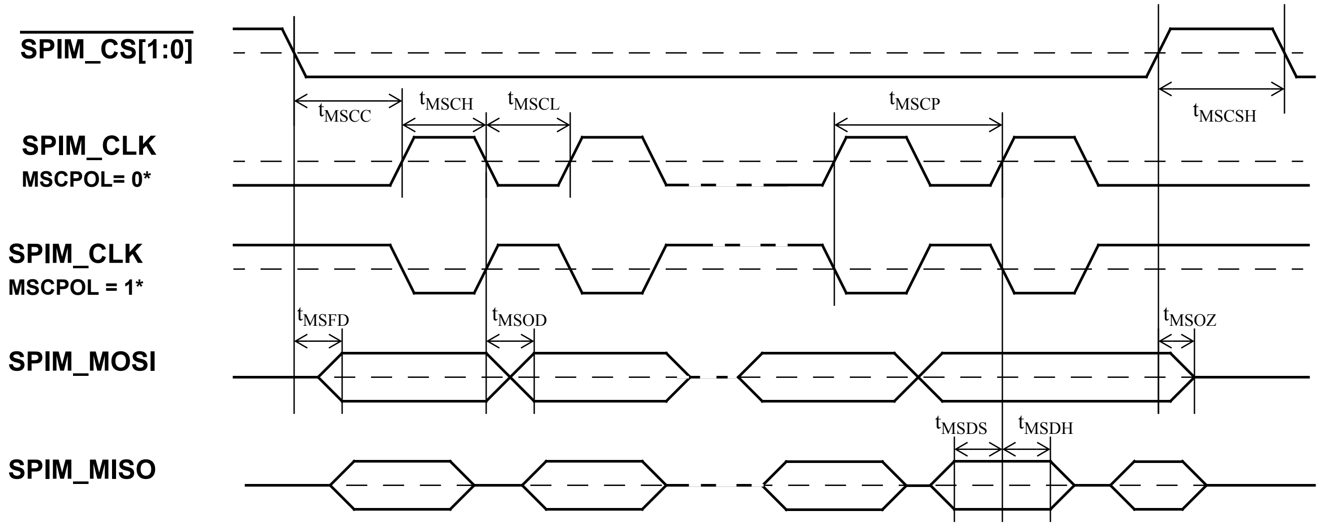
	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	SPIM_CLK Clock Period	t_{MSCP}	40		333344	ns	Max. 25.0 MHz
2	SPIM_CLK Pulse Width High	t_{MSCH}	18		166672	ns	
3	SPIM_CLK Pulse Width Low	t_{MSCL}	18		166672	ns	
4	SPIM_MISO Setup Time	t_{MSDS}	6			ns	
5	SPIM_MISO Hold Time	t_{MSDH}	0			ns	
6	SPIM_CS_B Asserted to SPIM_CLK Sampling Edge	t_{MSCC}	18			ns	
7	SPIM_SCLK Driving Edge to SPIM_MOSI Valid	t_{MSOD}			5	ns	C_L = 30 pF
8	SPIM_CS_B Asserted to SPIM_MOSI Driven	t_{MSFD}	-10		0	ns	C_L = 30 pF
9	SPIM_CS_B De-asserted to SPIM_MOSI high impedance (See Note 2)	t_{MSOZ}	-17		0	ns	C_L = 30 pF
10	$\overline{\text{SPIM\_CS[1:0]}}$ Pulse High (See Note 1)	t_{MSCSH}	18			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

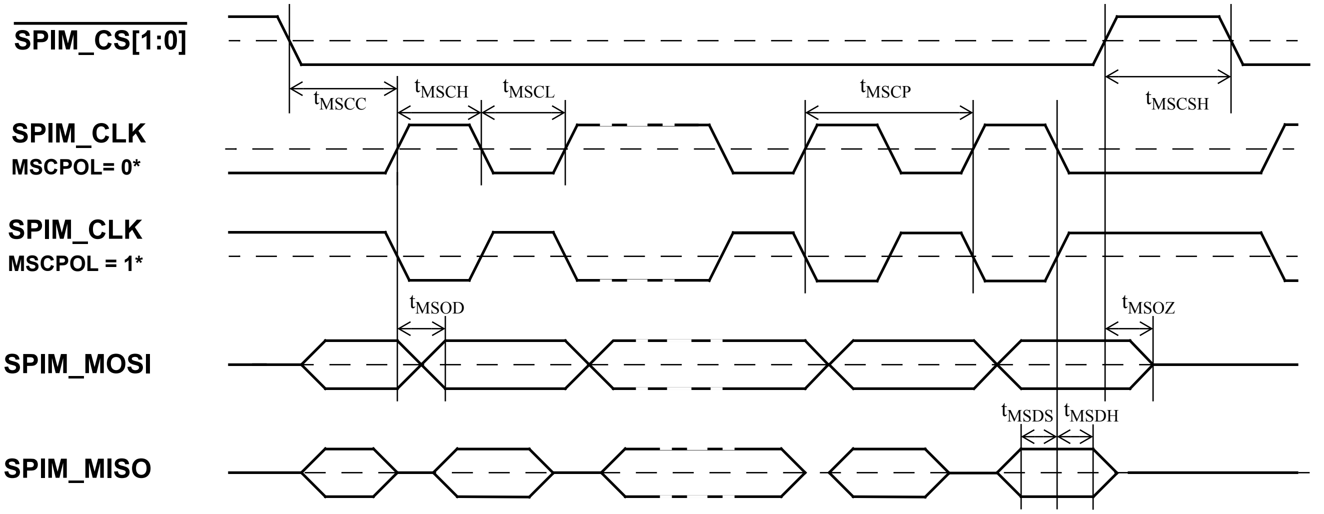
Note 1: The operation of this signal is controlled through the Master SPI Control Register.

Note 2: The minimum duration between the last edge of SPIM_CLK before $\overline{\text{SPIM\_CS[1:0]}}$ becomes inactive and SPIM_MOSI becoming high impedance is 18 ns.



* Control bits are found in the Master SPI Control Register, see Firmware Manual

Figure 47 - Master SPI Timing (MSCPHA = 0)



* Control bits are found in the Master SPI Control Register, see Firmware Manual

Figure 48 - Master SPI Timing (MSCPHA = 1)

AC Electrical Characteristics - Slave I^2S Timing†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes/Conditions
1	I^2S_SCK Clock Period (Note1) f_s = 48 kHz f_s = 8 kHz	t_{ISSCP}		651.04 3.91		ns µs	1/(32 x f_S)
2	I^2S_SCK Pulse Width High f_s = 48 kHz f_s = 8 kHz	t_{ISSCH}	292.97 1.76		358.07 2.15	ns µs	0.45/(32 x f_S) 0.55/(32 x f_S)
3	I^2S_SCK Pulse Width Low f_s = 48 kHz f_s = 8 kHz	t_{ISSCL}	292.97 1.76		358.07 2.15	ns µs	0.45/(32 x f_S) 0.55/(32 x f_S)
4	I^2S_SDi Setup Time	t_{ISDS}	2			ns	
5	I^2S_SDo (input) Setup Time (2 Dual Analog-to-Digital Converters)	t_{ISDS}	2			ns	See Figure 20
6	I^2S_LRCK Setup Time	t_{ISDS}	2			ns	
7	I^2S_SDi Hold Time	t_{ISDH}	5			ns	
8	I^2S_SDo (input) Hold Time (2 Dual Analog-to-Digital Converters)	t_{ISDH}	5			ns	See Figure 20
9	I^2S_LRCK Hold Time	t_{ISDH}	5			ns	
10	I^2S_SCK Falling Edge to I^2S_SDi/o (output) Valid (2 Dual CODECs)	t_{ISOD}	3		17	ns	C_L = 30 pF See Figure 18

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: I^2S_SCK frequency is 32 x f_S, where f_S is the sampling frequency of the external converter.

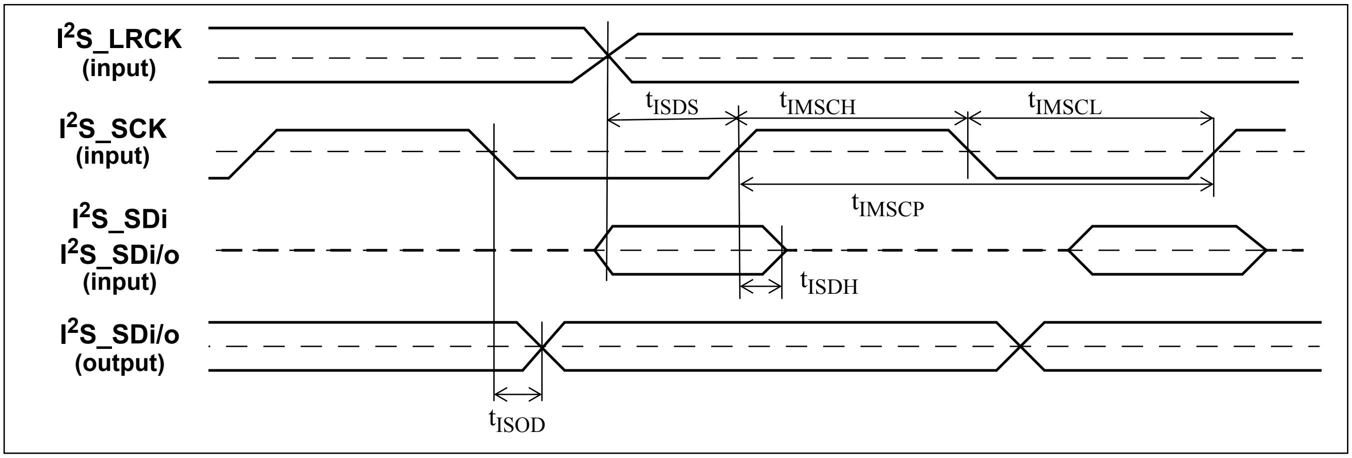


Figure 49 - Slave I^2S Timing

AC Electrical Characteristics - Master I^2S Timing †

	Characteristics		Sym.	Min.	Typ. ‡	Max.	Units	Notes/Conditions
1	I^2S_MCLK Clock Period (Note 1)	f_s = 48 kHz f_s = 8 kHz	t_{IMMCP}		81.38 488.28		ns ns	1/(256 x f_S)
2	I^2S_MCLK Pulse Width High	f_s = 48 kHz f_s = 8 kHz	t_{IMMCH}	33.2 236.6		48.2 251.6	ns ns	(0.5/(256 x f_S)) - 7.5 (0.5/(256 x f_S)) + 7.5
3	I^2S_MCLK Pulse Width Low	f_s = 48 kHz f_s = 8 kHz	t_{IMMCL}	33.2 236.6		48.2 251.6	ns ns	(0.5/(256 x f_S)) - 7.5 (0.5/(256 x f_S)) + 7.5
4	I^2S_SCK Clock Period (Note 2)	f_s = 48 kHz f_s = 8 kHz	t_{IMSCP}		651.04 3.91		ns µs	1/(32 x f_S)
5	I^2S_SCK Pulse Width High	f_s = 48 kHz f_s = 8 kHz	t_{IMSCH}	318.0 1.95		333.0 1.96	ns µs	(0.5/(32 x f_S)) - 7.5 (0.5/(32 x f_S)) + 7.5
6	I^2S_SCK Pulse Width Low	f_s = 48 kHz f_s = 8 kHz	t_{IMSCL}	318.0 1.95		333.0 1.96	ns µs	(0.5/(32 x f_S)) - 7.5 (0.5/(32 x f_S)) + 7.5
7	I^2S_SDi Setup Time		t_{IMDS}	9			ns	
8	I^2S_SDo (input) Setup Time (2 Dual Analog-to-Digital Converters)		t_{IMDS}	9			ns	See Figure 20
9	I^2S_SDi Hold Time		t_{IMDH}	0			ns	
10	I^2S_SDo (input) Hold Time (2 Dual Analog-to-Digital Converters)		t_{IMDH}	0			ns	See Figure 20
11	I^2S_SCK falling to Edge to I^2S_LRCK		t_{IMOD}	-7.5		7.5	ns	C_L = 30 pF
12	I^2S_SCK Falling Edge to I^2S_SDi/o (output) Valid (2 Dual CODECs)		t_{IMOD}	-7.5		7.5	ns	C_L = 30 pF See Figure 18

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note 1: I^2S_MCLK frequency is 256 x f_S, where f_S is the sampling frequency of the external converter.

Note 2: I^2S_SCK frequency is 32 x f_S, where f_S is the sampling frequency of the external converter.

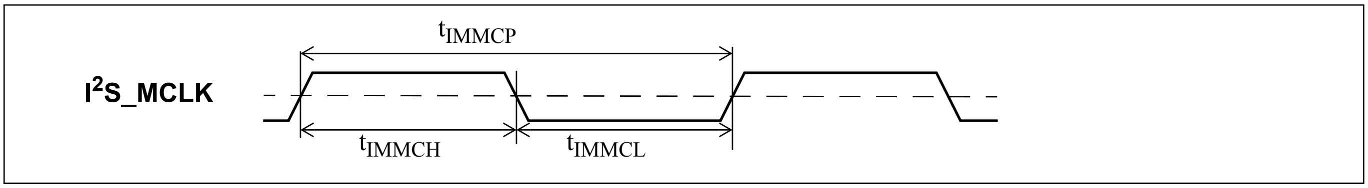


Figure 50 - I^2S Master Clock (MCLK) Timing

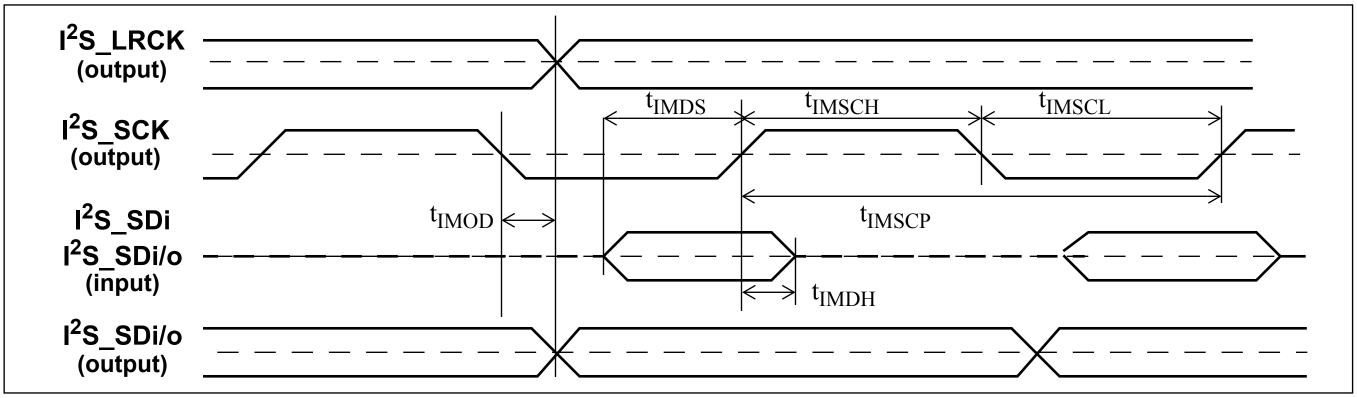


Figure 51 - Master I^2S Timing

AC Electrical Characteristics - UART Timing †

	Characteristics	Sym.	Min.	Typ. ‡	Max.	Units	Notes/Conditions
1	UART_Rx and UART_Tx bit width Baud rate = 9600 bps Baud rate = 115.2 kbps	t_{UP}		 104.17 8.68		 µs µs	
2	Time between two consecutive UART_Rx accesses	t_{UIA}	0				All baud rates

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

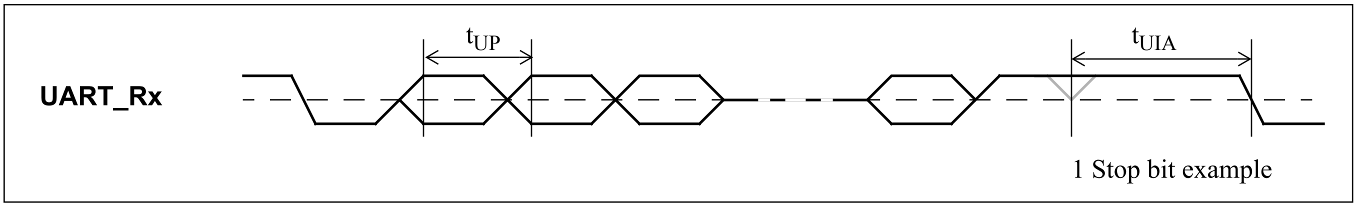


Figure 52 - UART_Rx Timing

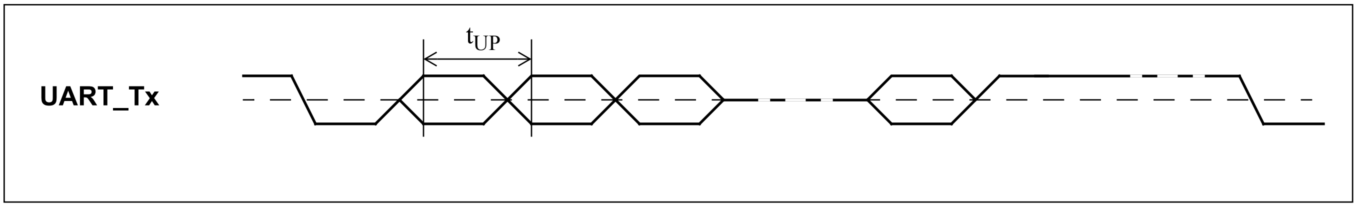


Figure 53 - UART_Tx Timing

8.0 Applications

8.1 Power Supply

8.1.1 Power Sequencing

The ZL38012 requires external latch-up protection between the V_{DD}IO and V_{DD}CORE supplies. That is, the V_{DD}CORE voltage must not exceed V_{DD}IO voltage during power up and power down. Figure 54 illustrates two options (A & B) to meet this requirement. Option A uses a Schottky diode forward biased between V_{DD}1V2 (V_{DD}CORE) and V_{DD}IO. This ensures that the core voltage will never exceed the IO voltage by more than a few hundred millivolts, which is sufficient to meet the ZL38012 latch-up requirement.

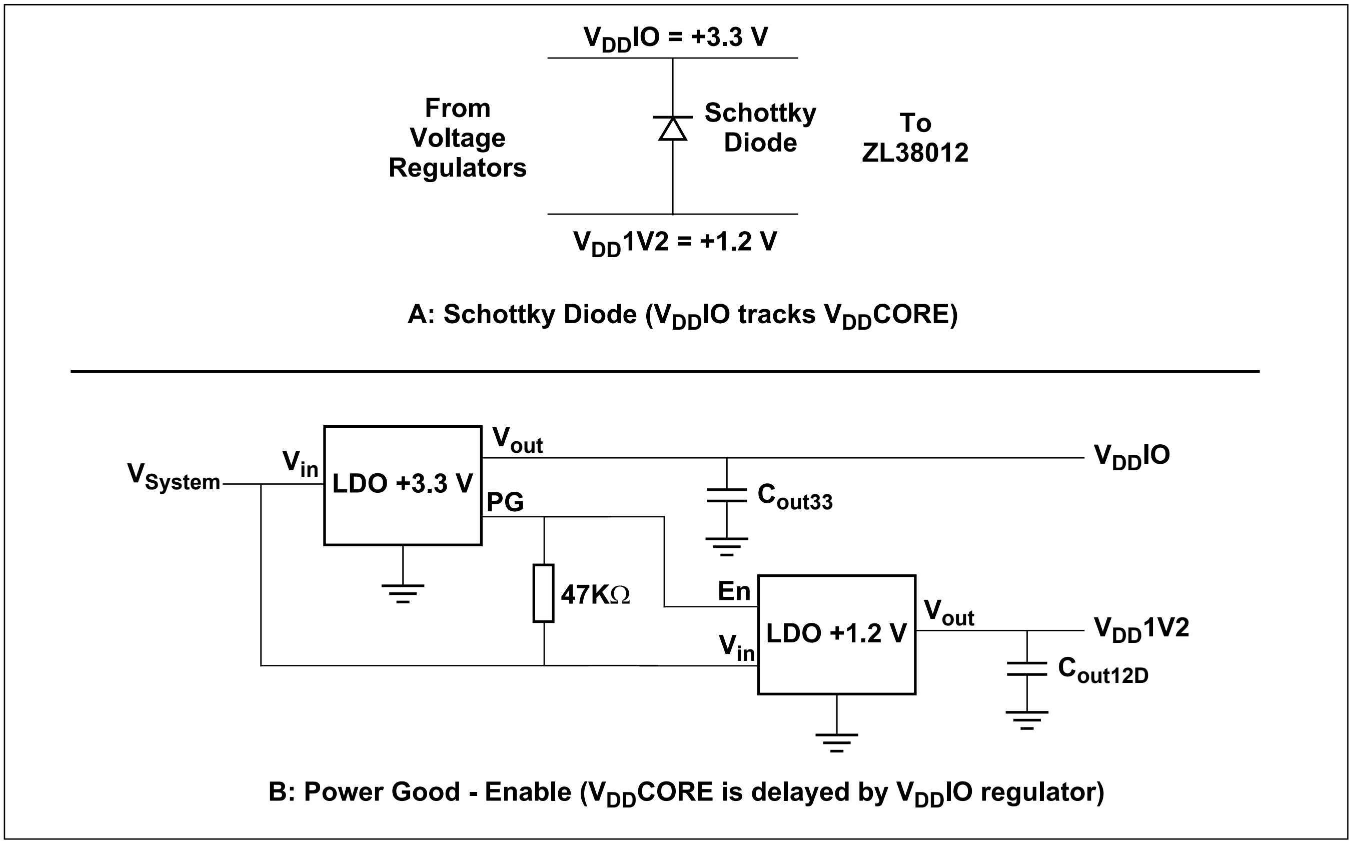


Figure 54 - Latch-Up Prevention Circuit Options

Option B uses the Power Good (PG) output of the +3.3 V LDO regulator to enable the +1.2 V LDO regulator. During power up the PG signal will not enable the +1.2 V regulator until V_{DD}IO reaches almost full nominal value (i.e., $V_{OnThreshold}$ = 80 to 100% of nominal voltage depending on the devices selected) plus a turn-on delay. During power down the PG signal will turn off the +1.2 V regulator when V_{DD}IO drops below its $V_{OffThreshold}$ plus a turn-off delay.

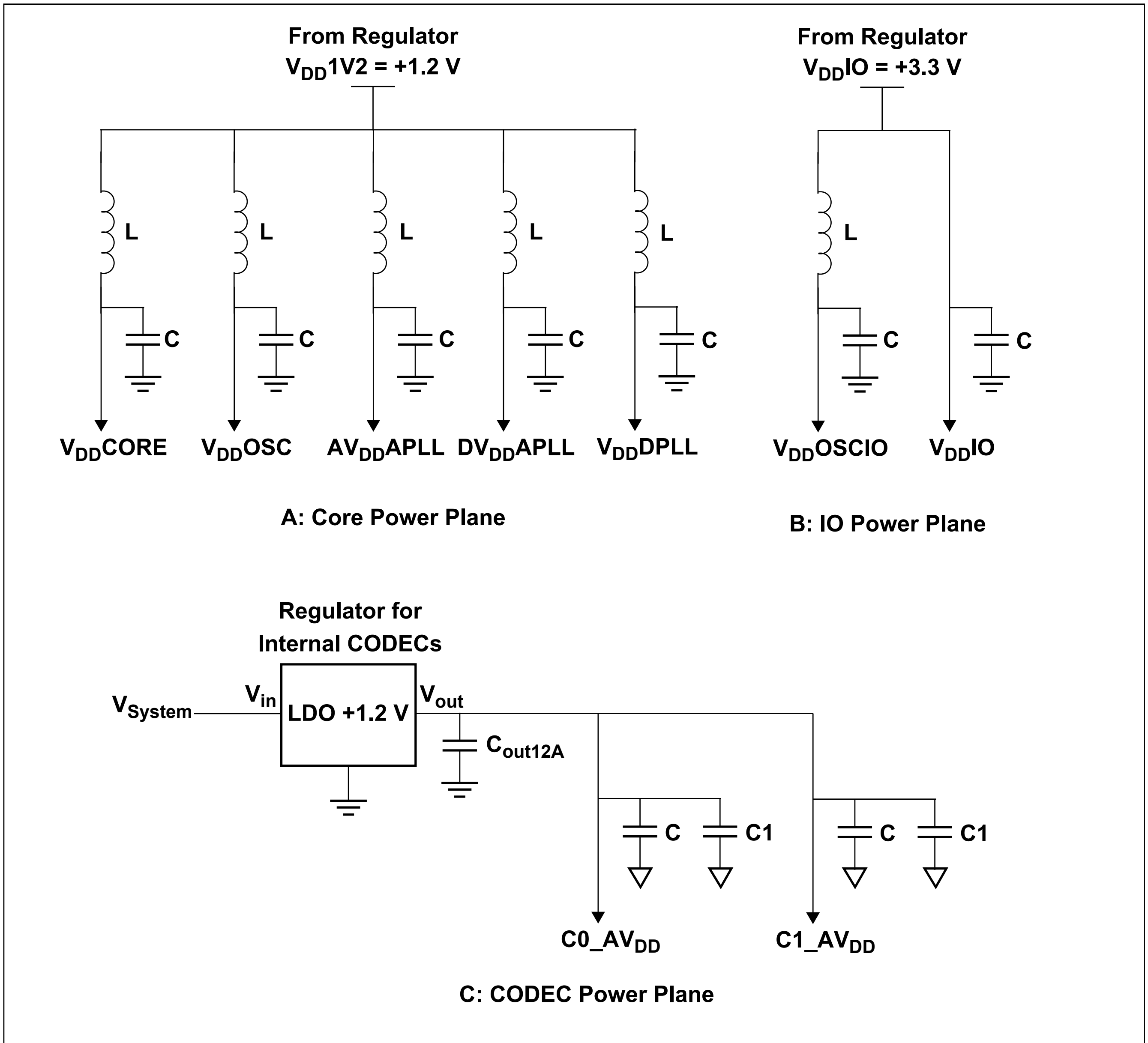
There are no latch-up requirements for power sequencing between the +3.3 V IO or +1.2 V Core and +1.2 V Analog supplies.

8.1.2 Supply Isolation

An ZL38012 application should be designed with three separate isolated power planes as shown in Figure 55 (i.e., A: Core Power Plane; B: IO Power Plane; and C: CODEC Power Plane). Isolation is provided through separate voltage regulators that supply each plane, see also Figure 54. Each one of the Core supply pins (V_{DD}CORE, V_{DD}OSC, AV_{DD}APLL, DV_{DD}APLL and V_{DD}DPLL) are further isolated from each other using inductors (L). The V_{DD}OSCIO of the +3.3 V plane is isolated from the other IO supply pins using an inductor L as well.

The capacitors C are 0.1 μF ceramic decoupling capacitors, which should be placed as close as possible to the V_{DD} pins to minimize impedance from V_{DD} to V_{SS}. Capacitors C1 are 1.0 μF ceramic bypass capacitors. The value of Cout12A and additional capacitors from V_{System} to system ground are to be selected based on the system design requirements and selected voltage regulator stability requirements. Figure 55 also shows an example component number and manufacturer for L.

It should be noted that the isolation illustrated in Figure 55 may not be necessary for all applications. It is presented here as good engineering practice and a place to start. Also, the ground symbols used in Figure 55 should not be interpreted to mean that separate analog and digital ground planes are required for the ZL38012. A single (analog and digital) ground plan is adequate for the vast majority of applications. This is the case as long as the ground plane is homogeneous so that relatively large ground return currents are not forced through narrow channels.



L = BLM31PG601SN1 (μRata)
C = 0.1 μF (place as close as possible to V_{DD} pin for minimum Z between V_{DD} and V_{SS})
C1 = 1.0 μF

Figure 55 - Power Supply Isolation

8.2 External Clock Requirements

In all modes of operation the ZL38012 requires an external clock source for the APLL, which is the source for internal timing signals including the 100 MHz MCLK. This external clock source may be either a crystal, crystal oscillator with a CMOS output or an external clock signal. The frequency of the APLL clock source may be any of the following: 2048, 4096, 8192, 12288, 16384, 20000, 24576 or 25000 kHz.

The accuracy of the external clock source is not critical for voice processing applications.

8.2.1 Crystal Oscillator Specification

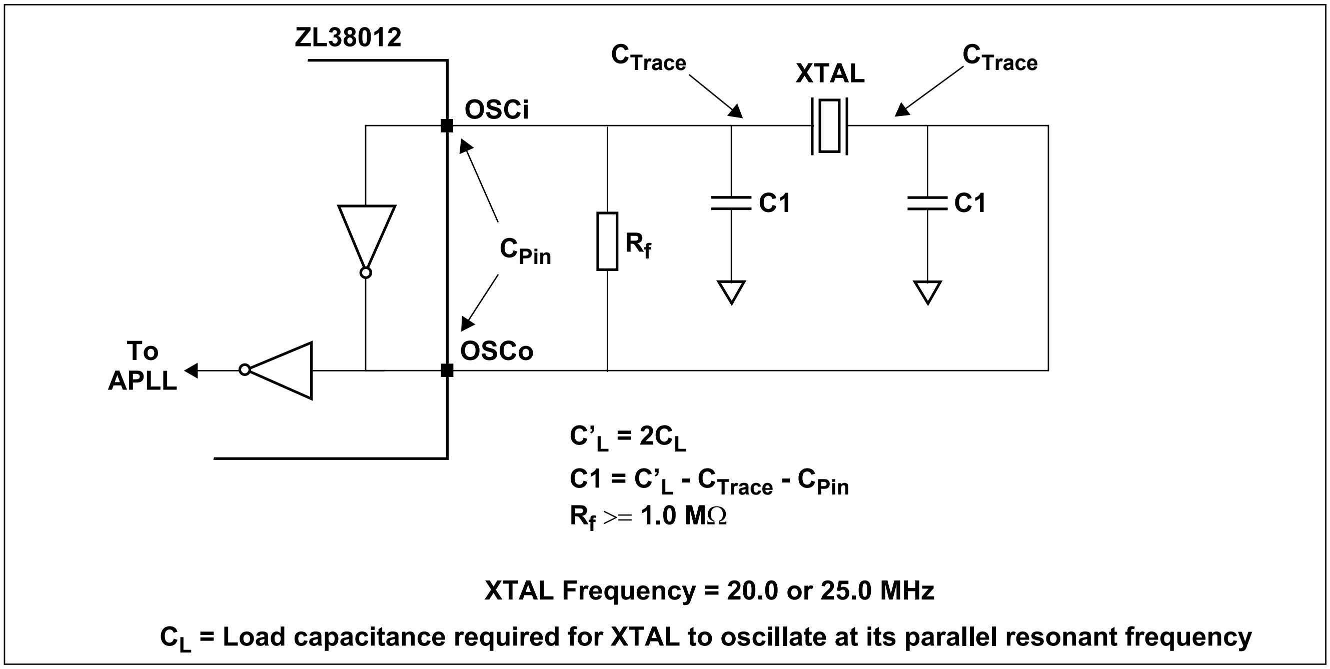


Figure 56 - Crystal Application Circuit

The oscillator circuit that is created across pins OSCi and OSCo requires an external fundamental mode crystal that has a specified parallel resonance at one of the XTAL frequencies listed in Figure 56 with a load capacitance of C_L. Every oscillator circuit requires positive feedback (around 360 degrees of phase difference from output to input) to ensure that oscillations can build in the system. Every crystal has both a series and parallel resonance frequency of operation. The series resonant frequency (f_S) is determined from the motion parameters (L_m, C_m & R_m) of the crystal to be when $XL_m = -XC_m$ resulting in a purely resistive circuit R_m and no phase change added to the circuit. Parallel resonance (f_P) is based on the series motion parameters Lm and Cm in parallel with Co. Co is the capacitance formed by the crystal, its mounting and lead interface. The effective value of Co must include the external capacitance in the circuit (C_L, C_{Pin} and C_{Trace}), which are illustrated in Figure 56. This is why parallel resonant crystals are always specified to operate at a specific F_P with a specific load. If the load changes f_P will be pulled off its intended frequency. Crystal manufacturers can provide data that will indicate the frequency deviation per pF of capacitance (ppm/pF) away from the ideal C_L for specific crystals.

Another effect of parallel resonance is a 90 degree phase shift. Therefore, the total phase shift in the circuit of Figure 56 is 180 degrees (inverter) + 90 degrees (parallel resonance) + 90 degrees (Load Capacitance C_L) = 360 degrees, which meets a basic requirement for oscillation.

Capacitors C1 in Figure 56 along with C_{Trace} and C_{Pin} make up the total load capacitance that the crystal will see. The two C1 capacitors are actually in series with the with Co of the crystal so the required load capacitance $C_L = (C'_L \times C'_L)/(C'_L + C'_L)$ or $C'_L = 2C_L$. C_{Trace} and C_{Pin} are in parallel with C1 so they will reduce the required value of $C1 = C'_L - C_{Trace} - C_{Pin}$.

For example, if a crystal is selected that has a parallel resonance of 20.0 MHz with a C_L = 20.0 pF, then assuming typical values of C_{Pin} = 3.0 pf and C_{Trace} = 1.0 pf the following can be calculated:

C'L = 2CL = 2 x 20.0 = 40.0 pF;

$C1 = C'_L - C_{Trace} - C_{Pin}$ = 40.0 - 3.0 - 1.0 = 36.0 pF;

Therefore: C1 = 36.0 pF.

The feedback resistor (R_f) biases the internal inverter in a high gain region, which ensure that there is a 180 degree phase difference between its input and output immediately after power up. An R_f = 1.0 MΩ is normally adequate.

It is important to make sure that the maximum drive level (crystal power dissipation) specified in the crystal design manual is not exceeded in the application circuit. Excessive power dissipation may result in unstable operation, accelerated aging rates and crystal failure. The crystal power dissipation (P_D) can be determined from the equation PD = $Irms^2$ x R*m*, where a current probe is used to measure the Irms through the crystal during oscillation. An alternate method is to temporarily insert a sequence of resistors in series with the crystal until half the Vrms to ground, when the circuit is oscillating, is dropped across the resistor. The selected resistor value and voltage drop across it can be used to calculate the power that is being dissipated in the crystal ($P_D = 2Vrms^2/R$). Values of R*m* normally range from 20 to 400 Ω.

Table 22 shows some crystals that may be used with the ZL38012.

20.0 MHz	Fox Electronics: FOXSD/200-20, ±50 ppm absolute, ±50 ppm (-10°C to +70°C), 20 pf, 32 Ω, 0.5 mW, HC49SD SMT holder.
25.0 MHz	Ecliptec: EC3SM-25.000M

Table 22 - Recommended Crystals

8.2.2 Clock Oscillator

Figure 57 below illustrates the circuit that is used when the ZL38012 external clock source is a crystal oscillator. The output of the oscillator must be buffered to provide a nominal 3.3 V clock high signal relative to V_{SS} at OSCi (V_{IH} min = 2.0 V & V_{IL} max = 0.8 V), see DC Electrical Characteristics. Table 23 shows some crystal oscillators that may be used with the ZL38012.

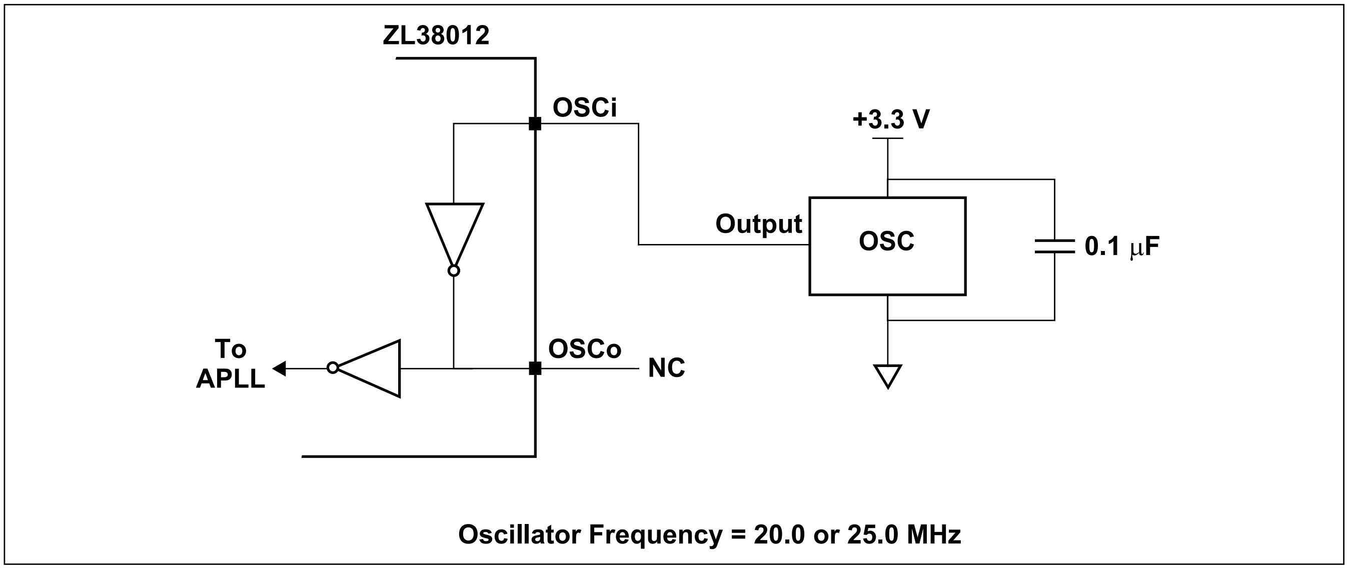


Figure 57 - Crystal Oscillator Application Circuit

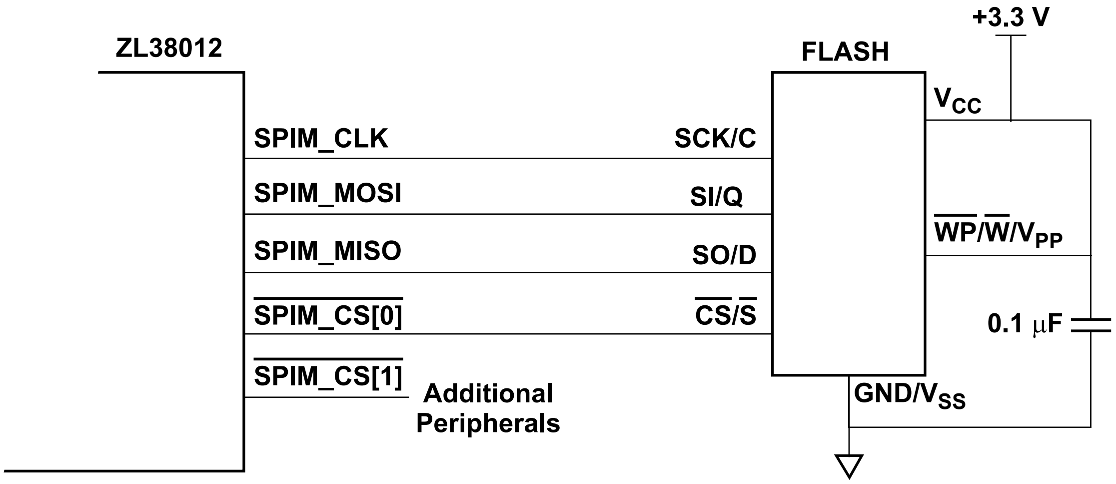
20.0 MHz	Raltron: COM2303-20.000, ±30 ppm (-10°C to +70°C), 10 ns rise and fall times, 40% to 60% duty cycle.
	CTS: CTS 03-41399-008 OXCO 20 MHz, ±4.6 ppm (-40°C to +85°C) for unit life, 40% to 60% duty cycle.

Table 23 - Recommended Crystal Oscillators

8.3 FLASH Specification

After power-up the ZL38012 will run its resident boot code, which establishes the initial setup of the Master SPI port and then downloads the firmware from external FLASH memory. This FLASH firmware establishes the modes of the of all the ZL38012 ports and then installs the resident application.

Figure 58 illustrates the connection of FLASH memory to the ZL38012 Master SPI port. The Master SPI port has two chip selects, which allows it to communication with two separate peripheral devices. This supports operations such as periodic code upgrades i.e., normally loads code from FLASH, but upgrades are from external port and then new code is down-loaded to FLASH.



FLASH

ATMEL AT25F4096 - SCK, SO, SI, $\overline{CS}$ & $\overline{WP}$ - CPOL = CPHA = 0

STMicroelectronics M25P32 - C, D, Q, $\overline{S}$ & $\overline{W}/V_{PP}$ - CPOL = CPHA = 0 or 1

Figure 58 - FLASH Interface Circuit

Table 24 shows the basic FLASH memory requirements. The read instruction requirement is necessary as this is the command that the ROM boot code will use initially to read data from external FLASH.

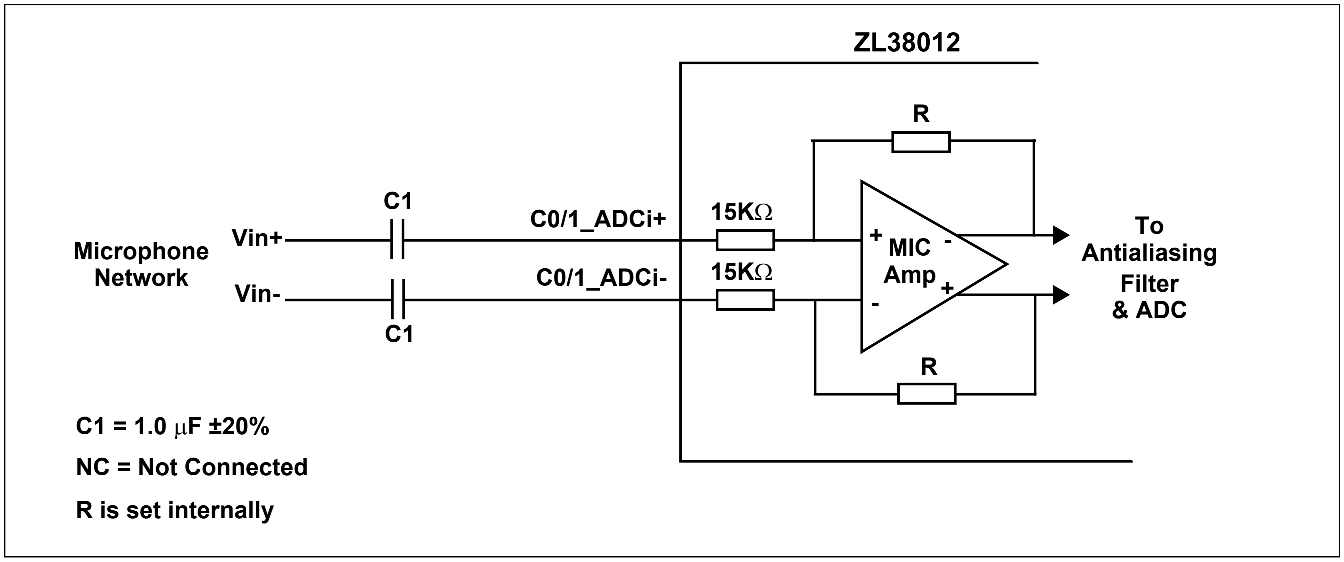
Read Instruction Code (Boot Requirement)	0000 0011
Clock Frequency Range	780 to 50000 kHz
Fast Read Mode	Not supported
Tested Devices	STMicroelectronicsM25P05-A (512 Kbits)
	STMicroelectronicsM25P10-A (1 Mbits)
	STMicroelectronics M25P32 (32 Mbits)
	STMicroelectronicsM25P64(64 Mbits)
	Atmel AT25F512A (512 Kbits)
	Atmel AT25F1024A (1 Mbits)
	Atmel AT25F4096 (4 Mbits)
	Winbond W25X10 (1 Mbits)

Table 24 - External FLASH Memory Requirements

8.4 Internal CODEC Interface

8.4.1 CODEC Microphone Amplifier ADC Circuit

When a ZL38012 internal CODEC ADC input buffer is configured as a differential microphone amplifier it must be AC coupled as shown in Figure 59. The input impedance of the is 15 KΩ.



C1 = 1.0 µF ±20%

NC = Not Connected

R is set internally

Figure 59 - CODEC 0/1 ADC Differential Microphone Amplifier Circuit

The Microphone Amplifier may also be configured for a single ended input by connecting Vin+ in Figure 59 to analog ground and Vin- to the single ended output of the previous stage.

8.4.2 CODEC DAC Driver Circuit

The minimum load impedance of the DAC differential output driver is 10 KΩ. C1 and R_L have been selected to implement a low pass filter with an acceptable corner frequency. The alternative component values have been selected as an example that will maintain both the load and low pass corner frequency requirements.

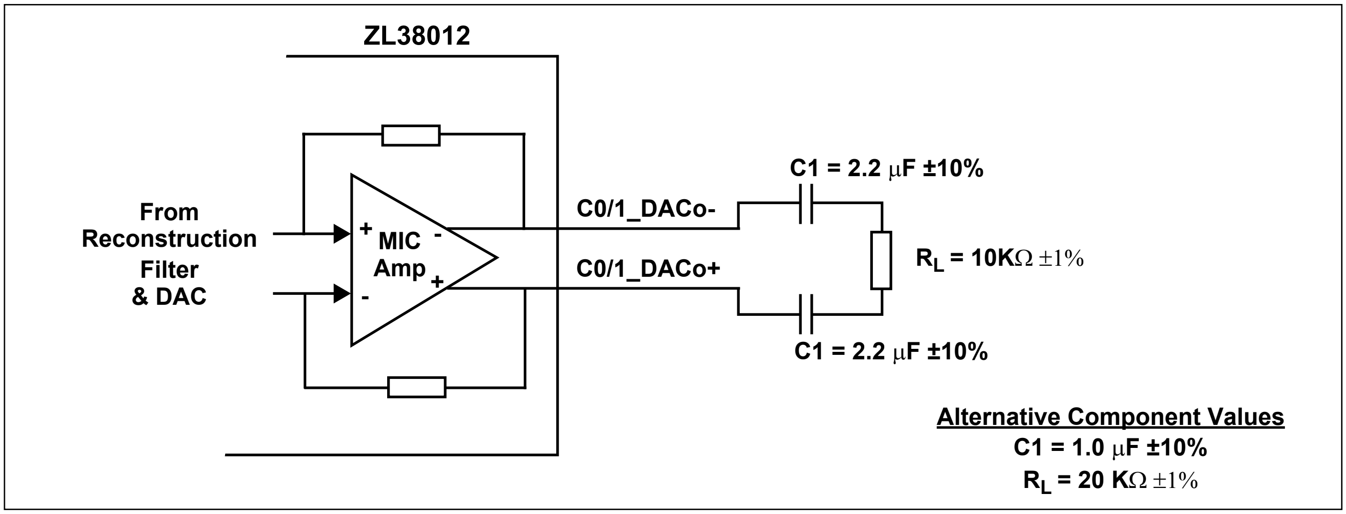


Figure 60 - CODEC 0/1 DAC Differential Driver Circuit

The minimum load impedance of the DAC differential output driver is 10 KΩ. This is maintained when interfacing to a single ended stage by splitting the impedance between the + and - outputs as shown in Figure 61 (i.e., 5 KΩ to ground for each output). If C is the same as in the differential circuit, Figure 60, R must be a minimum of 7.5 KΩ to maintain the same low pass cutoff frequency and load impedance. R = 7.5 KΩ, not 5 KΩ, because the voltage divider on the + input of the single ended stage creates a bias voltage on the - input of the single ended stage that will make the effective value of R = 0.67R. Therefore, R is increased to R/0.67 to compensate for this effect. Figure 61 also shows alternative components that have been selected to maintain the load impedance and low pass cutoff frequency requirements.

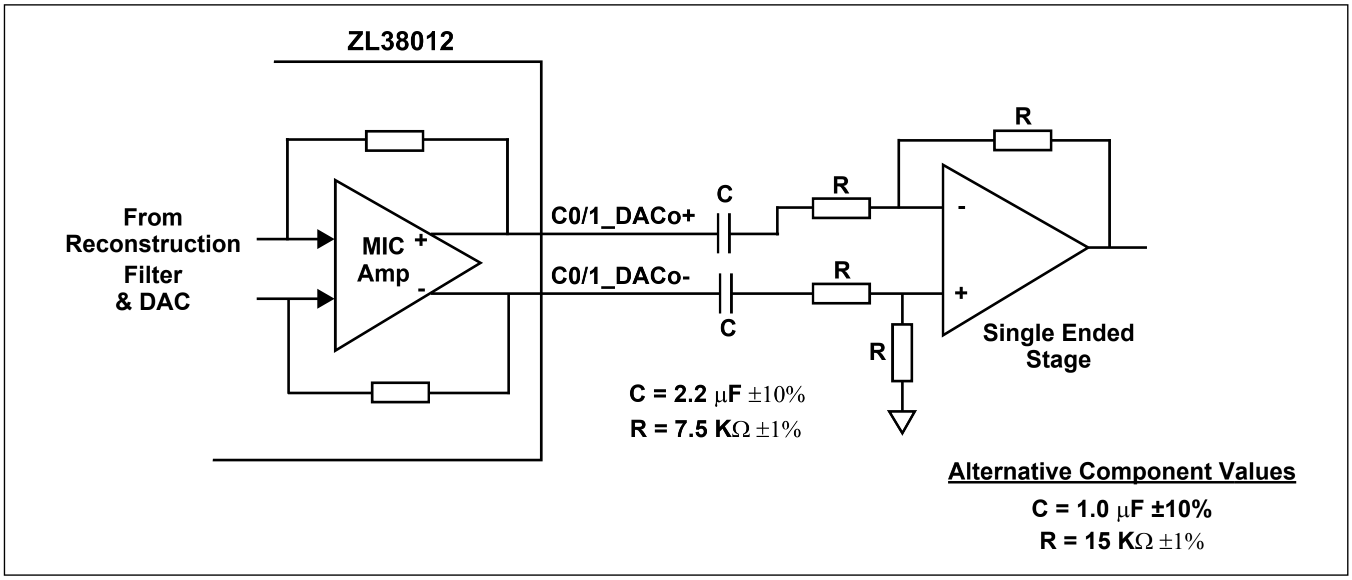


Figure 61 - CODEC 0/1 DAC Single Ended Driver Circuit

8.4.3 CODEC Bias Circuit

The common mode bias voltage output signal (BIAS_VCM) for the DAC output buffers is to be decoupled through a 0.1 μF ceramic capacitor to analog ground. The + and - ADC reference voltage outputs (BIAS_RF+/-) must be connected together through a 0.1 μF ceramic capacitor. These signals should also be decoupled to ground through 0.1 μF ceramic capacitors as shown in Figure 62.

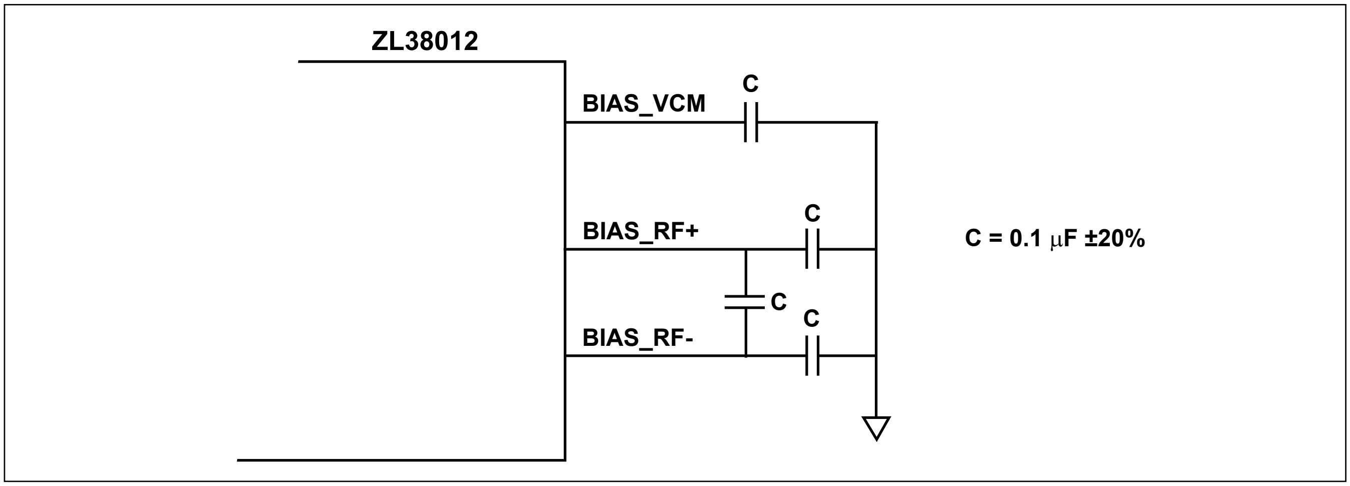


Figure 62 - CODEC 0/1 Bias Circuit

8.5 Host Microprocessor Access Examples

This section presents four examples that illustrate the steps required for an external microprocessor to access the status and control registers of the ZL38012. Figure 63 shows a data write to a register through the Slave SPI port, Figure 64 shows a register read through the Slave SPI port, Figure 65 shows a data write to a register through the UART port, and Figure 66 shows a register read through the UART port.

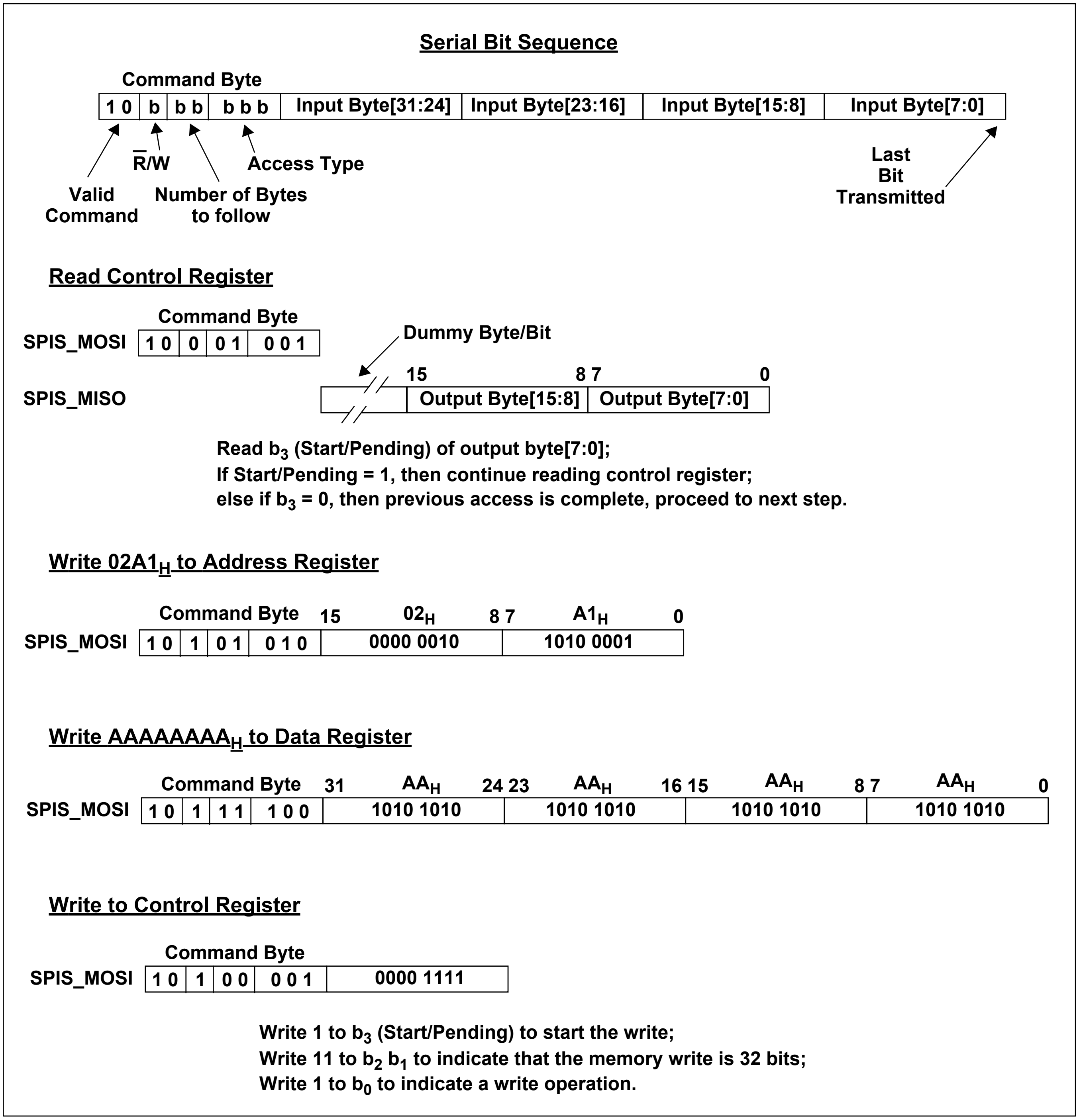
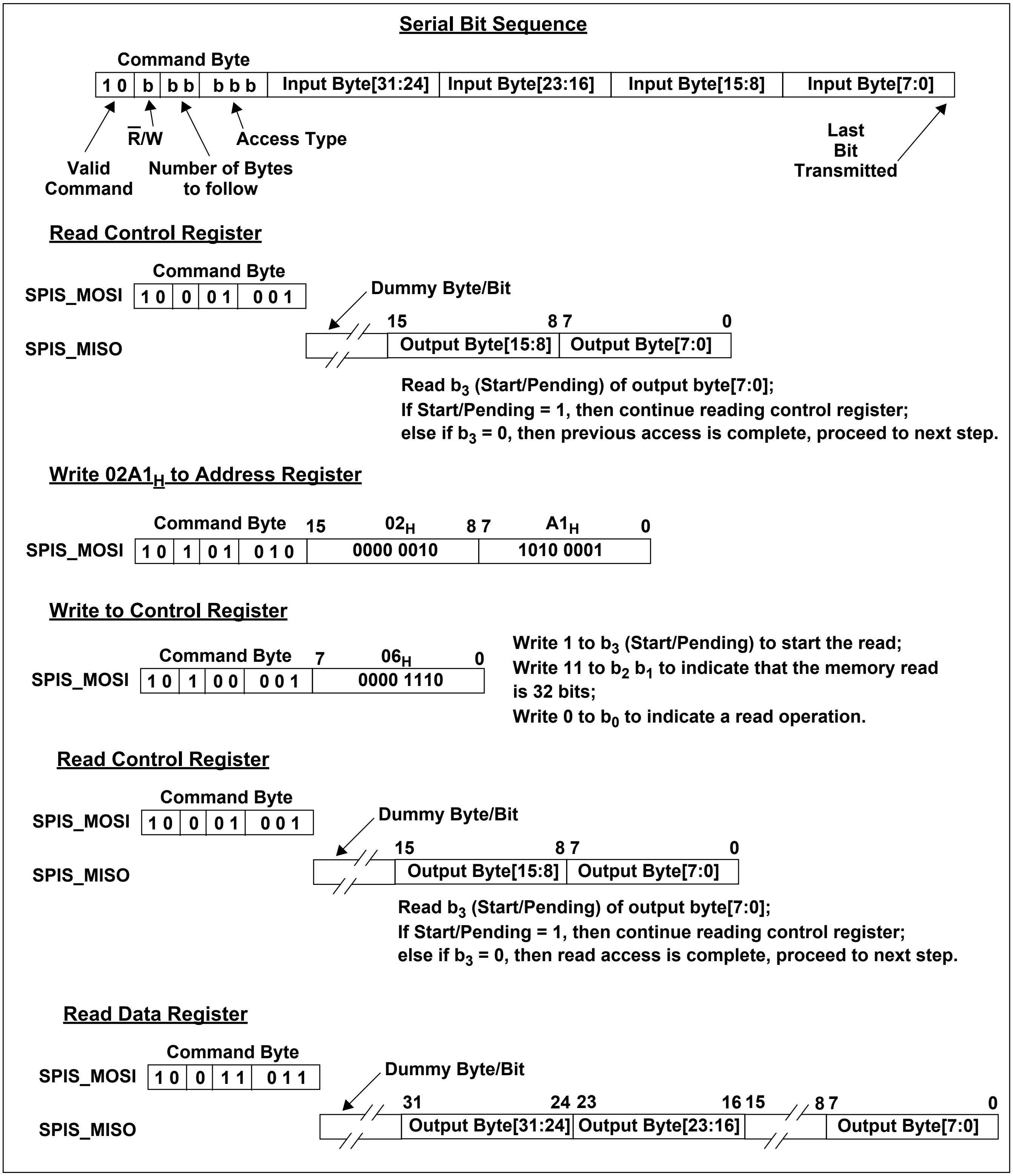


Figure 63 - SSPI Write AAAAAAAA$_H$ to Register Address 02A1$_H$

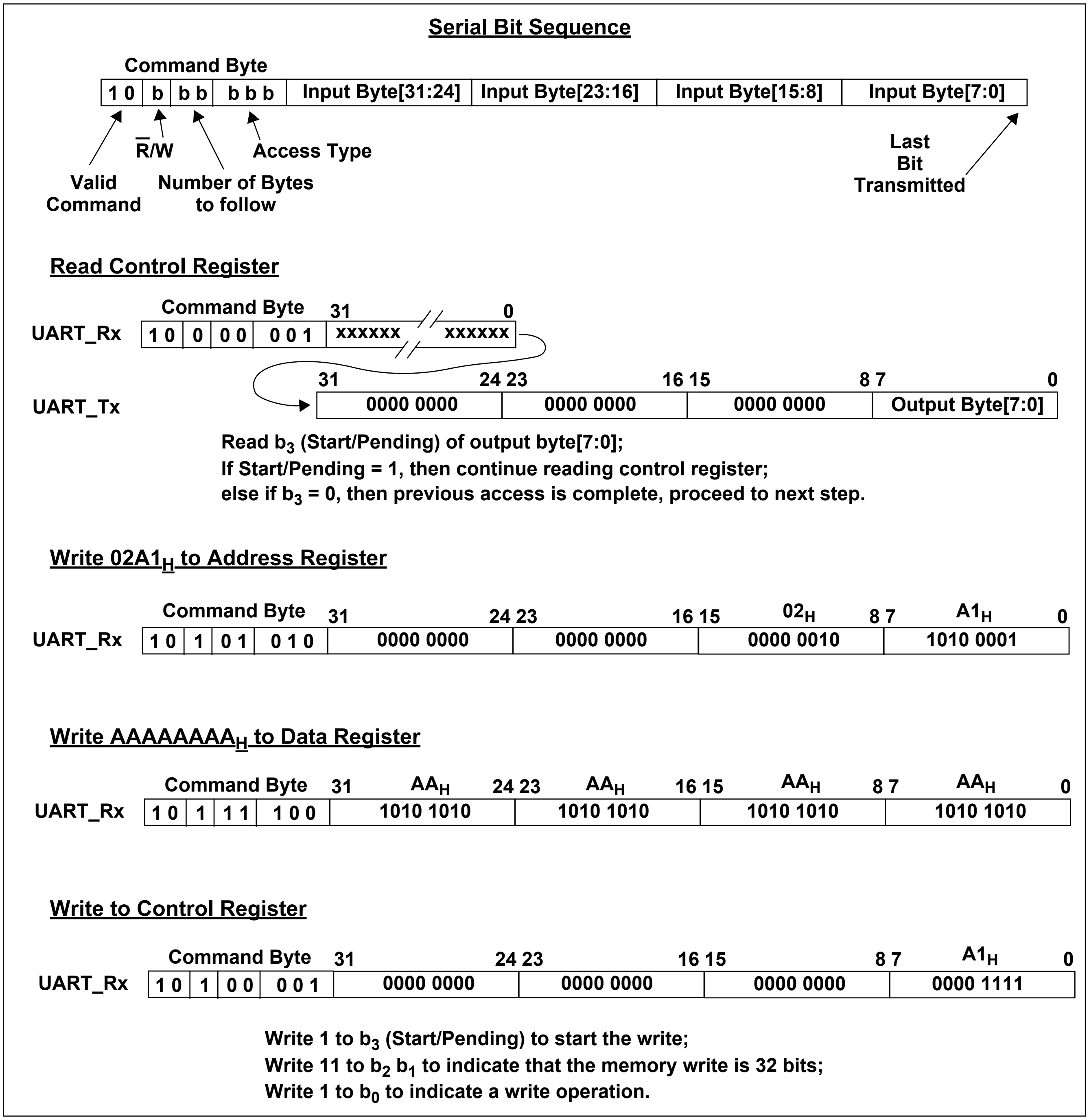


Read b_3 (Start/Pending) of output byte[7:0];
If Start/Pending = 1, then continue reading control register;
else if b_3 = 0, then previous access is complete, proceed to next step.

Write 1 to b_3 (Start/Pending) to start the read;
Write 11 to b_2 b_1 to indicate that the memory read is 32 bits;
Write 0 to b_0 to indicate a read operation.

Read b_3 (Start/Pending) of output byte[7:0];
If Start/Pending = 1, then continue reading control register;
else if b_3 = 0, then read access is complete, proceed to next step.

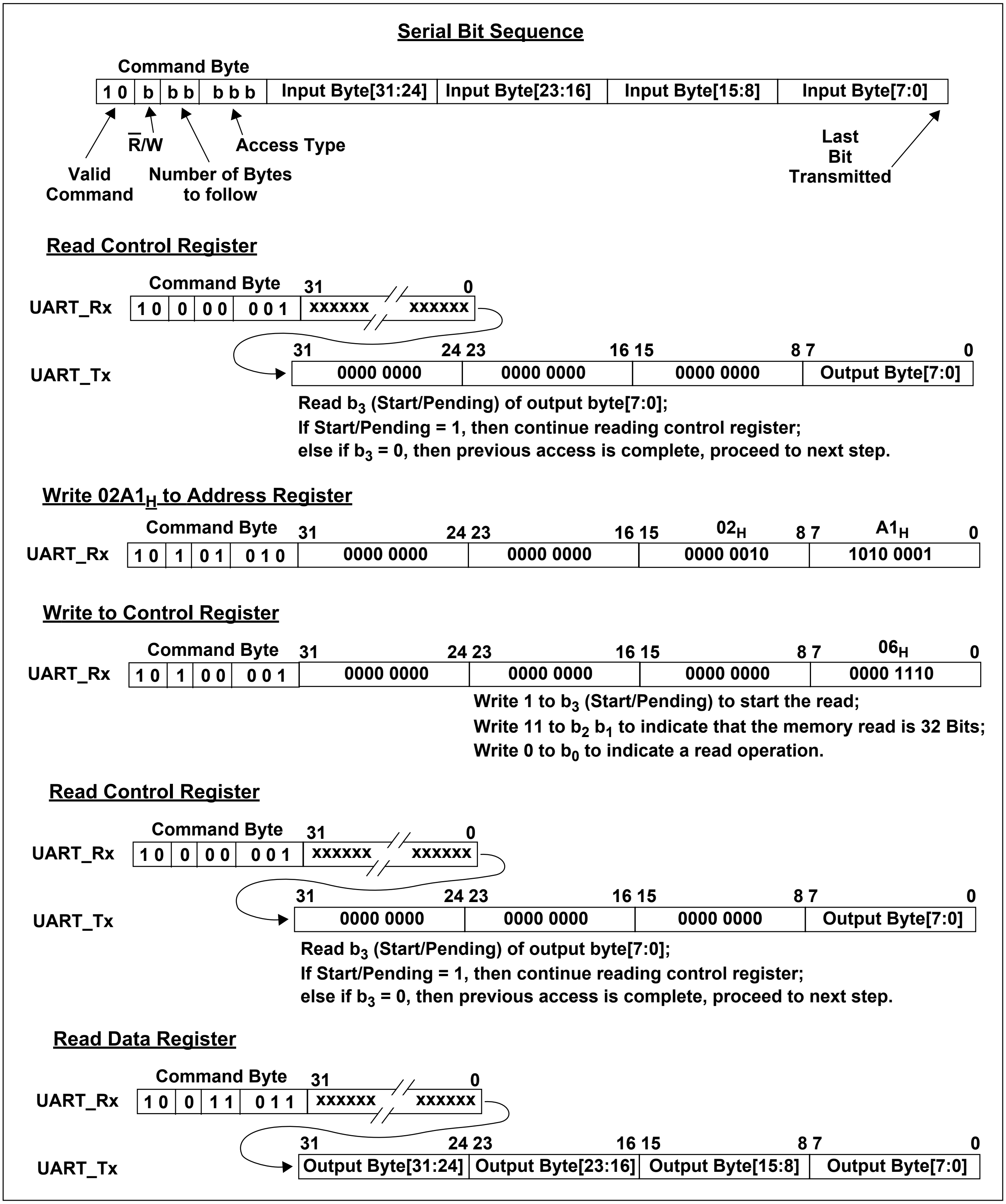
Figure 64 - SSPI Read Register Address $02A1_H$



Read b_3 (Start/Pending) of output byte[7:0];
If Start/Pending = 1, then continue reading control register;
else if b_3 = 0, then previous access is complete, proceed to next step.

Write 1 to b_3 (Start/Pending) to start the write;
Write 11 to b_2 b_1 to indicate that the memory write is 32 bits;
Write 1 to b_0 to indicate a write operation.

Figure 65 - UART Write AAAAAAAA$_H$ to Register Address 02A1$_H$



Read b_3 (Start/Pending) of output byte[7:0];
If Start/Pending = 1, then continue reading control register;
else if b_3 = 0, then previous access is complete, proceed to next step.

Write 1 to b_3 (Start/Pending) to start the read;
Write 11 to b_2 b_1 to indicate that the memory read is 32 Bits;
Write 0 to b_0 to indicate a read operation.

Read b_3 (Start/Pending) of output byte[7:0];
If Start/Pending = 1, then continue reading control register;
else if b_3 = 0, then previous access is complete, proceed to next step.

Figure 66 - UART Read Register Address 02A1$_H$

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