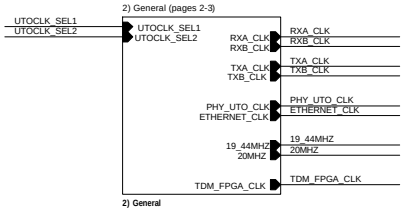
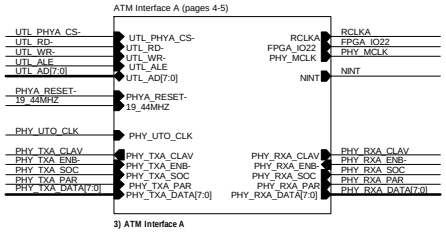
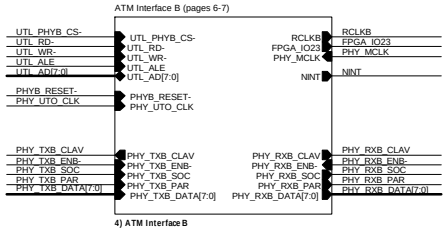
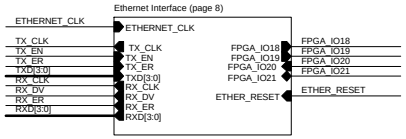
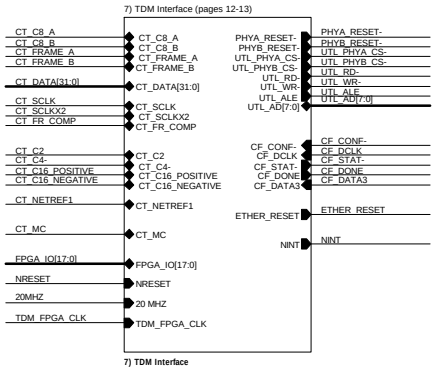
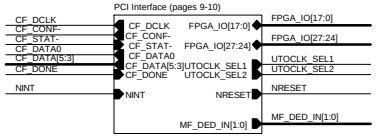


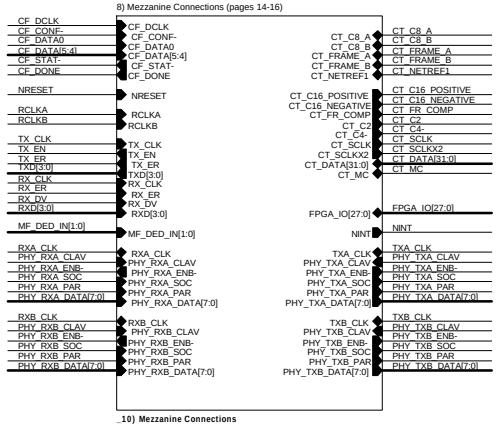








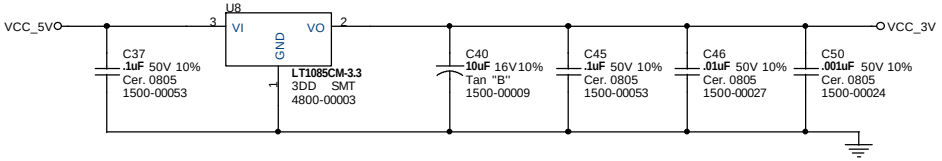


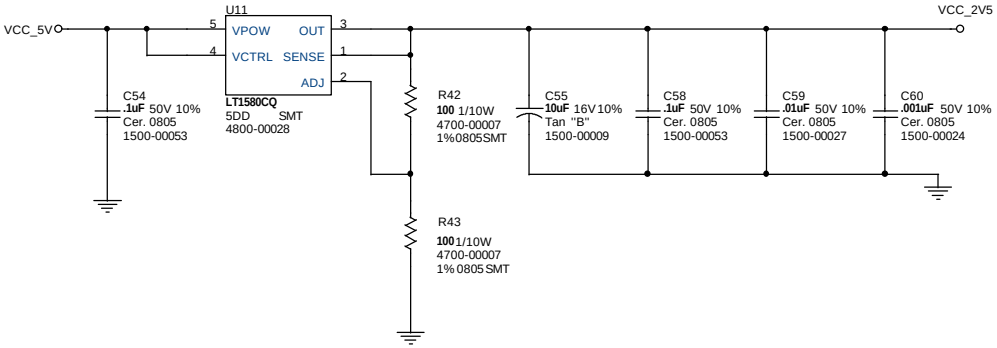


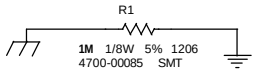
ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board — Interconnections				
Size: C	Document Number: 1000-003	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000	Sheet 1 of 16			

Connect the decoupling capacitor directly to the power pad of the regulator.
Use a wide copper area under the tab of the regulator to dissipate the heat when surface mounted.

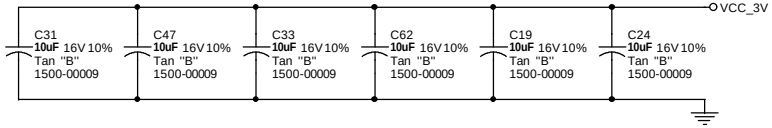




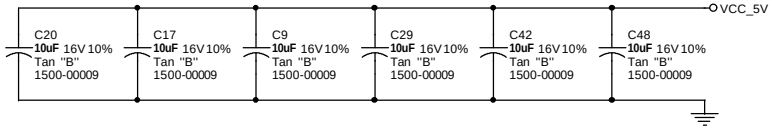


Note on the chassis ground:
This 1 Meg ohm provides a return path from the chassis ground to the digital ground. The mounting hole of the PCI bracket is also connected to the chassis ground.

Spread the bulk decoupling capacitors on the board.



Spread the bulk decoupling capacitors on the board.



ZARLINK Semiconductor - Global Design Support

Title			
T003 Customer Board		Power Interface	
Size B	Document Number 1000-000	Designed By:	Checked By: Rev 02
Date: Friday, November 17, 2000		Sheet 2 of 16	

Sent to both UTOPIA PHYs

<p.4,6> PHY_UTO_CLK — PHY_UTO_CLK

Send to Ethernet PHY

ETHERNET_CLK — ETHERNET_CLK

Sent to Mezzanine Connector

<p.14> RXA_CLK — RXA_CLK
<p.14> TXA_CLK — TXA_CLK
<p.14> RXB_CLK — RXB_CLK
<p.14> TXB_CLK — TXB_CLK

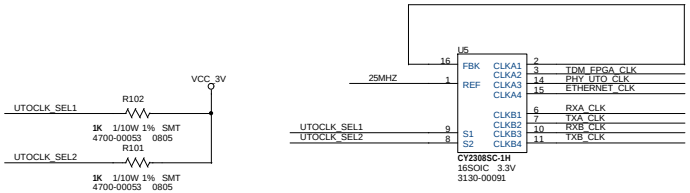
Comes from PCI FPGA

<p.9> UTOCLK_SEL1 — UTOCLK_SEL1
<p.9> UTOCLK_SEL2 — UTOCLK_SEL2

Sent to FPGA

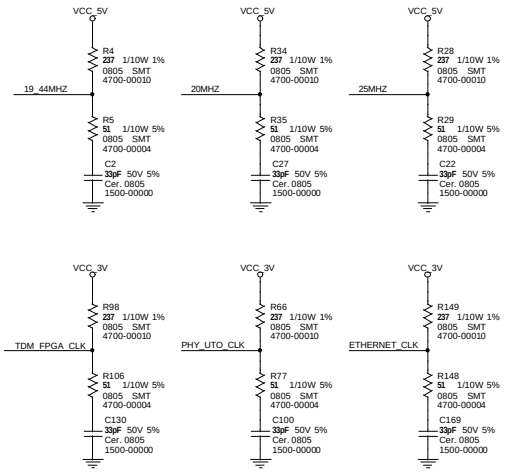
<p.11> TDM_FPGA_CLK — TDM_FPGA_CLK

The clock signals must be impedance controlled to 50 ohms.

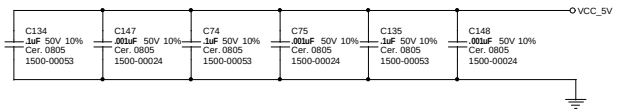


Place these clock terminations at the end of the line. See layout instruction for more details.

We can use two clock termination configurations. For Thevenin termination replace the capacitor by a jumper. For the AC termination no resistor is connected to VCC.

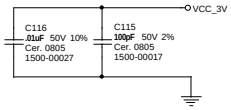


Place one .1uF and one .001uF capacitor near each 5V oscillator



Place near CY2308SC

Use a seperate GND VIA for each capacitor



ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board — Clock Interface				
Size: C	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000	Sheet 3 of 16			

UTOPIA Clock

<p.3> PHY_UTO_CLK — PHY_UTO_CLK

TX and RX UTOPIA Interface

<p.14> PHY_RXA_CLAV — PHY_RXA_CLAV
<p.14> PHY_RXA_ENB- — PHY_RXA_ENB-
<p.14> PHY_RXA_SOC — PHY_RXA_SOC
<p.14> PHY_RXA_PAR — PHY_RXA_PAR
<p.14> PHY_RXA_DATA[7:0] — PHY_RXA_DATA[7:0]

<p.14> PHY_TXA_CLAV — PHY_TXA_CLAV
<p.14> PHY_TXA_ENB- — PHY_TXA_ENB-
<p.14> PHY_TXA_SOC — PHY_TXA_SOC
<p.14> PHY_TXA_PAR — PHY_TXA_PAR
<p.14> PHY_TXA_DATA[7:0] — PHY_TXA_DATA[7:0]

To PCI FPGA

<p.9,16> NINT — NINT

To TDM FPGA and Mezzanine FPGA

<p.14> RCLKA — RCLKA

To Mezzanine FPGA

<p.15> FPGA_IO22 — FPGA_IO22

To ATM PHY B

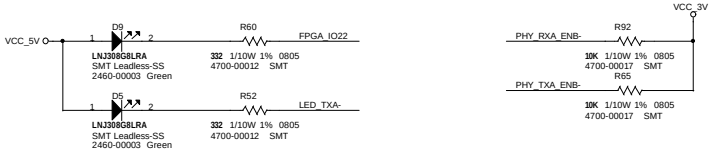
<p.6> PHY_MCLK — PHY_MCLK

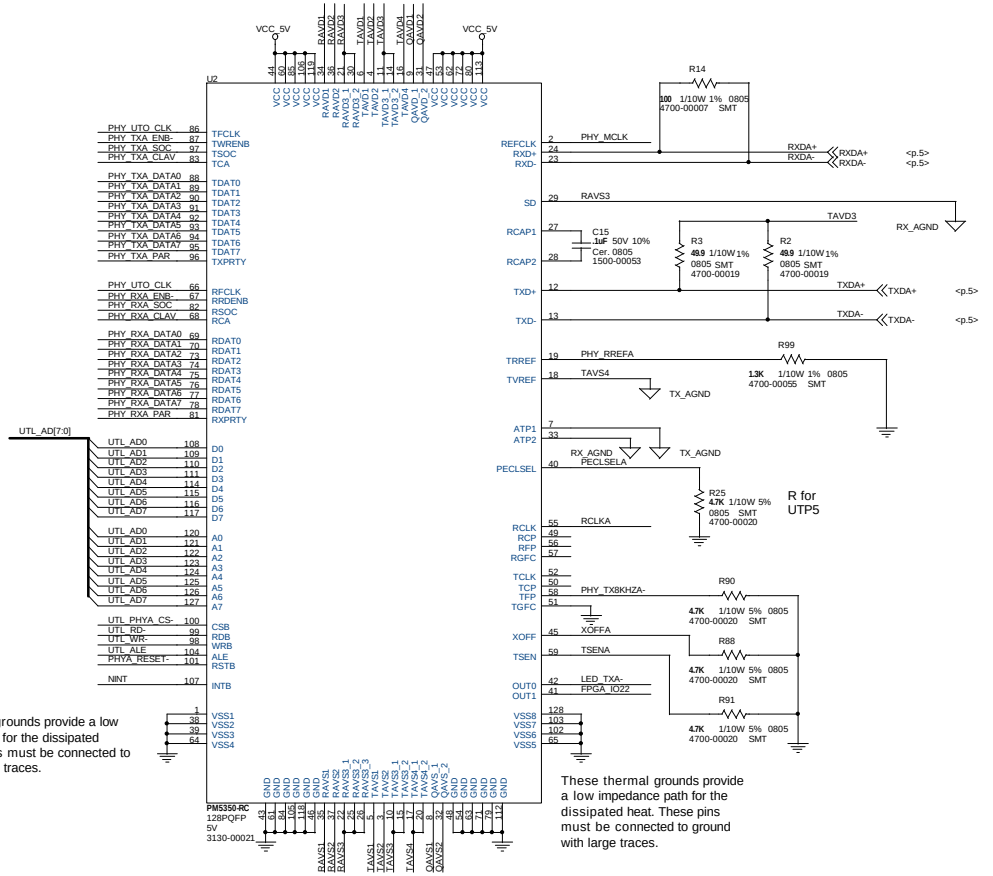
PHY CPU interface, controlled by TDM FPGA

<p.6,11> UTL_AD[7:0] — UTL_AD[7:0]
<p.11> UTL_PHYA_CS- — UTL_PHYA_CS-
<p.11> UTL_RD- — UTL_RD-
<p.11> UTL_WR- — UTL_WR-
<p.11> UTL_ALE — UTL_ALE
<p.11> PHYA_RESET- — PHYA_RESET-

Clock for PHY is 19.44 MHz clock from Oscillator

<p.3> 19_44MHZ — 19_44MHZ — PHY_MCLK



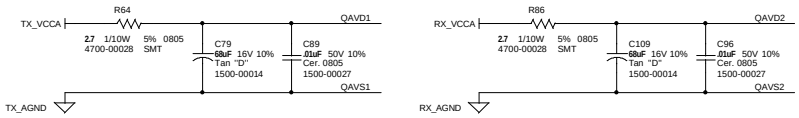


These thermal grounds provide a low impedance path for the dissipated heat. These pins must be connected to ground with large traces.

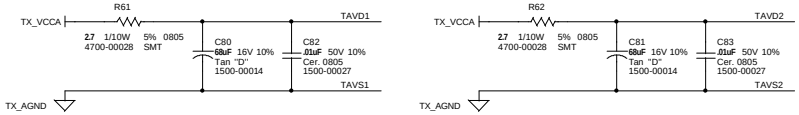
These thermal grounds provide a low impedance path for the dissipated heat. These pins must be connected to ground with large traces.

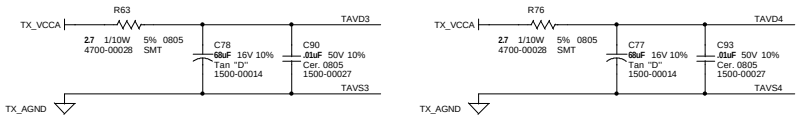
In this 155 Mbps PHY section, the clean VCC plane for the analog supply is called RX_VCCA/RX_AGND and TX_VCCA/TX_AGND. See the layout instructions to view the plane cut for the analog plane.

Quiet power supply

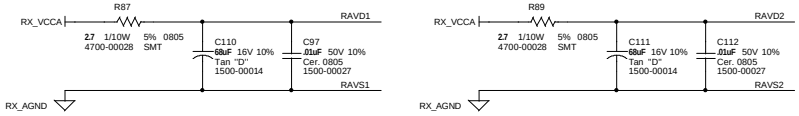


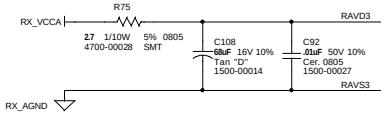
Transmit power supply



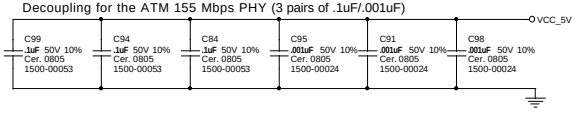


Receive power supply



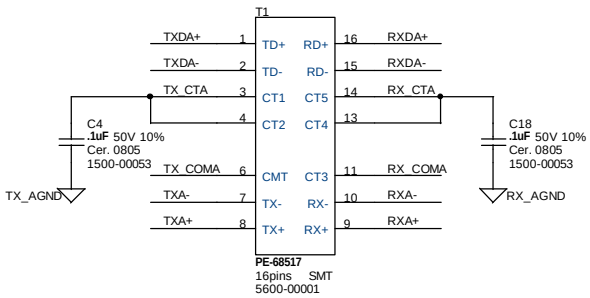


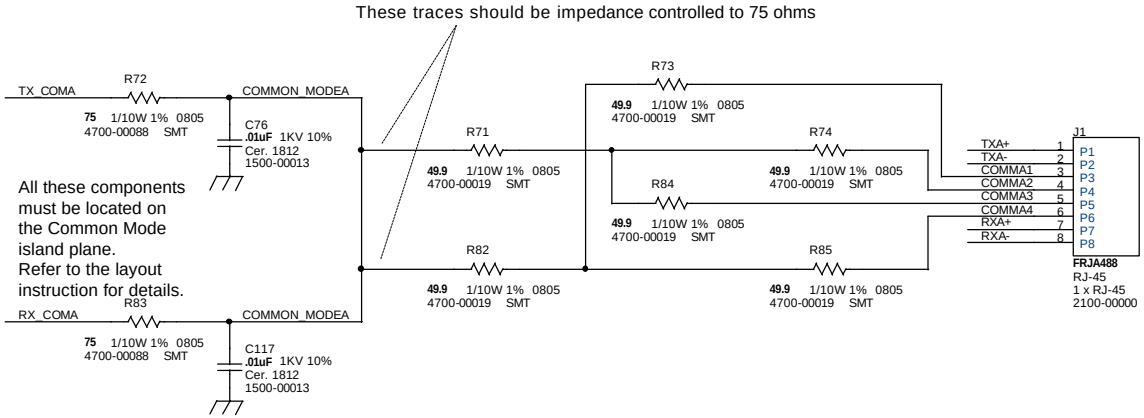
Decoupling for the ATM 155 Mbps PHY (3 pairs of .1uF/.001uF)



ZARLINK Semiconductor - Global Design Support

Title			
T003 Customer Board			Port A PHY 155 Mbps
Size: C	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000	Sheet 4 of 16		





<p.4> RXDA+ RXDA+

<p.4> RXDA- RXDA-

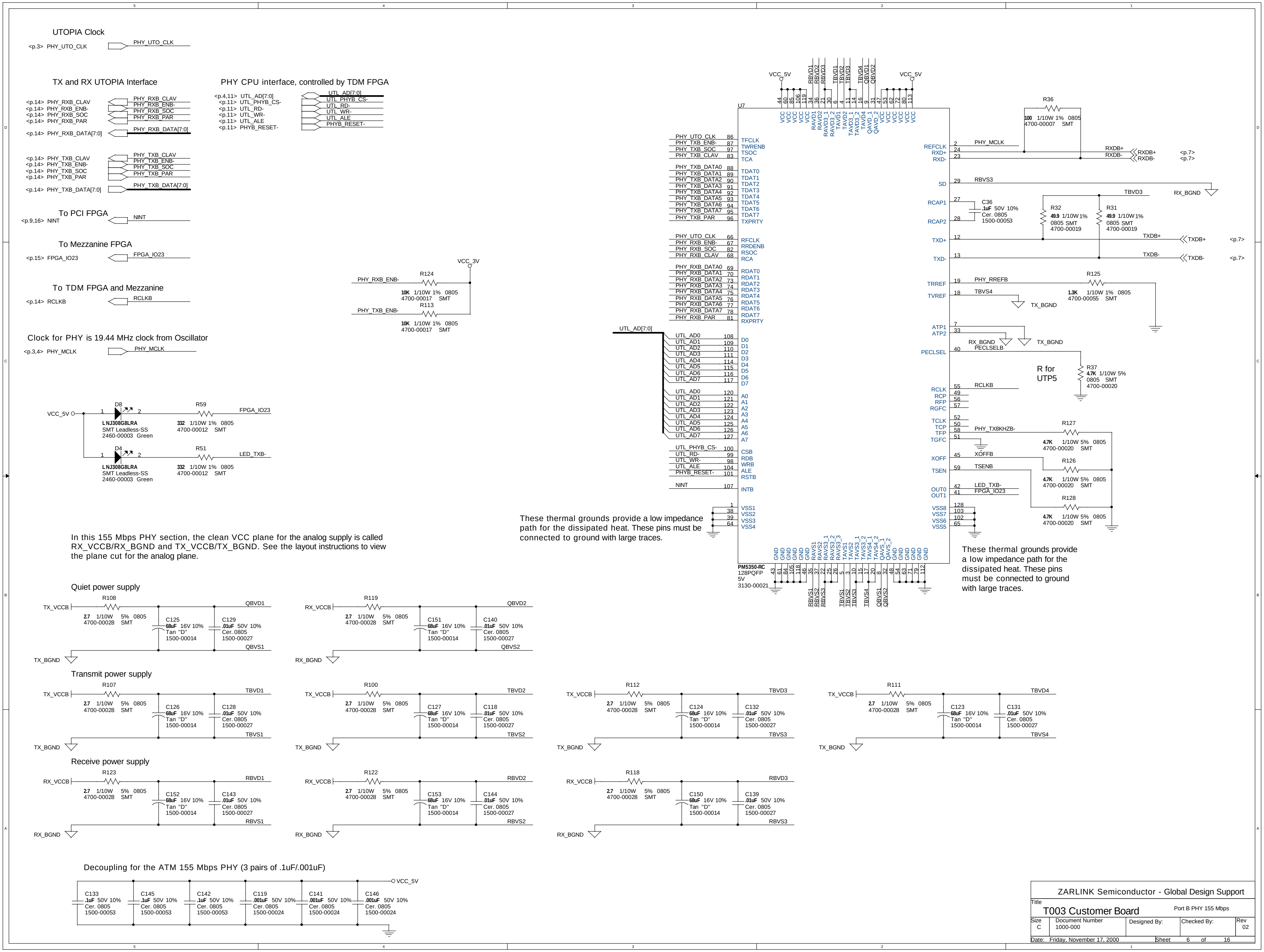
<p.4> TXDA+ TXDA+

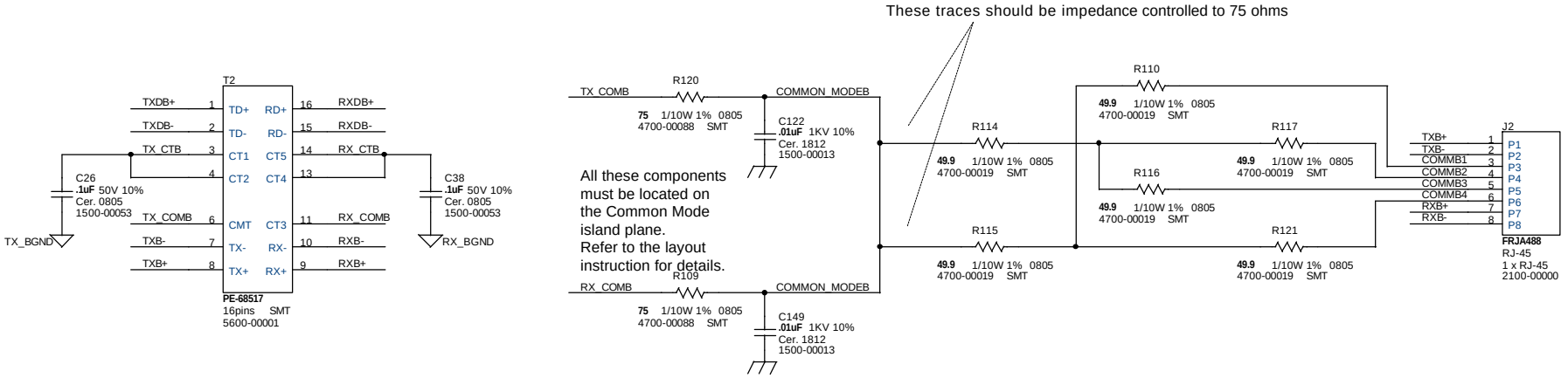
<p.4> TXDA- TXDA-

In this 155 Mbps PHY section, the clean VCC plane for the analog supply is called RX_VCCA/RX_AGND and TX_VCCA/TX_AGND. See the layout instructions to view the plane cut for the analog plane.

ZARLINK Semiconductor - Global Design Support

Title			
T003 Customer Board		Port A Twisted Pair Module Link	
Size B	Document Number 1000-000	Designed By:	Checked By: Rev 02
Date: Friday, November 17, 2000	Sheet 5 of 16		


UTOPIA Clock
TX and RX UTOPIA Interface
PHY CPU interface, controlled by TDM FPGA
To PCI FPGA
To Mezzanine FPGA
To TDM FPGA and Mezzanine
Clock for PHY is 19.44 MHz clock from Oscillator
In this 155 Mbps PHY section, the clean VCC plane for the analog supply is called RX_VCCB/RX_BGND and TX_VCCB/TX_BGND. See the layout instructions to view the plane cut for the analog plane.
These thermal grounds provide a low impedance path for the dissipated heat. These pins must be connected to ground with large traces.
These thermal grounds provide a low impedance path for the dissipated heat. These pins must be connected to ground with large traces.
R for UTP5
PM5350-RC
128PQFP
5V
3130-00021
Quiet power supply
Transmit power supply
Receive power supply
Decoupling for the ATM 155 Mbps PHY (3 pairs of .1uF/.001uF)
ZARLINK Semiconductor - Global Design Support
Title
T003 Customer Board
Port B PHY 155 Mbps
Size C
Document Number 1000-000
Designed By:
Checked By:
Rev 02
Date: Friday, November 17, 2000
Sheet 6 of 16



<p.6> RXDB+ RXDB+

<p.6> RXDB- RXDB-

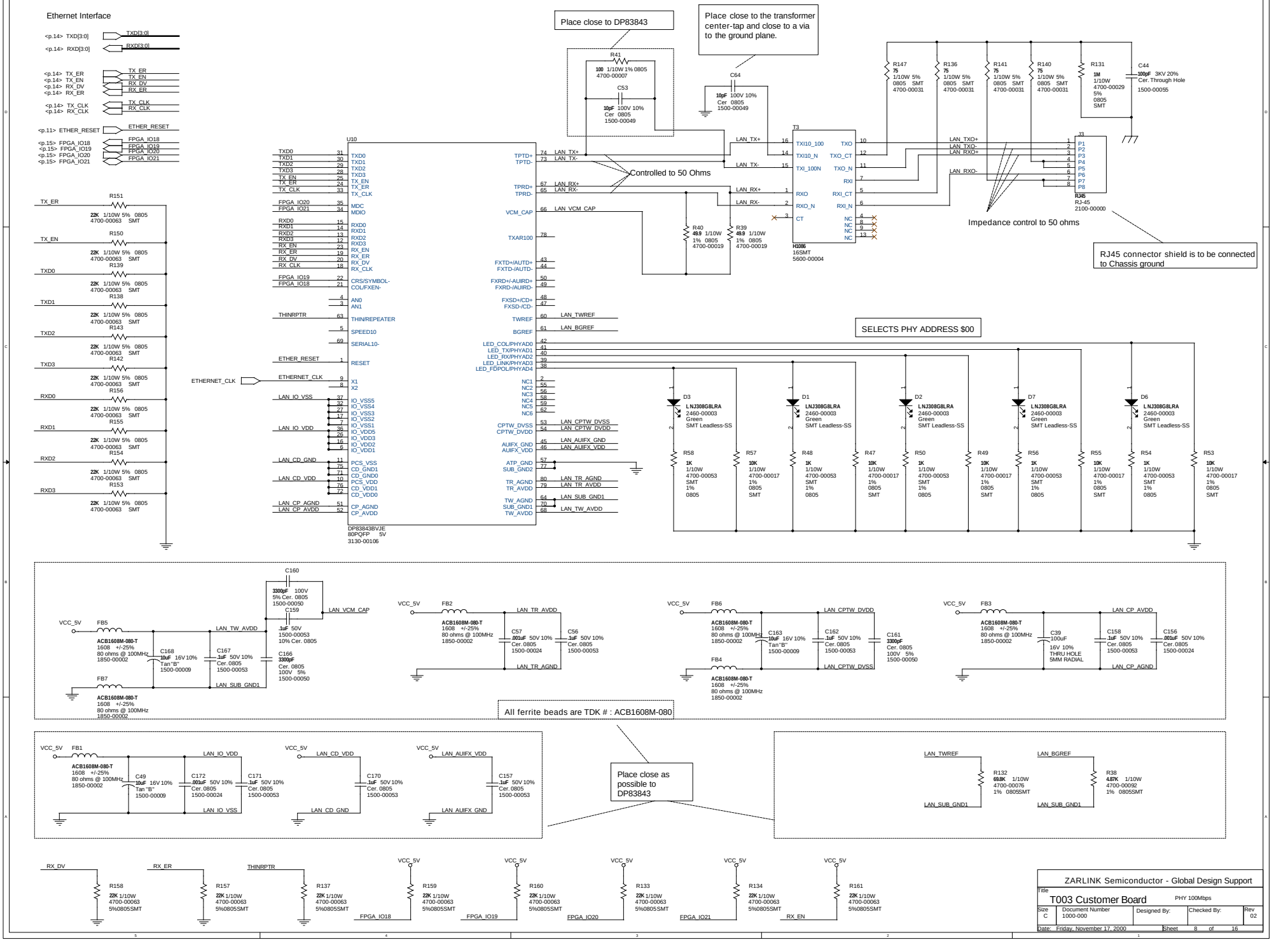
<p.6> TXDB+ TXDB+

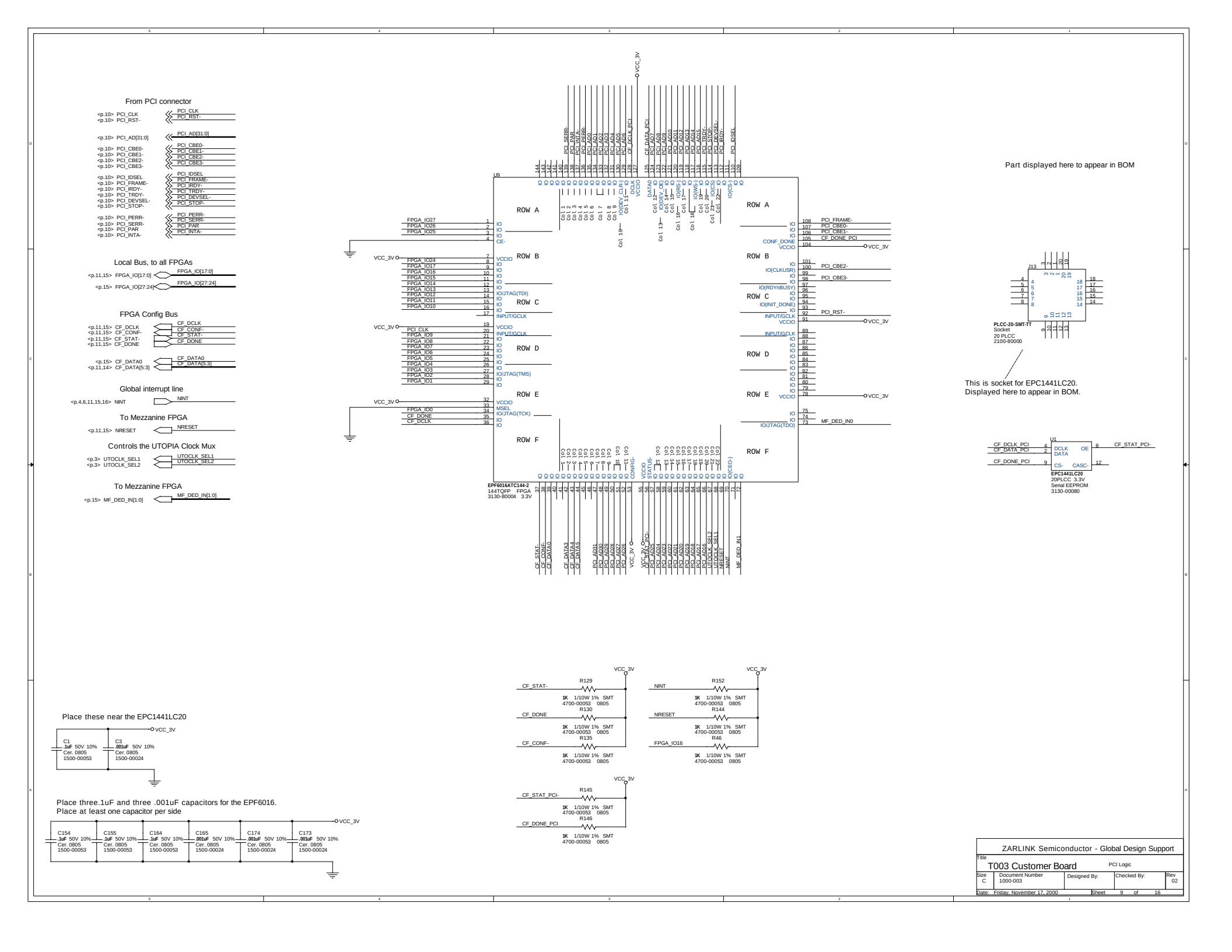
<p.6> TXDB- TXDB-

In this 155 Mbps PHY section, the clean VCC plane for the analog supply is called RX_VCCA/RX_AGND and TX_VCCA/TX_AGND. See the layout instructions to view the plane cut for the analog plane.

ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board — Port B Twisted Pair Module Link				
Size: B	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000	Sheet 7 of 16			


Ethernet Interface
Place close to DP83843
Place close to the transformer center-tap and close to a via to the ground plane.
Controlled to 50 Ohms
Impedance control to 50 ohms
RJ45 connector shield is to be connected to Chassis ground
SELECTS PHY ADDRESS $00
All ferrite beads are TDK # : ACB1608M-080
Place close as possible to DP83843
DP83843BVJE
80PQFP 5V
3130-00106
T003 Customer Board
PHY 100Mbps
ZARLINK Semiconductor - Global Design Support


From PCI connector
PCI_CLK
PCI_RST-
PCI_AD[31:0]
PCI_CBE0-
PCI_CBE1-
PCI_CBE2-
PCI_CBE3-
PCI_IDSEL
PCI_FRAME-
PCI_IRDY-
PCI_TRDY-
PCI_DEVSEL-
PCI_STOP-
PCI_PERR-
PCI_SERR-
PCI_PAR
PCI_INTA-
Local Bus, to all FPGAs
FPGA_IO[17:0]
FPGA_IO[27:24]
FPGA Config Bus
CF_DCLK
CF_CONF-
CF_STAT-
CF_DONE
CF_DATA0
CF_DATA[5:3]
Global interrupt line
NINT
To Mezzanine FPGA
NRESET
Controls the UTOPIA Clock Mux
UTOCLK_SEL1
UTOCLK_SEL2
To Mezzanine FPGA
MF_DED_IN[1:0]
U9
EPF6016ATC144-2
144TQFP FPGA
3130-80004 3.3V
ROW A
ROW B
ROW C
ROW D
ROW E
ROW F
Part displayed here to appear in BOM
PLCC-20-SMT-TT
Socket
20 PLCC
2100-80000
This is socket for EPC1441LC20.
Displayed here to appear in BOM.
EPC1441LC20
20PLCC 3.3V
Serial EEPROM
3130-00080
Place these near the EPC1441LC20
C1 .1uF 50V 10% Cer. 0805 1500-00053
C3 .001uF 50V 10% Cer. 0805 1500-00024
Place three.1uF and three .001uF capacitors for the EPF6016.
Place at least one capacitor per side
C154 .1uF 50V 10% Cer. 0805 1500-00053
C155 .1uF 50V 10% Cer. 0805 1500-00053
C164 .1uF 50V 10% Cer. 0805 1500-00053
C165 .001uF 50V 10% Cer. 0805 1500-00024
C174 .001uF 50V 10% Cer. 0805 1500-00024
C173 .001uF 50V 10% Cer. 0805 1500-00024
R129 1K 1/10W 1% SMT 4700-00053 0805
R130 1K 1/10W 1% SMT 4700-00053 0805
R135 1K 1/10W 1% SMT 4700-00053 0805
R152 1K 1/10W 1% SMT 4700-00053 0805
R144 1K 1/10W 1% SMT 4700-00053 0805
R46 1K 1/10W 1% SMT 4700-00053 0805
R145 1K 1/10W 1% SMT 4700-00053 0805
R146 1K 1/10W 1% SMT 4700-00053 0805
ZARLINK Semiconductor - Global Design Support
T003 Customer Board
PCI Logic
Document Number 1000-003
Designed By:
Checked By:
Rev 02
Date: Friday, November 17, 2000
Sheet 9 of 16

To PCI FPGA

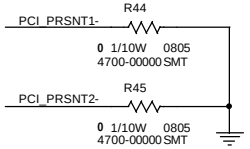
<p.9> PCI_CLK → PCI_CLK
<p.9> PCI_RST- → PCI_RST-
<p.9> PCI_INTA- → PCI_INTA-
<p.9> PCI_IDSEL → PCI_IDSEL

<p.9> PCI_CBE0- → PCI_CBE0-
<p.9> PCI_CBE1- → PCI_CBE1-
<p.9> PCI_CBE2- → PCI_CBE2-
<p.9> PCI_CBE3- → PCI_CBE3-

<p.9> PCI_DEVSEL- → PCI_DEVSEL-
<p.9> PCI_FRAME- → PCI_FRAME-
<p.9> PCI_IRDY- → PCI_IRDY-
<p.9> PCI_TRDY- → PCI_TRDY-
<p.9> PCI_STOP- → PCI_STOP-

<p.9> PCI_PERR- → PCI_PERR-
<p.9> PCI_SERR- → PCI_SERR-
<p.9> PCI_PAR → PCI_PAR

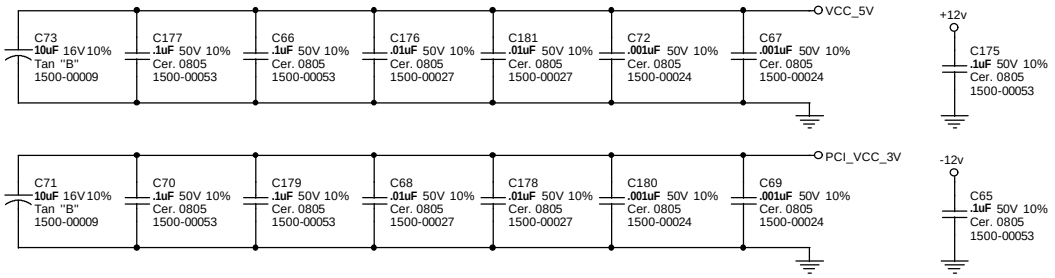
<p.9> PCI_AD[31:0] → PCI_AD[31:0]

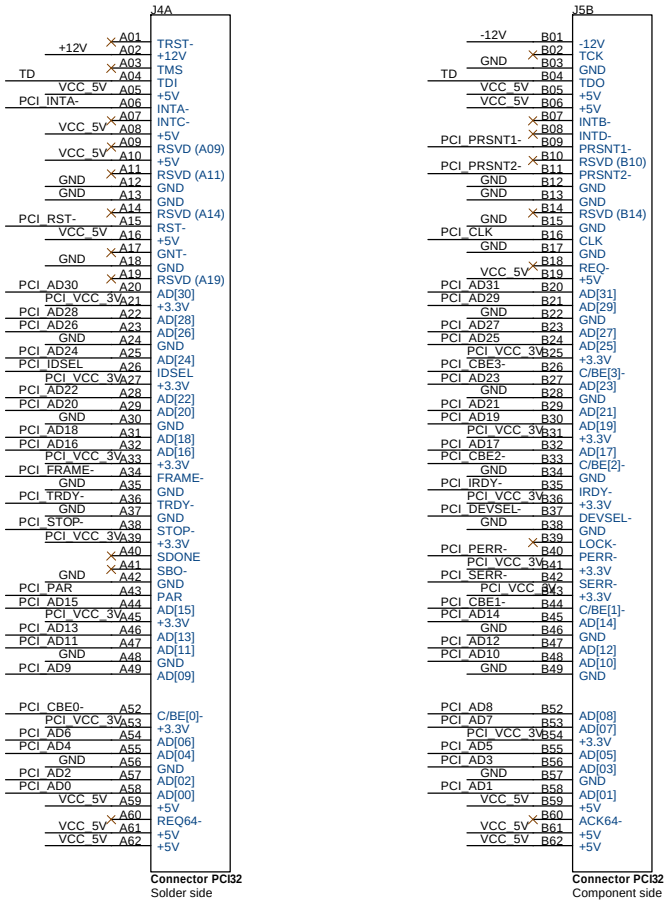


The PCI signals PCI_PRSNT1- and PCI_PRSNT2- indicates the power comsumption by the card. Populate the resistors according to the following table

PRSNT1- / PRSNT2- => Description
NO / NO => No card present
NO / YES => 7.5 Watts
YES / NO => 15 Watts
YES / YES => 25 Watts

Place all these decoupling capacitors near the PCI conecctor. The trace length from pin to capacitor pad shall be less than 0.25" using a trace width of at least 0.02".





PCI SIGNALS ROUTING
All signals routed to the PCI connector except PCI_CLK and PCI_INTA- must be less than 1.5" long.
Signal PCI_CLK must be exactly 2.5" +/- .1" long.
Signal PCI_INTA length is unspecified.

ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board		PCI Connector		
Size: B	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000		Sheet 10 of 16		

Global interrupt

<p.9,16> NINT — NINT

To H.100 Connector

<p.12,15,16> CT_C8_A — CT_C8_A
<p.12,15,16> CT_FRAME_A — CT_FRAME_A
<p.12,15,16> CT_C8_B — CT_C8_B
<p.12,15,16> CT_FRAME_B — CT_FRAME_B
<p.12,15,16> CT_DATA[15:0] — CT_DATA[15:0]
<p.12,15,16> CT_SCLKX2 — CT_SCLKX2
<p.12,15,16> CT_SCLK — CT_SCLK
<p.12,15,16> CT_FR_COMP — CT_FR_COMP

From ADPCM CODECs

<p.13> CODEC_RESET- — CODEC_RESET-
<p.13> CODEC_CS0- — CODEC_CS0-
<p.13> CODEC_CS1- — CODEC_CS1-
<p.13> CODEC_CLK — CODEC_CLK
<p.13> CODEC_DIN — CODEC_DIN
<p.13> CODEC_DOUT — CODEC_DOUT
<p.13> CODEC_BCLK — CODEC_BCLK
<p.13> CODEC_FSYNC — CODEC_FSYNC
<p.13> CODEC_DXA — CODEC_DXA
<p.13> CODEC_DRA — CODEC_DRA
<p.13> CODEC_DXB — CODEC_DXB
<p.13> CODEC_DRB — CODEC_DRB

Local configuration bus

<p.9,15> FPGA_IO[17:0] — FPGA_IO[17:0]

FPGA Config Bus

<p.9> CF_DCLK — CF_DCLK
<p.9> CF_CONF- — CF_CONF-
<p.9> CF_STAT- — CF_STAT-
<p.9> CF_DONE — CF_DONE
<p.9> CF_DATA3 — CF_DATA3

ATM PHY Reset

<p.4> PHYA_RESET- — PHYA_RESET-
<p.6> PHYB_RESET- — PHYB_RESET-

Reset for FPGA

<p.9> NRESET — NRESET

To ATM PHYs

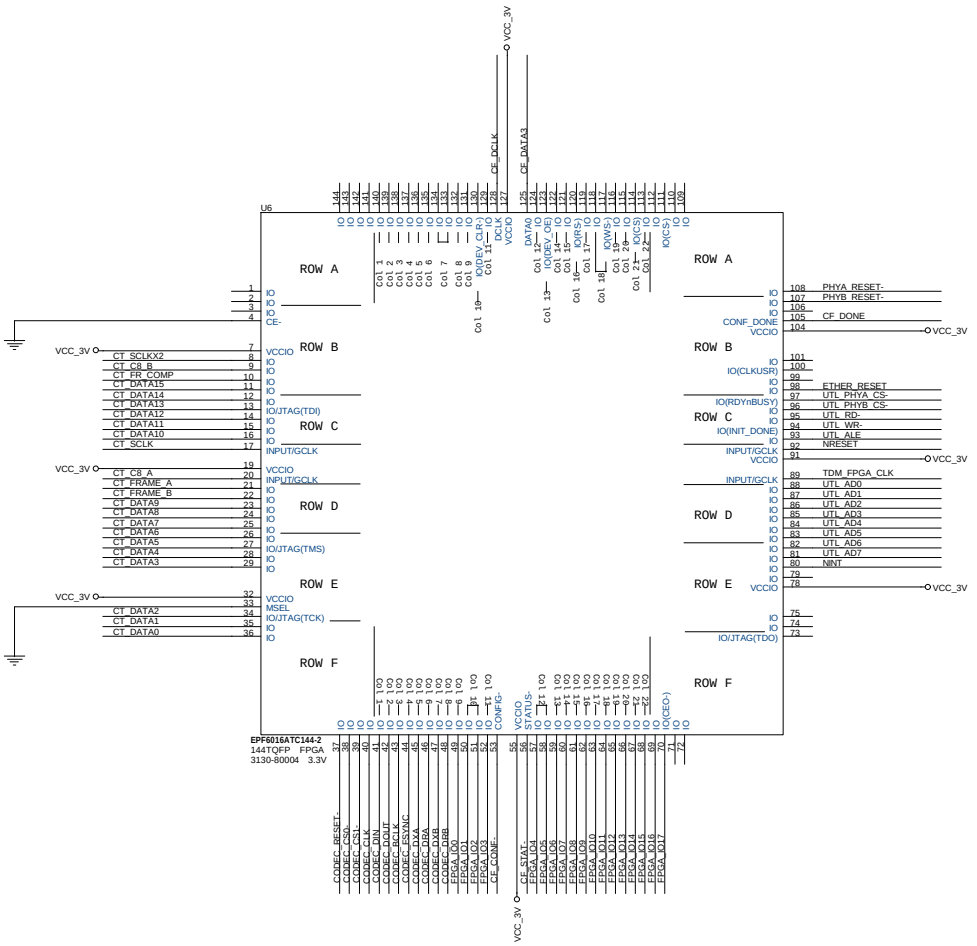
<p.4,6> UTL_AD[7:0] — UTL_AD[7:0]
<p.4> UTL_PHYA_CS- — UTL_PHYA_CS-
<p.6> UTL_PHYB_CS- — UTL_PHYB_CS-
<p.4,6> UTL_RD- — UTL_RD-
<p.4,6> UTL_WR- — UTL_WR-
<p.4,6> UTL_ALE — UTL_ALE

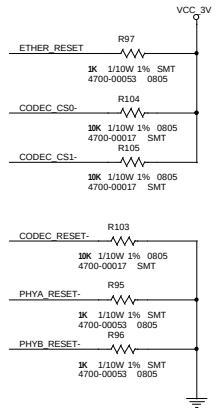
To Ethernet PHY

<p.8> ETHER_RESET — ETHER_RESET

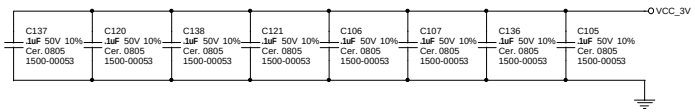
Main Clock for FPGA

<p.3> TDM_FPGA_CLK — TDM_FPGA_CLK





Place two .1uF capacitors per side of the EPF6016ATC



ZARLINK Semiconductor - Global Design Support

Title			
T003 Customer Board		TDM Logic	
Size: C	Document Number: 1000-003	Designed By:	Checked By:
Rev: 02			
Date: Friday, November 17, 2000	Sheet 11 of 16		

To Mezzanine Connector

<p.11,15,16> CT_C8_A — CT_C8_A
<p.11,15,16> CT_FRAME_A — CT_FRAME_A
<p.11,15,16> CT_C8_B — CT_C8_B
<p.11,15,16> CT_FRAME_B — CT_FRAME_B
<p.15> CT_NETREF1 — CT_NETREF1
<p.11,15,16> CT_SCLKX2 — CT_SCLKX2
<p.11,15,16> CT_SCLK — CT_SCLK
<p.11,15,16> CT_FR_COMP — CT_FR_COMP
<p.15,16> CT_MC — CT_MC
<p.15,16> CT_C16_NEGATIVE — CT_C16_NEGATIVE
<p.15,16> CT_C16_POSITIVE — CT_C16_POSITIVE
<p.15,16> CT_C4- — CT_C4-
<p.15,16> CT_C2 — CT_C2
<p.11,15,16> CT_DATA[31:0] — CT_DATA[31:0]

To TDM FPGA

<p.11,15,16> CT_C8_A — CT_C8_A
<p.11,15,16> CT_FRAME_A — CT_FRAME_A
<p.11,15,16> CT_C8_B — CT_C8_B
<p.11,15,16> CT_FRAME_B — CT_FRAME_B
<p.15> CT_NETREF1 — CT_NETREF1
<p.11,15,16> CT_SCLKX2 — CT_SCLKX2
<p.11,15,16> CT_SCLK — CT_SCLK
<p.11,15,16> CT_FR_COMP — CT_FR_COMP
<p.15,16> CT_MC — CT_MC
<p.15,16> CT_C16_NEGATIVE — CT_C16_NEGATIVE
<p.15,16> CT_C16_POSITIVE — CT_C16_POSITIVE
<p.15,16> CT_C4- — CT_C4-
<p.15,16> CT_C2 — CT_C2
<p.11,15,16> CT_DATA[15:0] — CT_DATA[15:0]

J6A

	1	Reserved	
CT_D31	3	CT_D31	
CT_D29	5	CT_D29	
	7	GND	
CT_D26	9	CT_D26	
CT_D24	11	CT_D24	
CT_D23	13	CT_D23	
CT_D21	15	CT_D21	
	17	GND	
CT_D18	19	CT_D18	
CT_D16	21	CT_D16	
CT_D15	23	CT_D15	
CT_D13	25	CT_D13	
	27	GND	
CT_D10	29	CT_D10	
CT_D8	31	CT_D8	
CT_D7	33	CT_D7	
CT_D5	35	CT_D5	
	37	GND	
CT_D2	39	CT_D2	
CT_D0	41	CT_D0	
CT_FRAME_A	43	/CT_FRAME_A	
CT_C8_A	45	CT_C8_A	
CT_NETREFA	47	CT_NETREF	
CT_FRAME_B	49	/CT_FRAME_B	
CT_C8_B	51	CT_C8_B	
CT_MC	53	CT_MC	
SC_FSYNC-	55	/FR_COMP	
CT_SCLK	57	SCLK	
CT_SCLKX2	59	SCLKx2*	
CT_C2	61	C2	
CT_C4-	63	/C4	
CT_C16_POSITIVE	65	/C16+	
	67	GND	

H.100 Edge Finger Connector
Component side

J6B

	2	CT_+5Vdc	
CT_D30	4	CT_D30	
CT_D28	6	CT_D28	
CT_D27	8	CT_D27	
CT_D25	10	CT_D25	
	12	GND	
CT_D22	14	CT_D22	
CT_D20	16	CT_D20	
CT_D19	18	CT_D19	
CT_D17	20	CT_D17	
	22	GND	
CT_D14	24	CT_D14	
CT_D12	26	CT_D12	
CT_D11	28	CT_D11	
CT_D9	30	CT_D9	
	32	GND	
CT_D6	34	CT_D6	
CT_D4	36	CT_D4	
CT_D3	38	CT_D3	
CT_D1	40	CT_D1	
	42	GND	
	44	GND	
	46	GND	
	48	GND	
	50	GND	
	52	GND	
	54	GND	
	56	GND	
	58	GND	
	60	GND	
	62	GND	
	64	GND	
CT_C16_NEGATIVE	66	/C16-	
	68	Reserved	

H.100 Edge Finger Connector
Solder side

RN8: CT_DATA3 CT_DATA2 CT_DATA1 CT_DATA0 — CT_D3 CT_D2 CT_D1 CT_D0
RN7: CT_DATA7 CT_DATA6 CT_DATA5 CT_DATA4 — CT_D7 CT_D6 CT_D5 CT_D4
RN4: CT_DATA19 CT_DATA18 CT_DATA17 CT_DATA16 — CT_D19 CT_D18 CT_D17 CT_D16
RN3: CT_DATA23 CT_DATA22 CT_DATA21 CT_DATA20 — CT_D23 CT_D22 CT_D21 CT_D20
RN6: CT_DATA11 CT_DATA10 CT_DATA9 CT_DATA8 — CT_D11 CT_D10 CT_D9 CT_D8
RN5: CT_DATA15 CT_DATA14 CT_DATA13 CT_DATA12 — CT_D15 CT_D14 CT_D13 CT_D12
RN2: CT_DATA27 CT_DATA26 CT_DATA25 CT_DATA24 — CT_D27 CT_D26 CT_D25 CT_D24
RN1: CT_DATA31 CT_DATA30 CT_DATA29 CT_DATA28 — CT_D31 CT_D30 CT_D29 CT_D28

24 1/16W 5% 8SMT Isolated 4700-00024

R6: CT_NETREFA — CT_NETREF1
R7: SC_FSYNC- — CT_FR_COMP
24.9 1/10W 1% 0805 4700-00002 SMT

SW1: TD08H0SK1 SPST 16SMT 5100-00001
CT_C4- CT_C2 CT_SCLK CT_SCLKX2 CT_C8_A CT_FRAME_A CT_C8_B CT_FRAME_B

R70	100 1/10W 1% 0805 SMT 4700-00007	C88	100pF 50V 5% Cer. 0805 1500-00011
R69	100 1/10W 1% 0805 SMT 4700-00007	C87	100pF 50V 5% Cer. 0805 1500-00011
R68	1K 1/10W 1% 0805 SMT 4700-00053	C86	.001uF 50V 10% Cer. 0805 1500-00024
R67	1K 1/10W 1% 0805 SMT 4700-00053	C85	.001uF 50V 10% Cer. 0805 1500-00024
R81	100 1/10W 1% 0805 SMT 4700-00007	C104	100pF 50V 5% Cer. 0805 1500-00011
R80	100 1/10W 1% 0805 SMT 4700-00007	C103	100pF 50V 5% Cer. 0805 1500-00011
R79	1K 1/10W 1% 0805 SMT 4700-00053	C102	.001uF 50V 10% Cer. 0805 1500-00024
R78	1K 1/10W 1% 0805 SMT 4700-00053	C101	.001uF 50V 10% Cer. 0805 1500-00024

RN12: CT_DATA0 CT_DATA1 CT_DATA2 CT_DATA3 — CT_DATA4 CT_DATA5 CT_DATA6 CT_DATA7 — VCC_5V
RN11: CT_DATA8 CT_DATA9 CT_DATA10 CT_DATA11 — CT_DATA12 CT_DATA13 CT_DATA14 CT_DATA15 — VCC_5V
RN10: CT_DATA16 CT_DATA17 CT_DATA18 CT_DATA19 — CT_DATA20 CT_DATA21 CT_DATA22 CT_DATA23 — VCC_5V
RN9: CT_DATA24 CT_DATA25 CT_DATA26 CT_DATA27 — CT_DATA28 CT_DATA29 CT_DATA30 CT_DATA31 — VCC_5V

100K 1/16W 5% 10SMT Bussed 4700-00025

ZARLINK Semiconductor - Global Design Support

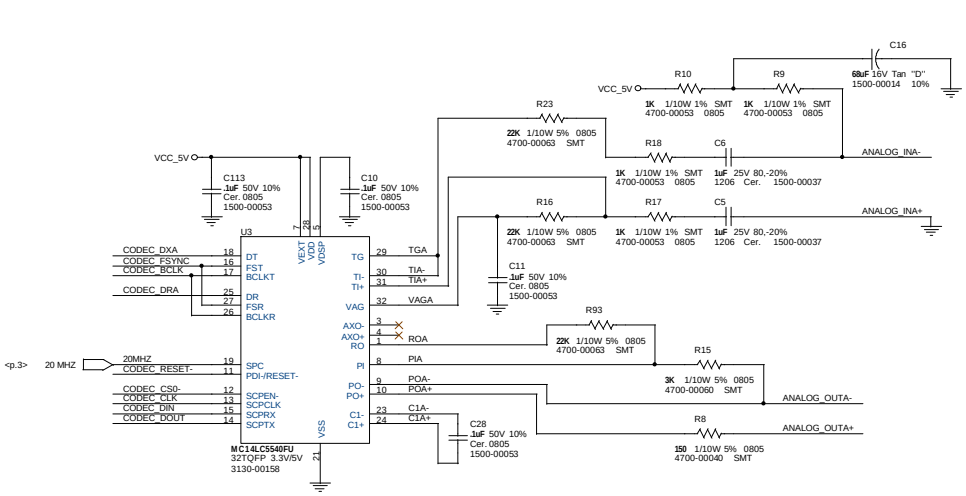
Title: T003 Customer Board			H.100 Connector	
Size: C	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000		Sheet 12 of 16		

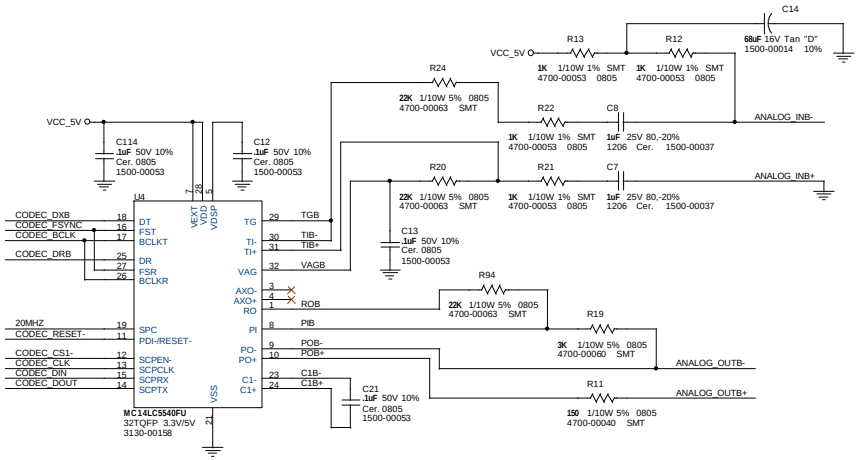
To TDM FPGA

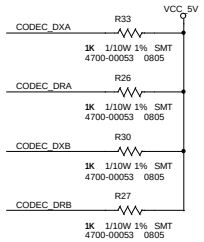
<p.11> CODEC_RESET- → CODEC_RESET-

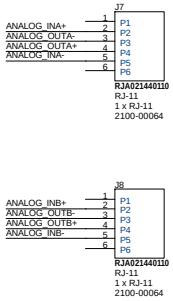
<p.11> CODEC_CS0- → CODEC_CS0-
<p.11> CODEC_CS1- → CODEC_CS1-
<p.11> CODEC_CLK → CODEC_CLK
<p.11> CODEC_DIN → CODEC_DIN
<p.11> CODEC_DOUT → CODEC_DOUT
<p.11> CODEC_BCLK → CODEC_BCLK
<p.11> CODEC_FSYNC → CODEC_FSYNC

<p.11> CODEC_DXA → CODEC_DXA
<p.11> CODEC_DRA → CODEC_DRA
<p.11> CODEC_DXB → CODEC_DXB
<p.11> CODEC_DRB → CODEC_DRB









ZARLINK Semiconductor - Global Design Support

Title				
T003 Customer Board		ADPCM CODECs		
Size: C	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000		Sheet 13 of 16		

3 UTOPIA ports.
Between Main board and MCA2.

<p.3> RXA_CLK
<p.4> PHY_RXA_CLAV
<p.4> PHY_RXA_ENB-
<p.4> PHY_RXA_SOC
<p.4> PHY_RXA_PAR
<p.4> PHY_RXA_DATA[7:0]

RXA_CLK
PHY_RXA_CLAV
PHY_RXA_ENB-
PHY_RXA_SOC
PHY_RXA_PAR
PHY_RXA_DATA[7:0]

<p.3> TXA_CLK
<p.4> PHY_TXA_CLAV
<p.4> PHY_TXA_ENB-
<p.4> PHY_TXA_SOC
<p.4> PHY_TXA_PAR
<p.4> PHY_TXA_DATA[7:0]

TXA_CLK
PHY_TXA_CLAV
PHY_TXA_ENB-
PHY_TXA_SOC
PHY_TXA_PAR
PHY_TXA_DATA[7:0]

<p.3> RXB_CLK
<p.6> PHY_RXB_CLAV
<p.6> PHY_RXB_ENB-
<p.6> PHY_RXB_SOC
<p.6> PHY_RXB_PAR
<p.6> PHY_RXB_DATA[7:0]

RXB_CLK
PHY_RXB_CLAV
PHY_RXB_ENB-
PHY_RXB_SOC
PHY_RXB_PAR
PHY_RXB_DATA[7:0]

<p.3> TXB_CLK
<p.6> PHY_TXB_CLAV
<p.6> PHY_TXB_ENB-
<p.6> PHY_TXB_SOC
<p.6> PHY_TXB_PAR
<p.6> PHY_TXB_DATA[7:0]

TXB_CLK
PHY_TXB_CLAV
PHY_TXB_ENB-
PHY_TXB_SOC
PHY_TXB_PAR
PHY_TXB_DATA[7:0]

Spare FPGA configuration pins.

<p.9> CF_DATA[5:4]
CF_DATA[5:4]

UTOPIA PHY clocks.
From PHYs A & B on Main Board
to FPGA on Mezzanine Board.

<p.4> RCLKA
<p.6> RCLKB
RCLKA
RCLKB

Ethernet

<p.8> TX_ER
<p.8> TX_EN
<p.8> RX_DV
<p.8> RX_ER
TX_ER
TX_EN
RX_DV
RX_ER

<p.8> TX_CLK
<p.8> RX_CLK
TX_CLK
RX_CLK

<p.8> TXD[3:0]
TXD[3:0]

<p.8> RXD[3:0]
RXD[3:0]

J10A

GND	1	USER_IO1	USER_IO2	2	GND
GND	3	USER_IO3	USER_IO4	4	CF_DATA5
CF_DATA4	5	USER_IO5	USER_IO6	6	
RX_ER	7	USER_IO7	USER_IO8	8	RX_DV
TX_EN	9	USER_IO9	USER_IO10	10	TX_ER
VCC_3V	11	USER_IO11	USER_IO12	12	VCC_3V
RXD3	13	USER_IO13	USER_IO14	14	RXD2
RXD1	15	USER_IO15	USER_IO16	16	RXD0
TXD3	17	USER_IO17	USER_IO18	18	TXD2
TXD1	19	USER_IO19	USER_IO20	20	TXD0
VCC_3V	21	USER_IO21	USER_IO22	22	VCC_3V
RX_CLK	23	USER_IO23	USER_IO24	24	TX_CLK
RCLKB	25	USER_IO25	USER_IO26	26	RCLKA
TXC_CLK	27	USER_IO27	USER_IO28	28	PHY_TXC_CLAV
	29	USER_IO29	USER_IO30	30	
	31	USER_IO31	USER_IO32	32	
GND	33	USER_IO33	USER_IO34	34	GND
	35	USER_IO35	USER_IO36	36	
	37	USER_IO37	USER_IO38	38	
	39	USER_IO39	USER_IO40	40	
	41	USER_IO41	USER_IO42	42	RXC_CLK
PHY_RXC_CLAV	43	USER_IO43	USER_IO44	44	PHY_RXC_ENB-
VCC_2V5	45	USER_IO45	USER_IO46	46	VCC_2V5
PHY_RXC_SOC	47	USER_IO47	USER_IO48	48	PHY_RXC_PAR
PHY_RXC_DATA7	49	USER_IO49	USER_IO50	50	PHY_RXC_DATA6
PHY_RXC_DATA5	51	USER_IO51	USER_IO52	52	PHY_RXC_DATA4
PHY_RXC_DATA3	53	USER_IO53	USER_IO54	54	PHY_RXC_DATA2
PHY_RXC_DATA1	55	USER_IO55	USER_IO56	56	PHY_RXC_DATA0
GND	57	USER_IO57	USER_IO58	58	GND
TXB_CLK	59	USER_IO59	USER_IO60	60	PHY_TXB_CLAV
PHY_TXB_ENB-	61	USER_IO61	USER_IO62	62	PHY_TXB_SOC
PHY_TXB_PAR	63	USER_IO63	USER_IO64	64	
	65	USER_IO65	USER_IO66	66	
VCC_3V	67	USER_IO67	USER_IO68	68	VCC_3V
	69	USER_IO69	USER_IO70	70	
	71	USER_IO71	USER_IO72	72	
	73	USER_IO73	USER_IO74	74	PHY_TXB_DATA7
PHY_TXB_DATA6	75	USER_IO75	USER_IO76	76	PHY_TXB_DATA5
PHY_TXB_DATA4	77	USER_IO77	USER_IO78	78	PHY_TXB_DATA3
VCC_5V	79	USER_IO79	USER_IO80	80	VCC_5V

177983-8 SMT
Mezzanine receptacle
2100-00043

J10B

PHY_TXB_DATA2	81	USER_IO81	USER_IO82	82	PHY_TXB_DATA1
PHY_TXB_DATA0	83	USER_IO83	USER_IO84	84	RXB_CLK
PHY_RXB_CLAV	85	USER_IO85	USER_IO86	86	PHY_RXB_ENB-
PHY_RXB_SOC	87	USER_IO87	USER_IO88	88	PHY_RXB_PAR
PHY_RXB_DATA15	89	USER_IO89	USER_IO90	90	PHY_RXB_DATA14
GND	91	USER_IO91	USER_IO92	92	GND
PHY_RXB_DATA13	93	USER_IO93	USER_IO94	94	PHY_RXB_DATA12
PHY_RXB_DATA11	95	USER_IO95	USER_IO96	96	PHY_RXB_DATA10
PHY_RXB_DATA9	97	USER_IO97	USER_IO98	98	PHY_RXB_DATA8
PHY_RXB_DATA7	99	USER_IO99	USER_IO100	100	PHY_RXB_DATA6
VCC_2V5	101	USER_IO101	USER_IO102	102	VCC_2V5
PHY_RXB_DATA5	103	USER_IO103	USER_IO104	104	PHY_RXB_DATA4
PHY_RXB_DATA3	105	USER_IO105	USER_IO106	106	PHY_RXB_DATA2
PHY_RXB_DATA1	107	USER_IO107	USER_IO108	108	PHY_RXB_DATA0
TXA_CLK	109	USER_IO109	USER_IO110	110	PHY_TXA_CLAV
PHY_TXA_ENB-	111	USER_IO111	USER_IO112	112	PHY_TXA_SOC
GND	113	USER_IO113	USER_IO114	114	GND
PHY_TXA_PAR	115	USER_IO115	USER_IO116	116	
	117	USER_IO117	USER_IO118	118	
	119	USER_IO119	USER_IO120	120	
	121	USER_IO121	USER_IO122	122	
VCC_3V	123	USER_IO123	USER_IO124	124	PHY_TXA_DATA7
PHY_TXA_DATA6	125	USER_IO125	USER_IO126	126	VCC_3V
PHY_TXA_DATA4	127	USER_IO127	USER_IO128	128	PHY_TXA_DATA5
PHY_TXA_DATA2	129	USER_IO129	USER_IO130	130	PHY_TXA_DATA3
PHY_TXA_DATA0	131	USER_IO131	USER_IO132	132	PHY_TXA_DATA1
PHY_RXA_CLAV	133	USER_IO133	USER_IO134	134	RXA_CLK
GND	135	USER_IO135	USER_IO136	136	PHY_RXA_ENB-
PHY_RXA_SOC	137	USER_IO137	USER_IO138	138	GND
PHY_RXA_DATA15	139	USER_IO139	USER_IO140	140	PHY_RXA_PAR
PHY_RXA_DATA13	141	USER_IO141	USER_IO142	142	PHY_RXA_DATA14
PHY_RXA_DATA11	143	USER_IO143	USER_IO144	144	PHY_RXA_DATA12
VCC_5V	145	USER_IO145	USER_IO146	146	PHY_RXA_DATA10
PHY_RXA_DATA9	147	USER_IO147	USER_IO148	148	VCC_5V
PHY_RXA_DATA7	149	USER_IO149	USER_IO150	150	PHY_RXA_DATA8
PHY_RXA_DATA5	151	USER_IO151	USER_IO152	152	PHY_RXA_DATA6
PHY_RXA_DATA3	153	USER_IO153	USER_IO154	154	PHY_RXA_DATA4
PHY_RXA_DATA1	155	USER_IO155	USER_IO156	156	PHY_RXA_DATA2
GND	157	USER_IO157	USER_IO158	158	PHY_RXA_DATA0
	159	USER_IO159	USER_IO160	160	GND

177983-8 SMT
Mezzanine receptacle
2100-00043

RN16
PHY_RXA_DATA8 1 — 10 VCC_3V
PHY_RXA_DATA9 2 — 9 PHY_RXA_DATA12
PHY_RXA_DATA10 3 — 8 PHY_RXA_DATA13
PHY_RXA_DATA11 4 — 7 PHY_RXA_DATA14
VCC_3V 5 — 6 PHY_RXA_DATA15
100K 1/16W 5% 10SMT Bussed 4700-00025

RN14
PHY_RXC_DATA0 1 — 10 VCC_3V
PHY_RXC_DATA1 2 — 9 PHY_RXC_DATA4
PHY_RXC_DATA2 3 — 8 PHY_RXC_DATA5
PHY_RXC_DATA3 4 — 7 PHY_RXC_DATA6
VCC_3V 5 — 6 PHY_RXC_DATA7
100K 1/16W 5% 10SMT Bussed 4700-00025

RN15
PHY_RXB_DATA8 1 — 10 VCC_3V
PHY_RXB_DATA9 2 — 9 PHY_RXB_DATA12
PHY_RXB_DATA10 3 — 8 PHY_RXB_DATA13
PHY_RXB_DATA11 4 — 7 PHY_RXB_DATA14
VCC_3V 5 — 6 PHY_RXB_DATA15
100K 1/16W 5% 10SMT Bussed 4700-00025

RN13
PHY_RXC_ENB- 1 — 10 VCC_3V
PHY_RXC_SOC 2 — 9 TXC_CLK
PHY_RXC_PAR 3 — 8 RXC_CLK
PHY_RXC_CLAV 4 — 7 PHY_TXC_CLAV
VCC_3V 5 — 6
100K 1/16W 5% 10SMT Bussed 4700-00025

Place two 10uF and two .1uF capacitors near the connector.

VCC_3V
C51 10uF 16V 10% Tan "B" 1500-00009
C30 .1uF 50V 10% Cer. 0805 1500-00053

Place two 10uF and two .1uF capacitors near the connector.

VCC_2V5
C41 10uF 16V 10% Tan "B" 1500-00009
C23 .1uF 50V 10% Cer. 0805 1500-00053

Place two 10uF and two .1uF capacitors near the connector.

VCC_5V
C61 10uF 16V 10% Tan "B" 1500-00009
C34 .1uF 50V 10% Cer. 0805 1500-00053

ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board — Left Connector

Size	Document Number	Designed By:	Checked By:	Rev
B	1000-000			02

Date: Friday, November 17, 2000 Sheet 14 of 16

H.100 Clocks and data

<p.11,12,16> CT_C8_A
<p.11,12,16> CT_C8_B
<p.11,12,16> CT_FRAME_A
<p.11,12,16> CT_FRAME_B
<p.12,16> CT_C16_NEGATIVE
<p.12,16> CT_C16_POSITIVE
<p.11,12,16> CT_FR_COMP
<p.12,16> CT_C2
<p.12,16> CT_C4-
<p.11,12,16> CT_SCLK
<p.11,12,16> CT_SCLKX2
<p.12> CT_NETREF1
<p.12,16> CT_MC

To PCI FPGA

<p.9,16> NINT

To Mezzanine FPGA

<p.9> MF_DED_IN[1:0]

General Purpose IO Bus

<p.4,6,8,9,11> FPGA_IO[27:0]

Mezzanine FPGA configuration signals

<p.9> CF_CONF-
<p.9> CF_DATA0
<p.9> CF_DCLK
<p.9> CF_STAT-
<p.9> CF_DONE
<p.9> NRESET

<p.11,12,16> CT_DATA[31:0]

H.100 Clocks and Data Signals

<p.11,12,16> CT_C8_A
<p.11,12,16> CT_FRAME_A

<p.11,12,16> CT_C8_B
<p.11,12,16> CT_FRAME_B

<p.11,12,16> CT_DATA[15:0]

<p.11,12,16> CT_SCLK
<p.11,12,16> CT_SCLKX2

<p.11,12,16> CT_FR_COMP

<p.12,16> CT_MC
<p.16> MC_CLOCK
<p.16> MC_TX
<p.16> MC_RX

<p.12,16> CT_C16_NEGATIVE
<p.12,16> CT_C16_POSITIVE
<p.12,16> CT_C4-
<p.12,16> CT_C2

Interrupt Line

<p.4,6,9,11,16> NINT

Pull-up for Mezz board detection

MF_DED_IN0 — R162 — VCC_3V

10K 1/10W 1% 0805
4700-00017 SMT

J11A

GND	1	2	GND
NINT	3	4	
	5	6	
VCC_5V	7	8	
	9	10	VCC_5V
	11	12	
	13	14	
	15	16	
GND	17	18	GND
	19	20	
	21	22	
	23	24	
	25	26	
VCC_2V5	27	28	VCC_2V5
	29	30	
	31	32	
	33	34	
	35	36	
VCC_5V	37	38	VCC_5V
	39	40	
	41	42	
FPGA_IO27	43	44	FPGA_IO26
FPGA_IO25	45	46	FPGA_IO24
GND	47	48	GND
FPGA_IO23	49	50	FPGA_IO22
FPGA_IO21	51	52	FPGA_IO20
FPGA_IO19	53	54	FPGA_IO18
VCC_3V	55	56	VCC_3V
FPGA_IO17	57	58	FPGA_IO16
FPGA_IO15	59	60	FPGA_IO14
FPGA_IO13	61	62	FPGA_IO12
FPGA_IO11	63	64	FPGA_IO10
VCC_2V5	65	66	VCC_2V5
FPGA_IO9	67	68	FPGA_IO8
FPGA_IO7	69	70	FPGA_IO6
FPGA_IO5	71	72	FPGA_IO4
FPGA_IO3	73	74	FPGA_IO2
GND	75	76	GND
FPGA_IO1	77	78	FPGA_IO0
	79	80	

	1	USER_IO1	USER_IO2
	3	USER_IO3	USER_IO4
	5	USER_IO5	USER_IO6
	7	USER_IO7	USER_IO8
	9	USER_IO9	USER_IO10
	11	USER_IO11	USER_IO12
	13	USER_IO13	USER_IO14
	15	USER_IO15	USER_IO16
	17	USER_IO17	USER_IO18
	19	USER_IO19	USER_IO20
	21	USER_IO21	USER_IO22
	23	USER_IO23	USER_IO24
	25	USER_IO25	USER_IO26
	27	USER_IO27	USER_IO28
	29	USER_IO29	USER_IO30
	31	USER_IO31	USER_IO32
	33	USER_IO33	USER_IO34
	35	USER_IO35	USER_IO36
	37	USER_IO37	USER_IO38
	39	USER_IO39	USER_IO40
	41		
	43	USER_IO41	USER_IO42
	45	USER_IO43	USER_IO44
	47	USER_IO45	USER_IO46
	49	USER_IO47	USER_IO48
	51	USER_IO49	USER_IO50
	53	USER_IO51	USER_IO52
	55	USER_IO53	USER_IO54
	57	USER_IO55	USER_IO56
	59	USER_IO57	USER_IO58
	61	USER_IO59	USER_IO60
	63	USER_IO61	USER_IO62
	65	USER_IO63	USER_IO64
	67	USER_IO65	USER_IO66
	69	USER_IO67	USER_IO68
	71	USER_IO69	USER_IO70
	73	USER_IO71	USER_IO72
	75	USER_IO73	USER_IO74
	77	USER_IO75	USER_IO76
	79	USER_IO77	USER_IO78
		USER_IO79	USER_IO80

177983-8 SMT
Mezzanine receptacle
2100-00043

J11B

MF_DED_IN1	81	82	MF_DED_IN0
VCC_3V	83	84	VCC_3V
NRESET	85	86	CF_DONE
CF_STAT-	87	88	CF_DCLK
CF_DATA0	89	90	CF_CONF-
	91	92	
GND	93	94	GND
	95	96	
	97	98	CT_DATA31
CT_DATA30	99	100	CT_DATA29
CT_DATA28	101	102	CT_DATA27
VCC_5V	103	104	VCC_5V
CT_DATA26	105	106	CT_DATA25
CT_DATA24	107	108	CT_DATA23
CT_DATA22	109	110	CT_DATA21
GND	111	112	GND
CT_DATA20	113	114	CT_DATA19
CT_DATA18	115	116	CT_DATA17
CT_DATA16	117	118	CT_DATA15
CT_DATA14	119	120	CT_DATA13
VCC_3V	121	122	VCC_3V
CT_DATA12	123	124	CT_DATA11
CT_DATA10	125	126	CT_DATA9
CT_DATA8	127	128	CT_DATA7
CT_DATA6	129	130	CT_DATA5
VCC_2V5	131	132	VCC_2V5
CT_DATA4	133	134	CT_DATA3
CT_DATA2	135	136	CT_DATA1
CT_DATA0	137	138	MC_RX
MC_TX	139	140	MC_CLOCK
GND	141	142	GND
CT_MC	143	144	
CT_NETREF1	145	146	CT_SCLKX2
CT_SCLK	147	148	CT_C4-
CT_C2	149	150	CT_FR_COMP
VCC_3V	151	152	VCC_3V
CT_C16_POSITIVE	153	154	CT_C16_NEGATIVE
CT_FRAME_B	155	156	CT_FRAME_A
CT_C8_B	157	158	CT_C8_A
GND	159	160	GND

	81	USER_IO81	USER_IO82
	83	USER_IO83	USER_IO84
	85	USER_IO85	USER_IO86
	87	USER_IO87	USER_IO88
	89	USER_IO89	USER_IO90
	91	USER_IO91	USER_IO92
	93	USER_IO93	USER_IO94
	95	USER_IO95	USER_IO96
	97	USER_IO97	USER_IO98
	99	USER_IO99	USER_IO100
	101	USER_IO101	USER_IO102
	103	USER_IO103	USER_IO104
	105	USER_IO105	USER_IO106
	107	USER_IO107	USER_IO108
	109	USER_IO109	USER_IO110
	111	USER_IO111	USER_IO112
	113	USER_IO113	USER_IO114
	115	USER_IO115	USER_IO116
	117	USER_IO117	USER_IO118
	119	USER_IO119	USER_IO120
	121		
	123	USER_IO121	USER_IO122
	125	USER_IO123	USER_IO124
	127	USER_IO125	USER_IO126
	129	USER_IO127	USER_IO128
	131	USER_IO129	USER_IO130
	133	USER_IO131	USER_IO132
	135	USER_IO133	USER_IO134
	137	USER_IO135	USER_IO136
	139	USER_IO137	USER_IO138
	141	USER_IO139	USER_IO140
	143	USER_IO141	USER_IO142
	145	USER_IO143	USER_IO144
	147	USER_IO145	USER_IO146
	149	USER_IO147	USER_IO148
	151	USER_IO149	USER_IO150
	153	USER_IO151	USER_IO152
	155	USER_IO153	USER_IO154
	157	USER_IO155	USER_IO156
	159	USER_IO157	USER_IO158
		USER_IO159	USER_IO160

177983-8 SMT
Mezzanine receptacle
2100-00043

Place two 10uF and two .1uF capacitors near the connector.

VCC_3V
C63 **10uF** 16V 10% Tan "B" 1500-00009
C35 **.1uF** 50V 10% Cer. 0805 1500-00053

Place two 10uF and two .1uF capacitors near the connector.

VCC_2V5
C52 **10uF** 16V 10% Tan "B" 1500-00009
C32 **.1uF** 50V 10% Cer. 0805 1500-00053

Place two 10uF and two .1uF capacitors near the connector.

VCC_5V
C43 **10uF** 16V 10% Tan "B" 1500-00009
C25 **.1uF** 50V 10% Cer. 0805 1500-00053

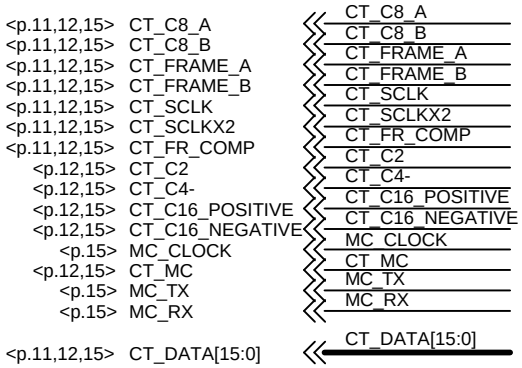
ZARLINK Semiconductor - Global Design Support

Title: T003 Customer Board — Right Connector

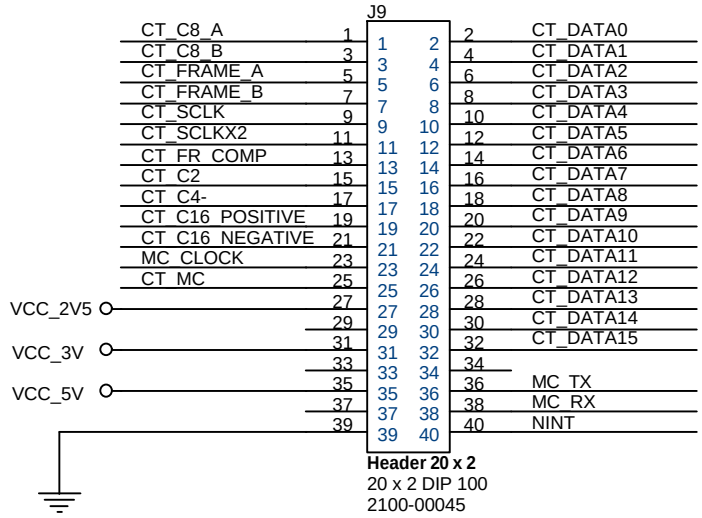
Size	Document Number	Designed By:	Checked By:	Rev
B	1000-000			02

Date: Friday, November 17, 2000 Sheet 15 of 16

H.100 Clocks and Data Signals



Interrupt Line



ZARLINK Semiconductor - Global Design Support				
Title: T003 Customer Board — Test Headers				
Size: A	Document Number: 1000-000	Designed By:	Checked By:	Rev: 02
Date: Friday, November 17, 2000	Sheet 16 of 16			