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# Programmer's Manual
# for the MT90220/1

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| Document Status: | Issue 3 |
| Issue Date: | December 1999 |

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# MT90220/1

## 1.0 Introduction

### 1.1 Purpose of Manual

This manual is a guide to programming the MT90220/1 device.

Section 2.0 provides general programming concepts common to all modes
Section 3.0 lists the necessary steps to use the device in IMA mode
Section 4.0 lists the necessary steps to use the device in UNI (non-IMA) mode
Section 5.0 describes mixed mode (some links in UNI mode, some in IMA mode)
Section 6.0 provides basic troubleshooting techniques
Section 7.0 presents a diagram of the interrupt registers and structure
Section 8.0 lists changes to this document since Issue 2

### 1.2 Format of Manual (Conventions)

Register names within text descriptions match those found in the MT90220/1 Data Sheet. They are shown in **Bold**. Register names in summary tables are the software defines and are indicated in **UPPERCASE_BOLD**. References to device driver (DD) software functions are in *Italic( )*. For brevity, argument lists for these functions are not included in this document.

### 1.3 What is Covered, What is not Covered

This manual complements the MT90220/1 Datasheet. Detailed descriptions of each functional block and each register can be found in the datasheet and are not reproduced in this document. Hardware issues such as physical layout and timing are not covered in this manual. This document does not discuss the control of the T1 or E1 framers and the ATM layer, as these initialization procedures are implementation specific.

This document does not describe the details of the IMA protocol.

The programming steps in this document should be followed in the sequence they are presented. Sequences described in this document and provided in the sample code are suggestions only - other sequences may work.

### 1.4 Related Documents

1.4.1 Data Sheet - MT90220
1.4.2 Data Sheet - MT90221
1.4.3 IMA Specification - AF-PHY-0086.000

### 1.5 Related Software

Mitel provides Windows NT device drivers for the MT90220/1 device. The included test scripts provide an example of how to program the device. The test scripts follow the same general procedures as described in this document.

The customer must provide the Link State, Group State and Group Traffic State Machines in software.

## 2.0  General Programming

### 2.1  Direct Access Method

The MT90220/1 datasheet provides the memory address and default value (at hardware reset) for each register. The datasheet indicates which registers appear on a link-by-link basis or group-by-group basis. In these cases, the first address indicated is for link or group 0. Address information may also be obtained from the header files provided with the device driver software.

### 2.2  Indirect Access Method

Some registers use an indirect access method. For example, to read the current value of a counter the programmer must first select the particular counter (e.g. bad ICP cells) and action (e.g. read) in the counter load word. The value is then read from the counter value registers (lsb, mid and msb). Note if the MT90220/1 is used in a multitasking or multi-threaded environment, common indirect accesses (e.g. reading counter values) should be protected by an appropriate mechanism (e.g. in an RTOS: use a semaphore; in a Win32 environment, use a mutex object).

### 2.3  Toggle Bit

A toggle bit facility is available as bit 6 in **RX External SRAM Control Register**.

This bit gives the programmer the ability to detect when a register has been successfully written. This may be necessary when a fast processor is used, and the programmer needs an indication that a successful write has been completed.

### 2.4  Miscellaneous

Some registers contain reserved bits. Care should be taken to write only the values specified in the MT90220/1 Data Sheet for "normal operation".

Note that although they may be referred to as Interrupt *Mask* Registers in the software and some documentation, a value of one enables the interrupt and a zero masks the interrupts for these registers.

## 3.0  IMA mode

### 3.1  Assumptions

- The number of links used for TX and RX is based on bandwidth requirements and is known. More links than the minimum required could be initialized and kept as backup. It is possible that only some of the links carry traffic.
- The RX PCM functions of any RX PCM links can be used to determine if ICP cells are received on any links. The extracted values from each link are available to validate the parameters of the RX IMA group during the start-up procedure. The extracted values can be obtained either from the RX registers or from the RX ICP cell buffers for each link. As part of the start-up procedure (as described in the IMA spec) the Near End (NE) RX side can accept or reject the parameters of a Far End (FE) TX link.
- The specific physical links to be part of a specific IMA group on the TX side must be defined at start-up.
- The TX and RX IMA groups can be asymmetric or symmetric as required by the implementation.

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### 3.2  Implemented State Machines

The MT90220/1 device implements the Cell Delineation (CD) State Machines and the IMA Frame State Machines (IFSM). The main parameters of these state machines are programmable. The current state of the CD and IFSM can be obtained by reading the **RX State Register** for a specific link.

### 3.3  Procedure

3.3.1   Initialization

3.3.1.1   IRQ and Counters

Disable all possible source of interrupt by setting all enable bits to 0 in the **IRQ Master Enable Register**. Reset all counters to zero.

3.3.1.2   Initialize Test Registers

Write 0x60 to **Test Register 1** and 0x40 to **Test Register 2.** If the MT90220/1 is used in Utopia Level 1 configuration write 0x00 to **Test Register 1.** Note that if the MT90220/1 is used in a Utopia Level 1 configuration it must be the only PHY device connected to the Utopia bus.

3.3.1.3   External RAM

Write to the **SRAM Control Register** to reflect the amount of external SRAM and the proper memory configuration. Reset the external RAM interface with the **RX External SRAM Control Register.** After a reset, the bit 7 of the **RX External SRAM Control Register** will go back to 1 indicating that the SRAM is initialized and can be used. The reset period corresponds to 256 system clock cycles.

Configure direct memory access by writing to the **Test Mode Enable Register, Delay Link Number Register** and **External Ram Control Transfer Register.**

3.3.1.4   Utopia Input FIFO (TX) Size

There are a number of Utopia TX FIFOs contained in the TX interface of the MT90220/1.There is a single Utopia TX FIFO for each of the four IMA groups and one for each links when used in UNI mode. Each of the Utopia TX FIFOs can have a maximum size of 15 cells. The recommended size for the Utopia TX FIFO for any IMA group is 1 cell and the Utopia TX FIFO for each link to be part of an IMA group is 0 cells. Select the size of each TX Utopia FIFO buffer by writing to the **TX FIFO Length Definition Registers.**

For each link that is part of an IMA group, there is an internal TX FIFO with a programmable size.

Limit the size of the internal FIFO for each link by setting the FIFO overflow and underflow values. For ITC mode, the recommended overflow limit is 5 and the recommended underflow limit is 2. For CTC mode, the recommended overflow limit is 6 and the recommended underflow limit is 1. Specify these values in the **TX IMA Control Register**. It is important to remember that the total number of cells "reserved" for all the TX FIFO buffers should be 58 cells or less. The MT90220/1 implements the internal FIFOs using the same pool of 58 user cells, so the size of the internal FIFOs must be taken into account when defining the size of all the TX FIFOs.

3.3.1.5   Cell Delineation

Write to the **Cell Delineation Register** for the proper value of the ALPHA and DELTA parameters. The same values are used for all eight CD state machines.

Write to the **Loss Cell Delineation Register** for the selected value (multiple of 2). The same value is used for all eight CD state machines. A value of zero is not allowed in this register.

3.3.1.6    IMA Frame Delineation

Write to the **Frame Delineation Register** for the proper value of the ALPHA, BETA and GAMMA parameters. The MT90220/1 uses the same parameters for each of the four IFSMs.

| Step | Register(s) | Example |
|---|---|---|
| Disable Interrupts | **IRQ_MASTER_MASK_REG**<br>**IRQ_LINK_MASK_REG** | *mask_all()* |
| Reset All Counters | **SELECT_COUNTER_REG**<br>**COUNTER_TRANSFER_REG** | *reset_all_counters();* |
| Set Test Mode Registers | **TEST_1_REG**<br>**TEST_2_REG** | |
| Configure Memory<br><br>Reset External SRAM<br><br>Set Direct Access | **SRAM_CONTROL_REG**<br><br>**EXTERNAL_RAM_CTRL_TRANSFER_REG**<br><br>**ICP_CELL_RAM_WRITE_ADDR_1**<br>**(Test Mode Enable Register)**<br>**DELAY_LINK_NUMBER_REG**<br>**EXTERNAL_RAM_CTRL_TRANSFER_REG** | *init_mem();* |
| Set TX FIFO Size<br><br><br><br><br><br><br>Set TX FIFO Over/Underflow | **FIFO_LENGTH_DEFINITION_1_REG**<br>**FIFO_LENGTH_DEFINITION_2_REG**<br>**FIFO_LENGTH_DEFINITION_5_REG**<br>**FIFO_LENGTH_DEFINITION_6_REG**<br>**MT90220 only:**<br>**FIFO_LENGTH_DEFINITION_3_REG**<br>**FIFO_LENGTH_DEFINITION_4_REG**<br>**IMA_CONTROL_REG** | *reset_tx_fifo();* |
| Cell Delineation Alpha<br>Cell Delineation Delta | **CELL_DELINEATION_REG** | |
| Loss Cell Delineation | **LOSS_CELL_DELINEATION_REG** | |
| Frame Delineation | **FRAME_DELINEATION_REG** | |

**Table 1 - General**

3.3.1.7    TX Utopia Interface

The TX Utopia Clock must be active for the Utopia Input registers to be operational.

If configuring the first IMA group, reset the Utopia interface by writing to the **Utopia Input Control Register**.

Select the various TX Utopia options in the **Utopia Input Control Register**.

Disable the Utopia ports associated with the links to be used in IMA mode, by writing to the **Utopia Input Link PHY Enable Register**. (These ports correspond to the links used in UNI mode).

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Define the PHY address for the IMA group by writing to the **Utopia Input Group Address Register**.

| Step | Register(s) | Example |
|---|---|---|
| Reset TX Utopia | **UTOPIA_INPUT_CONTROL_REG** | |
| Disable Utopia links PHY that will be in IMA mode | **UTOPIA_INPUT_LINK_PHY_ENABLE** | |
| Define PHY Addresses | **UTOPIA_INPUT_GROUP_ADDRESS_REG** | |

**Table 2 - TX Utopia Interface**

### 3.3.1.8   TX PCM

Verify that the RX PCM clock or REF clock to be used is active by reading the **Clock Activity Register**.

Select the TX clock source by writing to the **TX PCM Link Control Register #2**. Note that all the links in an IMA group must have the same data rate but can have different clock sources.

Write to the **TX PCM Link Control Register #1**. Select PCM format and force outputs to high impedance mode until TX PCM configuration is completed. (After a reset, the outputs are in high impedance mode).

Select the source for the 2 PLL reference signals (output pins), if required, by writing to the **PLL Control Register**.

Set the outputs as active (no longer in high impedance mode) by writing to the **TX PCM Link Control Register #1**.

| Step | Register(s) | Example |
|---|---|---|
| Verify Reference Clock | **CHECK_CLOCK_AVAILABLE** | |
| Select TX Clock Sources | **TX_PCM_LINK_CONTROL_REG_2** | *configure_tx_pcm();* |
| Select PCM Format Force Outputs to Hi-Z | **TX_PCM_LINK_CONTROL_REG_1** | |
| Select Source for PLL Signals | **PLL_REFERENCE_CONTROL_REG** | |
| Set Outputs to Active | **TX_PCM_LINK_CONTROL_REG_1** | |

**Table 3 - TX PCM**

### 3.3.1.9   TX IMA

Write to the **TX Group Control Register** corresponding to the IMA group number to be initialized. Specify the value of M, the timing mode and the reference link number (physical link number).

Write to **TX Link ID Registers** for each link used in an IMA group. The link ID value is between 0-31 and the physical link number is between 0-7 for the MT90220, and between 0-3 for the MT90221. The LID should not be changed when a group is operational (Do not use the same LID for more than 1 link in an IMA group, as there is no H/W verification for this case).

Write to **TX ICP Cell Offset Registers**. This value depends on the value of M.

Typically, the reference link will have a delay of 0 cells in the IMA frame and each other link would be evenly spaced in multiple of M/N cells where N is the number of links in the IMA group. Do not change the ICP cell offset value once a group is operational.

Write to the **TX IDCR Integration Register**. Refer to the MT90220/1 Data Sheet for the suggested values.

Write to the **TX IMA Control Register** to select the stuff event notification (notification 4 or 1 IMA frames before the stuff event).

Initialize the TX ICP Cell content. Note that the TX OAM label (per group) is set in this ICP cell. Wait for the ready flag in the **ICP Cell Handler Register** to be set and then write to each one of the ICP cell bytes that are under the control of the software. The MT90220/1 calculates the HEC and CRC values automatically. Initiate the transfer by writing zero to the READY bit associated with the IMA group in the **ICP Cell Handler Register**. When the transfer is complete, the bit value returns to one.

The reference link must be the first link added and enabled in a TX IMA group to ensure the proper operation of the device.

Write to the **TX Link Control Register** to select the scrambling option, coset option, and send filler cells option. Adding a link to a TX IMA group must be done in two steps. Write the physical IMA group number (from 0-3) to the **TX Link Control Register.** Enable the IMA mode bit (bit 2) in this register. The link should be enabled to send user cells only when the corresponding receive group is active or when the TX Utopia port is not active.

Before adding additional links, verify that the TX reference link is in IMA mode by reading the **TX IMA Mode Status** Register. The link is reported in IMA mode when the corresponding bit in the TX IMA Status register is cleared (reads 0).

Note that the amount of time required for a link to go from UNI to IMA mode is 30 syst clock cycles in addition to the time required to empty the internal TX link FIFO. Typically, when going from UNI to IMA mode, no User cells are sent on that link, so the TX Link FIFO should have an average of 2 Idle cells. For T1, the time to go in IMA mode would be approx. 0.55 msec.

Additional TX links should be added one at a time. When adding links to the TX IMA group, enable the differential delay optimization mode by writing (0x48 + IMA group number) to **Test Register 2.** This ensures that the TX Differential delay between the TX links is less than 2.5 cell time. Write to the **TX Link Control Register** to select the scambling option, coset option, and send filler cells option. Again, adding a link to a TX IMA group must be done in two steps. Write the physical IMA group number (from 0-3) to the **TX Link Control Register.** Then enable the IMA mode bit (bit 2) in this register. Before continuing, verify that the link is in IMA mode by reading the **TX IMA Mode Status Register.** Once IMA mode is confirmed, reset the **Test Register 2** to 0x40.

| Step | Register(s) | Example |
|---|---|---|
| Set M Value<br>Set Timing Mode<br>Set Reference Link | **TX_GROUP_CONTROL_MODE_REG** | |
| Set Logical Link IDs | **TX_LINK_ID_REG** | |

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| Step | Register(s) | Example |
|---|---|---|
| Set ICP Offsets | **ICP_CELL_OFFSET_REG** | |
| Set TX IDCR Integration Value | **MEASURE_PERIODE_REG (TX IDCR Integration Value)** | |
| Set Stuff Event Notification | **IMA_CONTROL_REG** | |
| Initialize and Transfer ICP Cell Content | **ICP_CELL_HANDLER_REG** | |
| (Add Reference Link First) Select Coset Option Select Scrambling Option Send Filler Cells Select IMA Group Number | **TX_LINK_CONTROL_REG** | |
| Enable IMA Mode | **TX_LINK_CONTROL_REG** | |
| Confirm TX IMA Mode | **IMA_MODE_STATUS_REG** | |
| (Add Additional Links) Enable Optimize TX Differential Delay Mode Select Coset Option Select Scrambling Option Send Filler Cells Select IMA Group Number | **TEST_2_REG** **TX_LINK_CONTROL_REG** | |
| Enable IMA Mode | **TX_LINK_CONTROL_REG** | |
| Confirm TX IMA Mode | **IMA_ MODE_STATUS_REG** | |
| Disable Optimize TX Differential Delay Mode | **TEST_ 2_REG** | |

**Table 4 - TX IMA**

3.3.1.10  RX Utopia interface

The RX Utopia clock must be active for the MT90220/1 Utopia output registers to be operational.

If it is the first group to be setup, reset the Utopia interface by writing to the **Utopia Output Group PHY Enable Register**.

Disable the Utopia ports associated with the links used in IMA mode by writing to the **Utopia Output Link PHY Enable Registers** (These ports correspond to the links when configured in UNI mode).

Define the PHY address for the IMA group by writing to the **Utopia Output Group Address Register**.

Clear the **RX Utopia FIFO Link Register** and **RX Utopia Group Overflow Status Registers** and mask the interrupt generation for overflow conditions.

| Step | Register(s) | Example |
|---|---|---|
| Reset Utopia RX (output) | **UTOPIA_OUTPUT_ADDR_ENABLE_1**<br>**(Utopia Output Group PHY Enable Register)** | |
| Disable Links in IMA Mode | **UTOPIA_L2_OUTPUT_ADDR_0**<br>**(Utopia Output Link PHY Enable Register)** | |
| Define Utopia Output Group PHY Addresses | **UTOPIA_L2_OUTPUT_ADDR_1**<br>**(Utopia Output Group Address Register)** | |
| Clear RX Utopia FIFO Link Overflow Register<br>Clear RX Group Overflow Register | **RX_LINK_FIFO_OVERFLOW_ENABLE_REG**<br>**RX_IMA_FIFO_OVERFLOW_ENABLE_REG** | |

**Table 5 - RX Utopia**

3.3.1.11  RX PCM

Write to the **RX PCM Link Control Registers** for the PCM Mode, clock and SYNC signal polarity and enable the RX PCM circuitry. All the links in an IMA group must have the same data rate.

Write to the **RX Link Control Registers** to select counting all the cells or only the stuff cells, to enable the descrambler if required, to remove unassigned, idle and HEC errored cells and to select the coset option, if required. Do not activate the IMA mode yet.

| Step | Register(s) | Example |
|---|---|---|
| Configure RX PCM Format | **RX_PCM_LINK_CONTROL_REG** | *configure_rx_pcm();* |
| Configure RX Link Parameters | **RX_LINK_CONTROL_REG** | *configure_rx_link();* |

**Table 6 - RX PCM**

3.3.1.12  RX IMA

Set the OAM label value for the RX IMA Group in the **OAM Label Register.**

Ensure the RX IMA mode is off in the **RX Link Control Register**.

Wait for cell delineation to be achieved, by using the **RX Load Values Register** to specify the RX link and read the cell delineation state in the **RX State Register**. After the Cell Delineation is achieved, it is suggested to wait for at least 1 IMA frame before reading the values from an incoming ICP cell. The RX ICP Cell interrupt can be used to indicate when an ICP cell is received .

Verify if a physical RX link is to be part of an IMA group. With the IMA mode off (in the **RX LINK Control Register**), enable the RX PCM link (**RX PCM Link Control Register**). Access the key parameters of the RX IMA group for each link by issuing an RX Load Values command with a link number as argument. Read the updated **RX Link IMA ID Register, RX Link ICP Offset Register, Link ID Register, Reference ID Register and RX State Registers**. Use these read-only values to determine which physical RX link is part of which physical and logical IMA group.

Alternatively, collect all the valid RX ICP cells from a link into the RX ICP cell buffer. Write to the **RX ICP Cell Type RAM Registers** to configure accumulation of all valid ICP cells. Read the RX ICP cell contents from the RX ICP cell buffers to obtain the IMA ID, Link ID, Reference Link ID, ICP Cell Offset, etc.

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Based on the above information, initialize the **RX Reference Link Control Register** for the IMA group. Initialize the **RX Recombiner Registers** to specify which physical link belongs to which physical IMA group. Do not enable the recombiner process yet.

Read the various delays of each link by first issuing a command through the **RX Delay Select Register** and then reading the **RX Delay MSB** and **RX Delay LSB Register** and **RX Delay Link Number Register**.

Write to the **RX Maximum Operational Delay Register** and the **Guardband/Delta Delay Registers** for the acceptable values based on the amount of memory and the actual delay of the links. It is recommended to use a guardband of at least 4 cells and to define the value for the RX maximum operational delay to be[ 6 cells + maximum differential delay in cells] (i.e. always keep the equivalent of 6 cells SRAM space for jitter and wander that can be introduced by the stuff events and ITC clocking mode.)

Note that the MT90220/1 uses the RX maximum operational delay parameter to generate an LODS indication. It is possible to detect an LODS condition and still have the recombiner process operating correctly as long as there is enough memory to accommodate the delay.

Write to the **RX IDCR Integration Register**; refer to the MT90220/1 Data Sheet for the suggested values.

Enable the IMA mode by turning on the IMA bit in the **RX LINK Control Registers**.

Verify that the RX link achieved IMA frame synchronization after at least "GAMMA + 2" IMA frames. Issue a command to the **RX Load Values Register** to specify the RX link and read the IMA frame state in the **RX State Register**. If the synch. state is not achieved, a simple fix routine must be executed to correct this situation. (Workaround: Configure the RX link in UNI mode and then back in IMA mode by writing to the **RX Link Control Register**. The synch state should be acquired within "GAMMA + 2" IMA frames.)

Set or reset the IRQ mask registers using the **Enable Counter Register**, the **IRQ Link Enable Register** and the **IRQ Master Enable Register**. Enable the IRQ generated by the RX PCM block and the various counters and overflow IRQs.

Note that the PCM interfaces must be configured and working properly for the internal scheduler to work properly.

| Step | Register(s) | Example |
|------|-------------|---------|
| Set RX OAM Label | **OAM_LABEL_REG** | |
| Ensure RX IMA Mode is Off | **RX_LINK_CONTROL_REG** | |
| Enable RX PCM | **RX_PCM_LINK_CONTROL_REG** | |
| (Enable TX PCM) | **TX_PCM_LINK_CONTROL_REG_1** | |
| Confirm Cell Delineation | **LOAD_VALUES** **RX_STATE_REG** | *wait_for_cell_delineation();* |

| Step | Register(s) | Example |
|---|---|---|
| Validate RX Information (Load Values Method) | **LOAD_VALUES**<br>**RX_LINK_IMA_ID_REG**<br>**RX_LINK_ICP_OFFSET_REG**<br>**RX_LINK_ID**<br>**RX_LINK_REF** | *validate_rx_info();* |
| Validate RX Information (RX ICP Method) | **RX_ICP_CELL_TYPE_LINK_0**<br>**RX_ICP_CELL_TYPE_LINK_1**<br>**RX_ICP_CELL_TYPE_LINK_2**<br>**RX_ICP_CELL_TYPE_LINK_3**<br>**MT90220 only:**<br>**RX_ICP_CELL_TYPE_LINK_4**<br>**RX_ICP_CELL_TYPE_LINK_5**<br>**RX_ICP_CELL_TYPE_LINK_6**<br>**RX_ICP_CELL_TYPE_LINK_7** | *validate_rx_icp_info();* |
| Set RX Reference Link | **REF_LINK_CONTROL_REG** | |
| Assign Links to RX Recombiner | **RECOMBINATION_CONTROL_REG** | |
| Read Delays | **SRAM_POINTER_ADDRESS_REG**<br>**DELAY_MSB_REG**<br>**DELAY_LSB_REG**<br>**DELAY_LINK_NUMBER_REG** | *dump_delays();* |
| Guardband Delta Delay | **GUARDBAND_DELTA_DELAY_LSB_REG**<br>**GUARDBAND_DELTA_DELAY_MSB_REG** | |
| Maximum Operational Delay | **MAXIMUM_OPERATIONAL_DELAY_LSB_REG**<br>**MAXIMUM_OPERATIONAL_DELAY_MSB_REG** | |
| RX Integration Period | **MEASURE_PERIOD_REG**<br>**(RX IDCR Integration Value)** | |
| Enable RX IMA Mode | **RX_LINK_CONTROL_REG** | |
| Wait for IMA Frame Sync | **LOAD_VALUES**<br>**RX_IMA_FRAME_STATE** | *wait_for_ima_sync();* |

**Table 7 - RX IMA**

3.3.2  Start-up

At this stage, the TX links are transmitting ICP cells, filler cells and stuff cells. When the RX links have successfully acquired cell delineation and IMA frame synchronization, enable the RX Utopia interface (MT90220/1 to ATM) for the IMA group by writing to the **Utopia Output Group PHY Enable Register**. Enable the recombiner circuitry by writing to the **RX Recombiner Registers**. There is one limitation: when adding the first link, the recombining process CANNOT have the recombiner delay option active. The RX link recombiner is reported active when the enable recombiner status bit associated with this specific link is set. This bit is located in the **Enable Recombination Status Register**.

The status of all links that are part of an IMA group should be constantly monitored (by managing the IRQs, polling status registers and reading the **RX State Register**.)

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Read the content of the received ICP cells to verify the status of the FE RX links.

When all the conditions are met, enable the transmission of user cells by writing to the **TX Link Control Register** (bit 6) of the reference link. Enable the Utopia interface (ATM to MT90220/1) for the group by writing to the **Utopia Input Group PHY Enable Register**. Typically, enable the TX sequencer to send user cells through the links before enabling the Utopia input port (from ATM to MT90220/1 device).

| Step | Register(s) | Example |
|---|---|---|
| Enable RX Utopia | UTOPIA_OUTPUT_ADDR_ENABLE_1 | |
| Enable Recombiner | RECOMBINATION_CONTROL_REG | *enable_recombination();* |
| Confirm Recombination | ENABLE_RECOMBINATION_STATUS | |
| Monitor IMA Status | LOAD_VALUES<br>RX_STATE_REG | |
| Start TX of User Cells | TX_LINK_CONTROL_REG | |
| Enable TX Utopia interface | UTOPIA_INPUT_GROUP_PHY_ENABLE | |

**Table 8 - Start-up**

### 3.3.2.1 TX ICP

Update the ICP cell and send it to the FE by issuing the transfer command. The ICP cell is "built up" in a scratch pad area and may include more than one change. All the changes will be part of the same ICP cell when the transfer command is issued.

| Step | Register(s) | Example |
|---|---|---|
| Transfer a Changed ICP cell | ICP_CELL_HANDLER_REG | *transfer_icp_buffer();* |

**Table 9 - TX ICP**

### 3.3.2.2 Counters

When the device declares the IMA group operational, reset the various counters and status registers. Enable the various sources of interrupt at this point.

| Step | Register(s) | Example |
|---|---|---|
| Reset All Counters | SELECT_COUNTER_REG<br>COUNTER_TRANSFER_REG | *reset_all_counters();* |
| Enable IRX ICP IRQ | IRQ_MASTER_MASK_REG<br>IRQ_MASTER_STATUS_REG<br>IRQ_LINK_MASK_REG<br>IRQ_LINK_STATUS_REG | *validate_rx_icp_irq();* |
| Enable Counter IRQ | SELECT_COUNTER_REG<br>COUNTER_TRANSFER_REG | *link_counter_irq();*<br>*group_counter_irq();* |

**Table 10 - Counters/IRQ**

### 3.3.3   Ongoing Operation

#### 3.3.3.1   ICP Cells

The MT90220/1 monitors the received ICP cells for the status & control change indication byte. The device will generate an interrupt if an ICP cell with changes is received (if configured to do so by enabling the IRQs and selecting "collect the RX ICP cells with changes" in the RX ICP cell buffer).

During operation, various events or error conditions external to the MT90220/1 may affect the LSM, GSM, GTSM or MIB interface. The software must inform the FE of these changes by updating and transmitting an ICP cell.

#### 3.3.3.2   IRQ Processing

There are many sources for interrupt and each may be enabled individually.

The IRQ status registers are organized on a per link basis. The **IRQ Master Status Register** is read first to find out which link(s) requested services and then the **IRQ Link Status Register** is read to find out the exact source of interrupt. IMA group related interrupts appear cascaded through bit 7 of the **IRQ Link Status Register** for link 0. See Section 7.0 for a detailed diagram of the interrupt structure.

#### 3.3.3.3   Worst Case

The "valid ICP cell with changes is received" interrupt is time critical. The software program has two IMA frames cell time to react to this new ICP cell. Up to one IMA frame time can be necessary between the update of the TX ICP cell and the time it is transmitted on the TX link. The one IMA frame time remains to detect an ICP cell with changes, read it, determine what has changed, react to it and update the TX ICP cell accordingly.

The time available to process the IRQ is directly dependent on the value of M (length of one IMA Frame), the link data rate and the number of IMA groups. For a value of M=32, one IMA group of E1 links, an IMA frame time corresponds to approximately 7 msec. (For a value of M=256, one IMA frame time equates to approximately 56 msec and for M=128, it corresponds to 28 msec.).

If the four IMA groups generate interrupts at the same time, the "one IMA frame/4" corresponds to 1.7 msec available to service the interrupt for each group. In the typical case where M=128, the time available to service the IRQ is approximately 7 msec.

Similar discussion is applicable in the case where the device receives new ICP cells with changes in consecutive IMA frames. The software program has up to one IMA frame time to process the received ICP cell.

#### 3.3.3.4   IRQ Latency

The most time critical delay to assert an IRQ corresponds to the case where the MT90220/1 receives a new ICP cell. The device generates an IRQ signal approximately 25 usec after the RX PCM interface receives the last byte of the ICP cell.

#### 3.3.3.5   Support for the Group Status and Control (GSC) Field

As per the IMA spec, the MT90220/1 must send an ICP cell as soon as possible to reflect any changes -- except for changes in the Group Status and Control (GSC) field. In GSC field case, the device must send the GSC information for at least two IMA frames. A maskable interrupt can be generated at the end of the TX IMA frame. The software can use this feature to implement a two-frame counter. The IMA frame IRQ would be enabled when the GSC field is updated and the TX ICP cell is transferred from the

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scratch pad to the internal memory. The software would have to wait for an IMA frame IRQ to get the end of a frame indication, count two additional IMA frame IRQs and then mask this interrupt and record that new GSC information can be sent. (i.e. three IRQs must be acknowledged to confirm at least two complete TX IMA frames).

### 3.3.3.6   RX ICP Cell Buffers

The MT90220/1 can generate an interrupt when a cell meeting the selected criteria is saved in the RX ICP cell buffer.

For simplification, the following section assumes that the RX ICP cell buffer is programmed to collect new RX ICP cells with changes.

The MT90220/1 stores the last processed RX ICP cells and can store the next two ICP cells with changes in a circular buffer. However, if the circular buffer reaches the level of two new cells, all the following ICP cells with changes received are not saved. In such a case, a procedure must be implemented to read the SCCI value of the last cell in the RX ICP cell buffer and then compare this value with the value of the SCCI field of the most recent RX ICP cell. This value can be obtained by issuing an RX Load Value command and then reading the **RX Link SCCI Sequence Number Register**. In the case where one or more RX ICP cells with changes were missed, the software could capture the current RX ICP cell by electing to collect in the RX ICP Cell buffer all the valid RX ICP cells to process the latest values (of the RX IMA group). Then, the software would reconfigure the RX ICP cell buffer to collect only the RX ICP cells with changes.

### 3.3.4   Additional Procedures

### 3.3.4.1   Adding A TX Link

To add a TX link, follow part of the general setup procedure described in the start-up of an IMA group (handshaking between the FE and NE is not discussed here). To add a TX link, first set the various link and group parameters. The ICP cell and filler cells are sent on this link until the link is ready to be activated. The link will become part of the TX IMA group sending user cells when the bit 6 of the **TX Link Control Register** is set to 1. Assign a valid ICP cell offset value to the new link. The offset values for previously active links should not be changed.

### 3.3.4.2   Removing A TX Link

To delete a link from a TX IMA group, use the reverse of the start-up procedure. Assuming no error or problem, the NE TX side should notify the FE of the intent to stop sending traffic. The TX link would send ICP cell and filler cells until it is time to remove the link from the IMA group. To stop sending user cells, set bit 6 of the **TX Link Control Register** to 0. When the FE RX link acknowledges the deletion procedures (and the RX buffers are cleared), configure the link into UNI mode by writing to the **TX Link Control Register** (bits 2-0). Finally, configure the PCM interface to be in high impedance mode by writing to the **TX PCM Link Control Registers**.

When deleting the last link of a TX IMA group, stop sending user cells from the ATM layer by disabling the TX Utopia interface by writing to the **Utopia Input Group PHY Enable Register**. Wait for the TX Utopia Group FIFO to be empty (using the **TX Utopia FIFO Level Register**) before configuring the link as UNI mode.

### 3.3.4.3   Changing Direction of TX Clock

The following procedure should be followed when changing the direction of the TX Clock ( TXCK ) from an input to an output. Turn off the clock source that drives TXCK. Set bit 7 in the **PLL Reference Control Register** to reset the clock selection state machine. Write to the **TX PCM Link Control Register #2** to set the correct RXCLK. Then set the TXCK to be an output.

Note that if TXCK is set as an input and the clock is not present, all other links in the group will be affected. The **Clock Activity Register** for the particular link should be used to verify the presence of a clock before configuring TXCK as an input.

### 3.3.4.4   Disabling a TX Group

The procedure to delete all the links in a TX IMA group is as follows:

Stop sending user cells from the ATM layer by disabling the TX Utopia interface by writing to the **Utopia Input Group PHY Enable Register**.

Stop sending user cells (send filler cells) after the TX Utopia FIFO is cleared on all the links and wait for feedback from the FE RX to report that it has cleared all the received user cells. Writing to bit 6 of the **TX Link Control Registers** does this.

Reconfigure the links to be in UNI mode by writing to the **TX Link Control Registers.** Configure the PCM interface to be in high impedance mode by writing to the **TX PCM Link Control Registers**.

### 3.3.4.5   Adding an RX Link

Follow part of the general IMA start-up procedure to add an RX link. Configure and enable the RX PCM port. Validate the parameters received on the link. Assign the link to an IMA group by writing to the **RX Recombiner Register** and then enable IMA mode by writing to the **RX Link Control Register**. Receive ICP cells and filler cells until the FE TX link is ready to be activated. Enable the RX link recombiner process (bit 2 of the **RX Recombiner Register** is set to 1). The MT90220/1 will start collecting cells when the Enable Recombination Status bit is set to 1. The Recombiner Delay Control bit can be activated to wait until the occurrence of the first user cell to automatically add the link in the effective recombiner process (included in IDCR calculation). This bit is found in the **RX Recombiner Delay Control Register** and is reset when the link is added to the RX IMA recombiner process.

### 3.3.4.6   Removing an RX Link

When removing one or more links but still keeping an IMA group operational with other active links, implement the reverse procedure of adding a link. Assuming no error or problem, first the FE TX must stop sending user cells. Remove the NE from the recombiner process (after all the received user cells are recovered from SRAM) by writing to the **RX Recombiner Register**. Configure the link in UNI mode and disable the RX PCM block by writing to the **RX PCM Link Control Register**.

### 3.3.4.7   Disabling an RX IMA Group

The procedure to delete all the links in an RX IMA group is as follows:

Stop the recombiner process for the RX links after the FE TX stopped sending user cells on the link(s). The recombiner process should be stopped only after the last received user cell is transferred to the ATM layer through the RX Utopia interface. This delay corresponds to the differential delay between the fastest and slowest links of the IMA group. Stop the recombiner process by writing to bit 2 of the **RX Recombiner Registers** associated with the links.

Wait for the recombiner process to be reported as stopped by reading the **Enable Recombination Status Register**. Reconfigure all the links in UNI mode by writing to the **RX Link Control Registers**. Configure the PCM interface in high impedance mode by writing to the **RX PCM Link Control Registers**.

### 3.3.4.8   Reading a Delay

Internal registers that hold the various link delay values are accessible through indirect access. The delay values are reported in number of cells and the equivalent time can be determined based on the

trunk type. For E1 (30 channels per frame), a cell is approximately 0.221 msec; for T1 (24 channels per frame), a cell time is approximately 0.276 msec; and for T1 ISDN (with 23 channels per frame), a cell time is approximately 0.288 msec. The link number and delay type are first selected by writing to the **RX Delay Select Register**. After 2 system clock cycles, the value in the **RX Delay MSB Register** and **RX Delay LSB Register** and the **RX Delay Link Number Register** are updated and can be read. The valid delay types are: the maximum delay over time, the current maximum delay, the current minimum delay for an IMA group and the current delay value for any links. Obtain the differential delay value by comparing the delay values of each link.

3.3.4.9   Using the Guardband/Delta Delay Register

The MT90220/1 device calculates the positions of the RX read and write pointers automatically when a link is declared part of an IMA group (before the recombiner process is enabled). In a typical start-up procedure, all the links declared part of an IMA group would have their operating mode defined as IMA. So, each time the IMA bit is enabled for a link, and as long as none of the recombiner bits are enabled for any of the links that are part of the IMA group, the position of all read and write pointers is recalculated. The minimum recombiner delay will be detected on the link having the longest transmission delay (the slowest link). The maximum recombiner delay will be detected on the link that is having the shortest transmission delay (the fastest link). As soon as one link has its recombiner bit turned on, the relative positions of the read and write pointers are frozen.

If the link to be added is slower than the slowest operational link, an LODS condition could be detected and a negative value for the link delay will be reported when the link delay value is read. To correct the situation, the pointer positions must be changed. This causes a disruption in the recombining process. To alleviate this problem, add an additional recombiner delay to the slowest link when initializing the group. Specify this additional delay in the **Guardband/Delta Delay Register**. If the link to be added is slower than the slowest operational link, but with the added delay is within the guardband value, then the link can be added without any disruption. This changes the current guardband of the group. Read the new guardband value by reading the current minimum delay of the IMA group.

If a link to be added has a delay value which falls beyond the worst delay value including the guardband, then there are 2 options: either reject the link or re-adjust the pointers. To readjust the pointers, specify a delta value which is the amount of extra delay to be added to the current recombiner delay (writing to the **Guardband/Delta Delay Register**) and then issue a command to increase the delay in the **Increment/Decrement Delay Control Register**. The MT90220/1 stops the recombining process for the time specified and then resumes the recombining process. No cell is lost, but there is an effect on the CDV. The device completes the increment process when the control bit used to initiate the correction returns to a zero value.

If a link to be added to an existing IMA group exhibits a transmission delay shorter than the current shortest link, then an LODS condition is generated if the new write pointer position is beyond the RX Maximum Operational Delay value. This is reported by a delay value that is positive and with a delay value that is greater than the current RX Maximum Operating Delay. In this situation, if the total differential delay can be accommodated by the amount of external SRAM, increase the RX Maximum Operational Delay value by writing to the **RX Maximum Operational Delay Registers**.

If a link to be removed from an IMA group is not the slowest link, no change is necessary in the recombiner delay.

If a link to be removed from an IMA group is the link with the largest delay, then the recombiner delay could be re-adjusted to remove part of the extra delay which is not required anymore. **The Guardband/Delta Delay Register** is used to specify the delay to be removed (in number of cells time) and then a command is issued to remove the delay. Use the **Guardband/Delta Delay Register** and the **Increment/Decrement Delay Control Register** for this operation. This MT90220/1 device recalculates

the pointers and drops all the cells between the old and new read pointer positions. This correction is not automatic - the user initiates the procedure.

### 3.3.4.10 Use of RX Maximum Operational Delay

The amount of reserved external memory for an operating IMA group is programmable. The amount of external memory defines the total amount of differential delay that the MT90220/1 may handle for an IMA group. The value of the RX Maximum Operational Delay defines what is accepted as valid for the current conditions. Specify the value of delay in the four **RX Maximum Operational Delay Registers**. The value does not have to be identical for all IMA groups. The total delay in each of the four registers cannot be larger than what can be accommodated by the external SRAM (less a safety margin). Refer to the MT90220/1 Data Sheet for the proper method to determine how much delay can be absorbed by any specific memory configuration.

### 3.3.4.11 CDV Performance

The configuration of the MT90220/1 can be "tuned" to achieve the best CDV performance. The IDCR integration period is a critical factor that effects the CDV performance. The period must be programmed to be as close as possible to an integer number of cells which should be as big as possible. The type of traffic (CBR vs. VBR) to be carried is also an important factor. Please refer to the proper section in the MT90220/1 Data Sheet for more details.

### 3.3.4.12 Calculation of RX User Cells in IMA mode

The total number of User cells is obtained by subtracting the number of HEC errors and number of Idle cells from the total number of cells and should reflect the correct number of User cells. The accuracy for each time period could be +/- a few cells but the total number over time is always accurate.

In IMA mode, the total number of User cells for a RX link can be evaluated using the following equation:

$$UserCells = TotalCells - \left[ TotalCells \times \frac{(M-1)}{M} \right] - \left[ TotalCells \times \left( \frac{2048}{2049} \right) \right]$$
$$- TotalFillerCells - TotalBadICPCells - TotalCellsWithHecError$$

The term:

$$\left[ TotalCells \times \frac{(M-1)}{M} \right]$$

determines how many ICP cells were received.

The term:

$$\left[ TotalCells \times \left( \frac{2048}{2049} \right) \right]$$

determines the average number of Stuff events.

The total number of User cells for an IMA group is the sum of the User Cells for all the links that are part of the IMA Group.

To support most MIBs, the user must read the various counters periodically, and report the number of cells for the last time interval. Because the counters may not be accessed at exactly the same time, there may be an inaccuracy of a few cells due to the time required to read each counter. For example, the time to receive a cell is approximately 0.2 msec and if the read process is relatively slow, some counters could get incremented before all the counters are read and reset. This would cause an

inaccuracy of a few cells for the current time period. If the counters are accumulated over time ( much greater than the reporting time period ), no cells will be missed and the total number will always be correct. Alternatively, the correct number of User cells could be obtained from the Utopia ATM Controller.

3.3.4.13  Recovery from RX Utopia Group Overflow Condition

The preferred way to recover from the RX Utopia Group Overflow Interrupt ( as reported in **IRQ IMA Overflow Status Register**, bit 4 ) is to remove the links from the recombiner, let the RX FIFO deplete (i.e. do not disable the RX Utopia port ), reset the IRQ status bit ( by writing a zero to it ) and then add the links back into to the recombiner.

Because each link is first configured in UNI mode to collect IMA information contained in incoming ICP cells, an RX Link Utopia overflow condition may occur (as reported in the **IRQ Link UNI Overflow Status Register**, bit 4). In this case the Overflow condition may be ignored since the links will later be added to an IMA group. The only way to clear this overflow is to enable the corresponding RX (link) Utopia port.

## 4.0  UNI (non-IMA) Mode

This checklist provides a typical sequence to initialize and use the MT90220/1 in an implementation where the T1/E1 links are used in UNI (non-IMA). The intent is to provide some information on the device interface and operation.

### 4.1  Assumptions

- The number of links used for TX and RX is based on bandwidth requirements and is known. More links than the minimum required can be initialized and kept as backup. It is possible that only some of the links carry traffic.
- The specific physical links used for the TX and RX directions are identified at start-up. The MT90220/1 is configured accordingly using the various registers described below. The TX and RX circuitry is totally independent so that the device may carry UNI traffic over different physical TX and RX links. For example, the TX direction can be carried over physical link 1 and the RX traffic can be received through the physical RX link 3.
- The control of the T1 or E1 Framers and the ATM layer is not discussed here, as these procedures are implementation specific.
- Utopia addresses associated with the physical links for both in TX and RX are programmable.
- No external SRAM is required for UNI mode and therefore, no SRAM initialization is necessary.

### 4.2  Implemented State Machines

The MT90220/1 implements the individual link Cell Delineation (CD) State Machines and the main parameters of these state machines are programmable. The current state of CD can be obtained at any time by reading a specific register.

**4.3  Procedure**

4.3.1  Initialization

4.3.1.1  IRQ

Disable all possible sources of interrupts by setting all enable bits to zero in the **IRQ Master Enable Register**. Reset all counters.

4.3.1.2  Initialize Test Registers

Write 0x60 to **Test Register 1** and 0x40 to **Test Register 2.** If the MT90220/1 is used in Utopia Level 1 configuration write 0x00 to **Test Register 1.** Note that if the MT90220/1 is used in a Utopia Level 1 configuration it must be the only PHY device connected to the Utopia bus.

4.3.1.3  Utopia Input FIFO Size

Select the size of each TX Utopia FIFO buffer by writing to the **TX FIFO Length Definition Registers**. The total of all the FIFO buffer size should be 58 cells or less. Please refer to the discussion about the size of the TX FIFO in the IMA setup section for more details.

4.3.1.4  Cell Delineation

Write to the **Cell Delineation Register** for the proper value of the cell delineation parameters.

Write to the **Loss Cell Delineation Register** for the proper loss cell count (a multiple of 2). The same values are used for all 8 CD state machines. Do not use a value of zero for this register.

4.3.1.5  TX Utopia Interface

Reset the Utopia interface, if required, and select the various options by writing to the **Utopia Input Control Register**.

Define the PHY Address(es) for the links in UNI mode by writing to the **Utopia Input Link Address Register(s)**.

4.3.1.6  TX PCM Info

Verify that the RX Clock or REF Clock is active by using the **Clock Activity Register**.

Select the TX Clock Source by writing to the **TX PCM Link Control Registers #2**.

Write to the **TX PCM Link Control Registers #1.** Select the PCM format and force the outputs to high impedance mode until the TX PCM configuration is complete. (Note: after a reset, the outputs are in high impedance mode).

Select the source for the two PLL reference signals (output pins), if required, by writing to the **PLL Control Register**.

Outputs can be made active (no longer in high impedance mode) by writing to the **TX PCM Link Control Registers #1**.

4.3.1.7  Link Info

Specify the UNI mode and cell scrambling option by writing to the **TX Link Control Register**. User cells are transmitted over the UNI link when the **Utopia Input Link PHY Enable Register** bit is set to 1.

| Step | Register (s) | Example |
|---|---|---|
| Disable Interrupts | **IRQ_MASTER_MASK_REG**<br>**IRQ_LINK_MASK_REG** | *mask_all()* |
| Reset All Counters | **SELECT_COUNTER_REG**<br>**COUNTER_TRANSFER_REG** | *reset_all_counters();* |
| Set Test Mode Registers | **TEST_1_REG**<br>**TEST_2_REG** | |
| Set TX FIFO Size<br><br><br><br><br><br><br><br>Set TX FIFO Over/Underflow | **FIFO_LENGTH_DEFINITION_1_REG**<br>**FIFO_LENGTH_DEFINITION_2_REG**<br>**FIFO_LENGTH_DEFINITION_5_REG**<br>**FIFO_LENGTH_DEFINITION_6_REG**<br>**MT90220 only:**<br>**FIFO_LENGTH_DEFINITION_3_REG**<br>**FIFO_LENGTH_DEFINITION_4_REG**<br>**IMA_CONTROL_REG** | *reset_tx_fifo();* |
| Cell Delineation Alpha<br>Cell Delineation Delta<br>Loss Cell Delineation | **CELL_DELINEATION_REG**<br><br>**LOSS_CELL_DELINEATION_REG** | |
| Reset TX Utopia | **UTOPIA_INPUT_CONTROL_REG** | |
| Disable Utopia Links PHY that will be in IMA mode | **UTOPIA_INPUT_LINK_PHY_ENABLE** | |
| Define PHY Addresses | **UTOPIA_INPUT_GROUP_ADDRESS_REG** | |
| Verify Reference Clock | **CHECK_CLOCK_AVAILABLE** | |
| Select TX clock sources | **TX_PCM_LINK_CONTROL_REG_2** | *configure_tx_pcm();* |
| Select PCM Format<br>Force Outputs to Hi-Z | **TX_PCM_LINK_CONTROL_REG_1** | |
| Set TX UNI Link Number<br>Select Link Options | **TX_LINK_CONTROL_REG** | |
| Start Sending User Cells | **UTOPIA_INPUT_LINK_PHY_ENABLE** | |
| Confirm TX UNI Mode | **IMA_MODE_STATUS_REG** | |

**Table 11 - TX UNI Mode Setup**

4.3.1.8 RX Utopia Interface

Write to **Utopia Output Group PHY Enable Register** (to reset the Utopia interface and to disable links in IMA mode).

Write to **Utopia Output Link Address Register** to define UNI PHY addresses.

4.3.1.9 RX PCM Information

Write to the **RX PCM Link Control Register** for the PCM Mode, clock and SYNC signal polarity and to enable the RX PCM circuitry. Select the clock and SYNC polarity before enabling the RX PCM link.

| Step | Register (s) | Example |
|------|------|---------|
| Reset Utopia RX (output) | **UTOPIA_OUTPUT_ADDR_ENABLE_1** | |
| Disable Links in IMA Mode | **UTOPIA_L2_OUTPUT_ADDR_0** | |
| Define Utopia Output Group PHY addresses | **UTOPIA_L2_OUTPUT_ADDR_1** | |
| Configure RX PCM Format | **RX_PCM_LINK_CONTROL_REG** | *configure_rx_pcm();* |
| Configure RX Link Parameters | **RX_LINK_CONTROL_REG** | *configure_rx_link();* |
| Enable RX PCM | **RX_PCM_LINK_CONTROL_REG** | |
| (Enable TX PCM) | **TX_PCM_LINK_CONTROL_REG_1** | |
| Confirm Cell Delineation | **LOAD_VALUES RX_STATE_REG** | *wait_for_cell_delineation();* |

**Table 12 - RX UNI Setup**

4.3.2   Start-up

Once the setup is done, and when the Cell Delineation is in synch state, enable the NE RX Utopia interface by writing to the **Utopia Output Link PHY Enable Register**.

Enable the NE TX side by writing to the **Utopia Input Link PHY Enable Register**.

It is the user's responsibility to implement any required handshaking between the NE and the FE.

Reset the various counters and status registers when the IMA group is declared operational. Enable the various sources of interrupt at this time.

| Step | Register(s) | Example |
|------|------|---------|
| Enable RX Utopia interface | **UTOPIA_OUTPUT_ADDR_ENABLE_1** | |
| Start TX of User Cells | **TX_LINK_CONTROL_REG** | |
| Enable TX Utopia interface | **UTOPIA_INPUT_GROUP_PHY_ENABLE** | |

**Table 13 - UNI Mode Start-up**

4.3.3   Ongoing

4.3.3.1   IRQ Processing

There are many sources of interrupts and each may be enabled individually.

The IRQ status registers are organized on a per link basis. The **IRQ Master Status Register** is read first to find out which link(s) requested services and then the **IRQ Link Status Register** is read to find out the exact source of interrupt.See Section 7.0 for a detailed diagram of the interrupt structure.

4.3.3.2   Calculation of RX User Cells in UNI mode

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With the MT90220, there is no direct method of obtaining the number of User (or Data) cells.
In UNI Mode, the number of User cells can be obtained by the following equation:

$$UserCells = TotalCells - TotalFillerIdleCells - TotalCellsWithHecError$$

Note that the counters start incrementing when the RX PCM port is enabled. Before the Cell Delineation is achieved, the counter for the total number of cells AND the counter for cells with HEC error will be incremented for every 53 bytes received on the RX PCM port. Once the Cell Delineation is achieved, the counter for cells with HEC error will stop incrementing and the counter for Idle/Filler cell will increment if no User cell is received.

As noted for IMA mode, it is not recommended to reset the counters after each read period since there may be time differences between counter resets. The suggested method is to accumulate the counters over a long period of time, reporting the differences over each reporting period.

Alternatively, the correct number of User cells could be obtained from the Utopia ATM Controller.

## 5.0  Mixed Mode

The MT90220/1 is capable of "mixed mode" operation meaning some links may be assigned to an IMA group, and some links may be configured in UNI mode. Use a combination of the aforementioned procedures to configure mixed mode. By default, a link that is not configured as part of an IMA group is configured as UNI mode. Note that some counters and interrupts will not be operational, depending on the configuration.

When implementing mixed mode, it is important not to assign links to both IMA and UNI PHY addresses. The MT90220/1 does not check for this condition. Ensure the Utopia ports for the links assigned to IMA groups are disabled.

The MT90220/1 software provides an example of a mixed mode configuration.

## 6.0  Error Detection and Handling

The following sections provide information on how to determine possible sources of errors with the MT90220/1.

### 6.1  Manufacturing Defects

6.1.1  RX External RAM Connection

Indirect access to the external SRAM using test registers is available providing a means to verify the SRAM interconnection and functionality. Writing to the Test Mode Enable Register (bit 7) will enable the test mode. The SRAM address to be accessed is programmed in three MT90220/1 registers and the data to write or read into another register. A transfer command must be initiated and a status bit indicates when the transfer is complete. These are the **RX External SRAM/Read/Write Address Registers 0 - 2**, the **RX External SRAM Read/Write Data Register** and **the RX External SRAM Control Register**.

### 6.1.2 Utopia Clock

The TX and RX Utopia clocks can be verified for a minimum of activity. This is reported in the **General Status Register**. The limit to declare a missing Utopia clock depends on the System Clock frequency. A Utopia Clock will be declared missing if there is no Utopia clock transition within 128 system clock cycles. Note that in the case where a slow Utopia Clock frequency is used with a typical System Clock frequency (of 25 MHz), there is a possibility that the Utopia Clock is reported missing although it is fully functional.

Additionally, The MT90220/1 reports the current level of the RxClk in bit 7 of the **Utopia Output Group PHY Enable Register**. This bit represents the level of the RxClk input pin at the time the register is read and may differ for every read access to the register.

## 6.2  Operational Errors

### 6.2.1 Utopia TX Errors

The HEC is checked in the TX Utopia block and reported through the bad HEC counter. Problems with the data bus and/or address bus may cause HEC errors.

The ATM Layer will report any major functional or interconnection problems when no handshaking or transfer between the MT90220/1 and ATM Layer takes place. As well, the Far End RX IMA group will observe this, as there will be no incoming traffic.

### 6.2.2 Utopia RX Errors

If the ATM layer is not reading the ATM cells from the MT90220/1 device, the RX Utopia FIFO inside the device will report an overflow condition. The device reports the Overflow conditions in the **RX Utopia Link FIFO Overflow Status Registers** and **RX Utopia Group FIFO Overflow Status Registers**. Optionally, the device can generate an IRQ when an overflow condition is detected (The underflow condition is not a valid detectable condition.). If the recombiner process is enabled when the RX Utopia transfer is suspended or interrupted, the recombiner delay will increase until the transfer is resumed. If the recombiner delay does not increase beyond the amount of delay that can be handled with the external SRAM, the RX process will resume. In this case, the recombiner delay is fixed at the delay value that was reported when the problem is corrected. If the recombiner delay increases beyond the maximum delay that can be handled by the external SRAM, then the recombining process will have to be stopped and the RX IMA group would have to be restarted.

### 6.2.3 RX PCM Errors

An RX SYNC pulse in the wrong position will be detected and reported in the **RX Sync Status Register**.

An RXSYNC signal which dies after at least 1 pulse in the proper position will not be detected as the RX PCM block will operate using an internal PCM channel counter, as long as the level is inactive.

Note: If RXSYNC is clamped to zero, the RX PCM interface continues to run. If RXSYNC is clamped high, the RX PCM interface hangs up.

A missing RXSYNC at initialization will likely produce errors in the Cell Delineation block but will not be easily diagnosed from the software point of view.

A missing RXCLK will cause a problem in the CD block and IMA Frame State machine, as no data will be received. Use the **Clock Activity Register** to verify if there is any activity on any RX Clocks, TX Clocks or REF Clocks.

A missing DSTi input signal will be detected as the Cell Delineation state machine will never go into PRESYNC or SYNC state.

It is assumed that the clock frequency will be within the T1 or E1 clock frequency specification as there is no ability to verify the clock accuracy from the MT90220/1.

The lack of the RXCLK on the RX reference link will cause the RX process to stop. This error will be reported as an LOS from the framer. A possible handling procedure is to switch to another RX reference link and resume operation. All cells that were received are still in memory and can be recovered but all the cells that were received during the time the RXCLK was not operational are lost, as they were not written into external SRAM.

### 6.2.4   TX PCM Errors

A missing TXCLOCK, TXSYNC or DSTo signal will not be detected at the Transmit block. The error will be detected at the Far End when no data or corrupted data is received. As part of the IMA protocol, this will be reported back to the Near End that originated the signal(s).

Verify the TX clock for any activity using the **Clock Activity Register**.

There is no ability to detect if the TX CLOCK and/or TXSYNC connection is correct. Use the NE or FE framers to detect this.

### 6.2.5   Severe Link Failures

The following is a suggested procedure to deal with severe link failures:

When an RX link failure is detected (by an OCD or an OIF interrupt from the MT90220/1 or by interrupts from the framers), the link should be taken out of the recombination process. The RX IMA group should resume its normal operation. If this does not occur (as evidenced by reported link delays), a "decrease delay" command that brings the link recombination delays to their normal range, should be implemented.
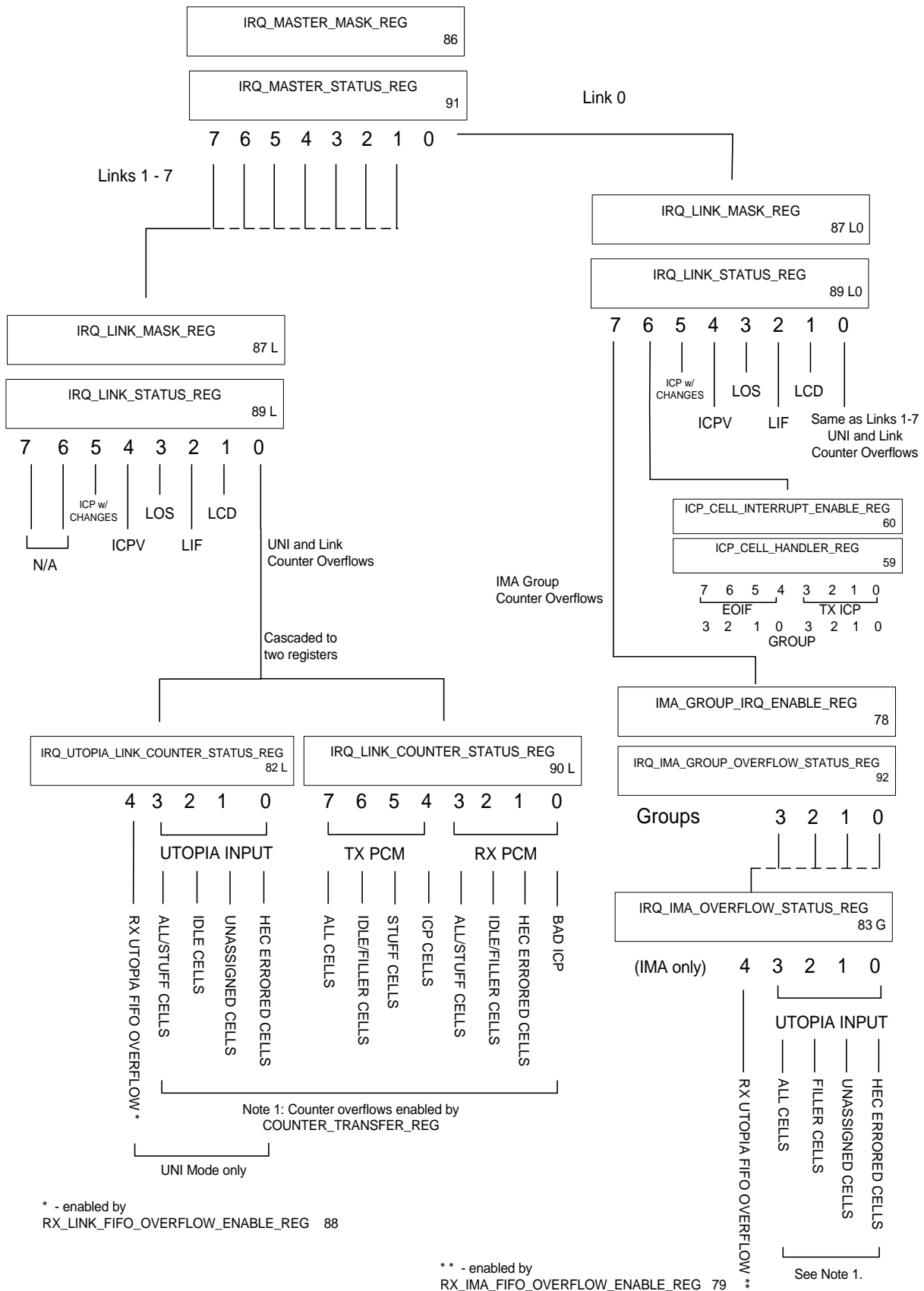
### 6.2.6   RX PCM Counter Behavior

The RX PCM counters are controlled by the RX PCM clock. If an RX PCM clock is present and there is no valid data, the MT90220/1 will "free run" counting multiples of 53 bytes and interpreting each as a cell with a HEC error. The total number of cells *and* HEC errors will continue to increase until the RX PCM port is disabled or the external RX PCM clock is lost.

A suggested workaround is: as a link or a group is started, RX counters should be cleared. The counter information can be considered valid until an RX PCM error condition. If the framer provides a LOS/OOF signal use this event to disable the RX PCM interface until the LOS/OOF condition is cleared. This will maximize the number of HEC errors reported.

Optionally, the counter values may be read and stored at the time of the reported error. Reset the counters when the error condition is cleared.

## 7.0  Interrupt Design

A diagram of the interrupt design of the MT90220/1 is presented in the following table. Registers are denoted by their example code "C" definition name. Numbers associated with each register denote the Register ID from the MT90220/1 example software, and whether they exist on a per-group ("G") or per-link ("L") basis. This diagram is an alternate presentation of information presented in the MT90220/1 datasheet.

IRQ_MASTER_MASK_REG
86

IRQ_MASTER_STATUS_REG
91

Link 0

7 6 5 4 3 2 1 0

Links 1 - 7

IRQ_LINK_MASK_REG
87 L0

IRQ_LINK_STATUS_REG
89 L0

7 6 5 4 3 2 1 0

ICP w/ CHANGES

LOS    LCD

ICPV    LIF

Same as Links 1-7
UNI and Link
Counter Overflows

IRQ_LINK_MASK_REG
87 L

IRQ_LINK_STATUS_REG
89 L

7 6 5 4 3 2 1 0

ICP w/ CHANGES

LOS    LCD

N/A    ICPV    LIF

UNI and Link
Counter Overflows

Cascaded to
two registers

IMA Group
Counter Overflows

ICP_CELL_INTERRUPT_ENABLE_REG
60

ICP_CELL_HANDLER_REG
59

7 6 5 4 3 2 1 0

EOIF    TX ICP
3 2 1 0  3 2 1 0
GROUP

IMA_GROUP_IRQ_ENABLE_REG
78

IRQ_IMA_GROUP_OVERFLOW_STATUS_REG
92

Groups    3 2 1 0

IRQ_UTOPIA_LINK_COUNTER_STATUS_REG
82 L

IRQ_LINK_COUNTER_STATUS_REG
90 L

4 3 2 1 0

7 6 5 4 3 2 1 0

UTOPIA INPUT

TX PCM    RX PCM

IRQ_IMA_OVERFLOW_STATUS_REG
83 G

(IMA only)    4 3 2 1 0

UTOPIA INPUT

RX UTOPIA FIFO OVERFLOW *

ALL/STUFF CELLS

IDLE CELLS

UNASSIGNED CELLS

HEC ERRORED CELLS

ALL CELLS

IDLE/FILLER CELLS

STUFF CELLS

ICP CELLS

ALL/STUFF CELLS

IDLE/FILLER CELLS

HEC ERRORED CELLS

BAD ICP

RX UTOPIA FIFO OVERFLOW **

ALL CELLS

FILLER CELLS

UNASSIGNED CELLS

HEC ERRORED CELLS

Note 1: Counter overflows enabled by
COUNTER_TRANSFER_REG

See Note 1.

UNI Mode only

*  - enabled by
RX_LINK_FIFO_OVERFLOW_ENABLE_REG   88

* *  - enabled by
RX_IMA_FIFO_OVERFLOW_ENABLE_REG   79

# MT90220/1

## 8.0 Changes to this Manual Since Issue 2

**Important Note:** The sequence for programming the MT90220/1 has not changed since Issue 2 of the Programmers Manual.

The following sections were changed since Issue 2:

Table 1 -- added reference to TEST_1_REG and TEST_2_REG ( as in text description ), additional note regarding Utopia Level 1 operation

Section 3.3.12.12 -- added references to RX Link Control Register, Cell Delineation procedure ( as in table description )

Table 7 -- added reference to OAM Label Register (as in text description )

Section 3.3.4.3 -- added section detailing procedure when changing direction of TXCK

Section 3.3.4.12 -- added section detailing calculation of User Cells in IMA mode

Section 3.3.4.13 -- added section detailing RX Group Utopia Fifo Overflow recovery

Section 4.3.1.2, Table 11 -- added programming of TEST_1_REG and TEST_2_REG in UNI mode, additional note regarding Utopia Level 1 operation

Section 4.3.3.2 -- added section detailing calculation of User Cells in UNI mode

Section 7.0 -- added Interrupt Design diagram

Section 8 -- added this section

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