MT90868

High Bandwidth Digital Switch

Data Sheet

December 2009

Features

- 32,768-channel x 8,192-channel blocking switching between backplane and local streams
- 8,192-channel x 8,192-channel non-blocking switching for local input and output streams
- 1,024-channel x 1,024-channel switch between two selected backplane input and output streams
- Rate conversion between backplane and local streams
- Accepts ST-BUS streams with data rate of 16.384 Mb/s or 32.768 Mb/s for backplane port
- Accepts ST-BUS streams with data rate of 8.192 Mb/s for local port
- Per-stream channel and bit delay for the local input streams
- Per-stream channel and bit advancement for the local output streams
- Per-stream bit delay for the backplane input streams
- Per-stream bit advancement for the backplane output streams

Ordering Information

MT90868AG	466 Ball PBGA	Trays
MT90868AG2	466 Ball PBGA*	Trays

*Pb Free Tin/Silver/Copper

-40 to +85° C

- Per-channel constant throughput delay
- Per-channel high impedance output control for local streams
- Per-channel high impedance or driven-high output control for backplane streams
- Per-channel message mode for backplane and local output streams
- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for local and backplane ports
- Non-multiplexed microprocessor interface
- Connection memory block programming for fast device initialization

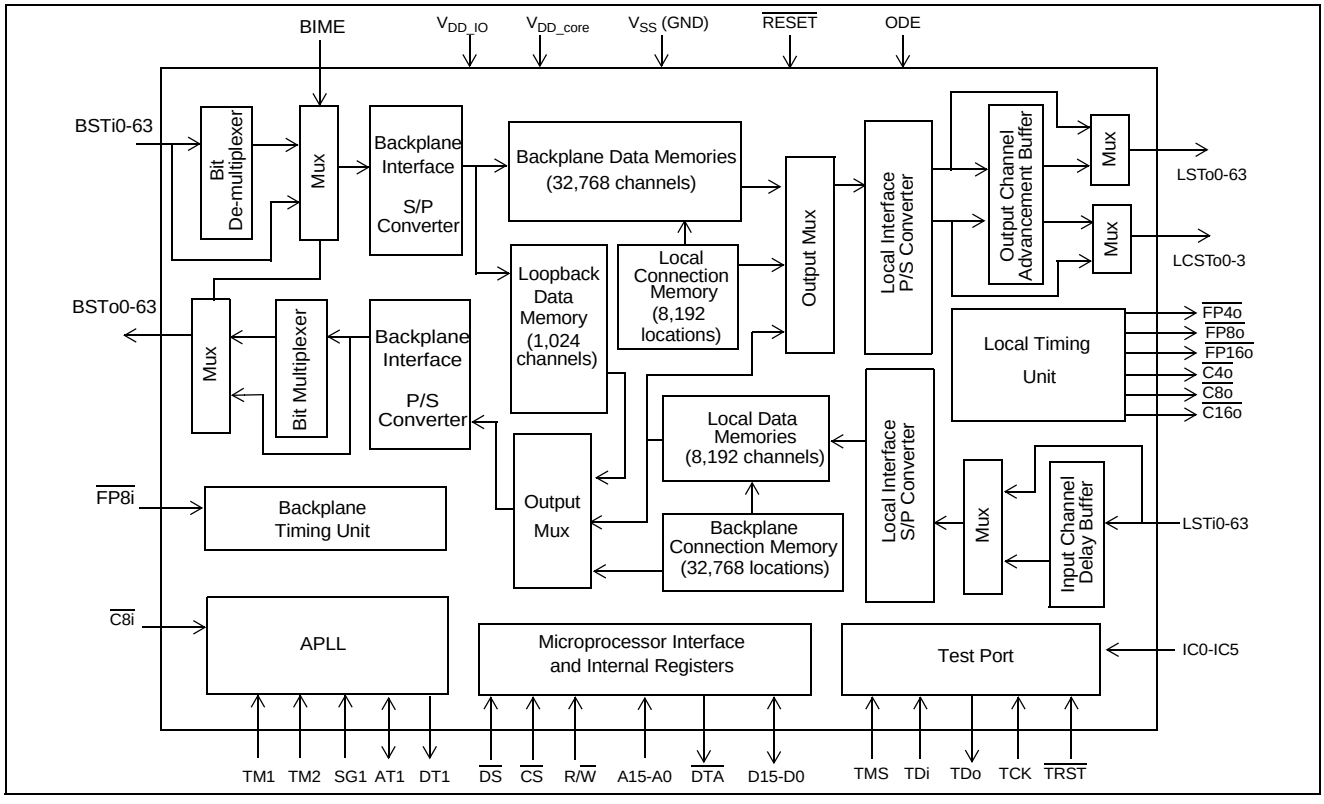

Figure 1 - Functional Block Diagram

- Tristate-control outputs for external drivers on local port
- Conforms to the mandatory requirements of the IEEE-1149.1 (JTAG) standard
- 1.8V core supply voltage
- 3.3V I/O supply voltage with 5V tolerant I/O’s

Applications

- Mediation switches
- High capacity TDM switching platforms utilizing DS-3/OC-3 rates
- Central office switches
- Access equipment

Change Summary

Changes from Decembre 2002 Issue to December 2009 Issue.

Page	Item	Change
1	Ordering Information	Updated ordering information to add PB Free part number.

Description

The MT90868 Digital Switch provides switching capacities of 32,768 x 8,192 channels between backplane and local streams, 8,192 x 8,192 channels among local streams and 1,024 x 1,024 channels among two selected backplane streams. The local port has sixty-four input and sixty-four output streams which operate at 8.192 Mb/s. The backplane port has sixty-four input and sixty-four output streams which operate at 16.384 Mb/s or 32.768 Mb/s.

The MT90868 has features that are programmable on per-stream or per-channel basis including message mode, input bit delay, output bit advancement, constant throughput delay, high impedance output control for both local and backplane streams and the driven-high backplane output control.

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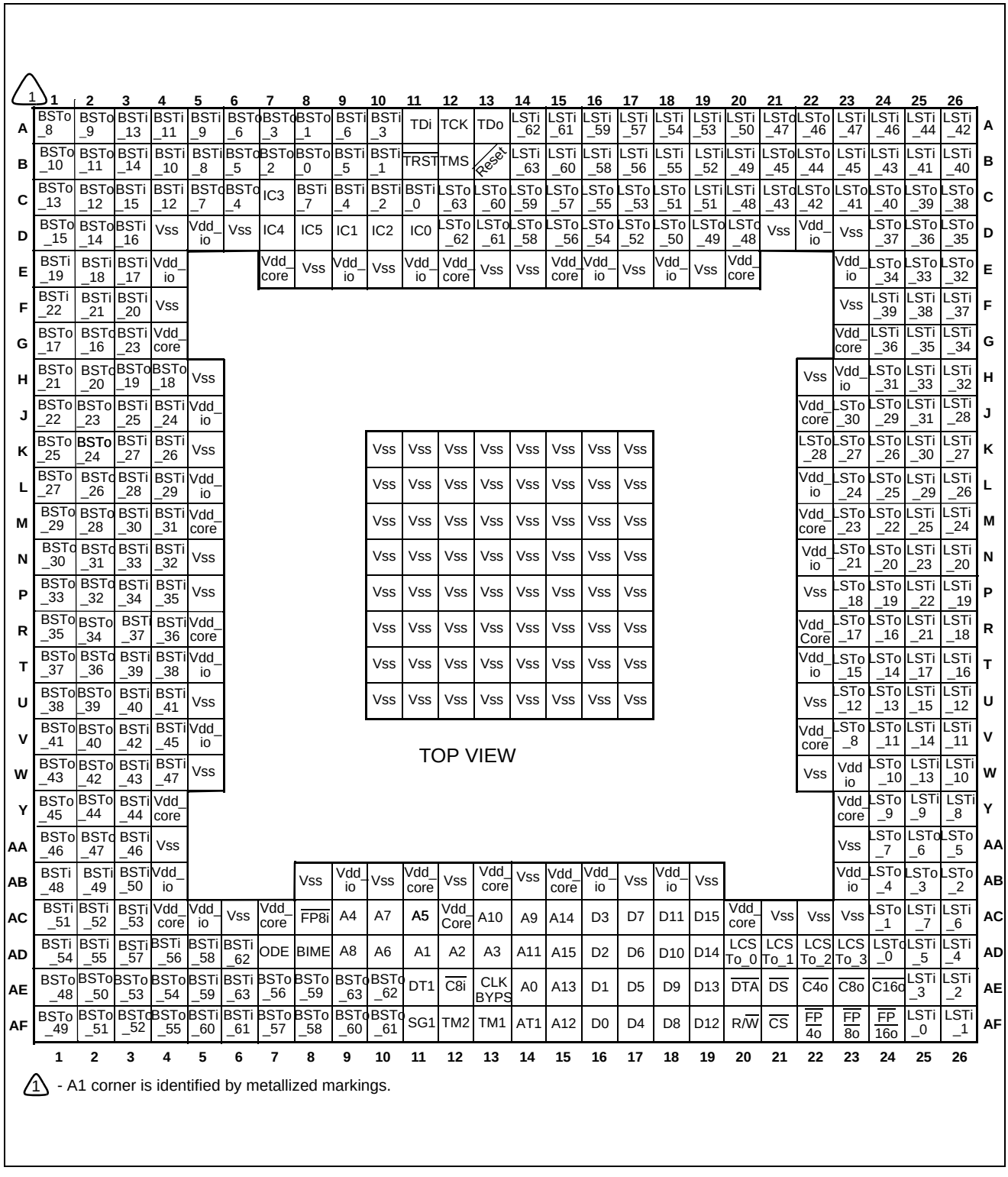


Figure 2 - 35 mm x 35 mm PBGA (JEDEC MO-151) Pinout

Ball Signal Assignment

Ball Number	Signal Name
A1	BSTo8
A2	BSTo9
A3	BSTi13
A4	BSTi11
A5	BSTi9
A6	BSTo6
A7	BSTo3
A8	BSTo1
A9	BSTi6
A10	BSTi3
A11	TDi
A12	TCK
A13	TDo
A14	LSTi62
A15	LSTi61
A16	LSTi59
A17	LSTi57
A18	LSTi54
A19	LSTi53
A20	LSTi50
A21	LSTo47
A22	LSTo46
A23	LSTi47
A24	LSTi46
A25	LSTi44
A26	LSTi42
B1	BSTo10
B2	BSTo11
B3	BSTi14
B4	BSTi10
B5	BSTi8
B6	BSTo5
B7	BSTo2
B8	BSTo0
B9	BSTi5
B10	BSTi1
B11	$\overline{\text{TRST}}$
B12	TMS
B13	$\overline{\text{RESET}}$
B14	LSTi63
B15	LSTi60
B16	LSTi58
B17	LSTi56
B18	LSTi55
B19	LSTi52
B20	LSTi49
B21	LSTo45
B22	LSTo44
B23	LSTi45
B24	LSTi43
B25	LSTi41
B26	LSTi40
C1	BSTo13
C2	BSTo12
C3	BSTi15
C4	BSTi12
C5	BSTo7
C6	BSTo4
C7	IC3
C8	BSTi7
C9	BSTi4
C10	BSTi2
C11	BSTi0
C12	LSTo63
C13	LSTo60
C14	LSTo59
C15	LSTo57
C16	LSTo55
C17	LSTo53
C18	LSTo51
C19	LSTi51
C20	LSTi48
C21	LSTo43
C22	LSTo42
C23	LSTo41
C24	LSTo40
C25	LSTo39
C26	LSTo38
D1	BSTo15
D2	BSTo14
D3	BSTi16
D4	GND
D5	VDD_IO

Ball Number	Signal Name
D6	GND
D7	IC4
D8	IC5
D9	IC1
D10	IC2
D11	IC0
D12	LSTo62
D13	LSTo61
D14	LSTo58
D15	LSTo56
D16	LSTo54
D17	LSTo52
D18	LSTo50
D19	LSTo49
D20	LSTo48
D21	GND
D22	VDD_IO
D23	GND
D24	LSTo37
D25	LSTo36
D26	LSTo35
E1	BSTi19
E2	BSTi18
E3	BSTi17
E4	VDD_IO
E7	VDD_CORE
E8	GND
E9	VDD_IO

Ball Number	Signal Name
E10	GND
E11	VDD_IO
E12	VDD_CORE
E13	GND
E14	GND
E15	VDD_CORE
E16	VDD_IO
E17	GND
E18	VDD_IO
E19	GND
E20	VDD_CORE
E23	VDD_IO
E24	LSTo34
E25	LSTo33
E26	LSTo32
F1	BSTi22
F2	BSTi21
F3	BSTi20
F4	GND
F23	GND
F24	LSTi39
F25	LSTi38
F26	LSTi37
G1	BSTo17
G2	BSTo16
G3	BSTi23
G4	VDD_CORE
G23	VDD_CORE

Ball Number	Signal Name
G24	LSTi36
G25	LSTi35
G26	LSTi34
H1	BSTo21
H2	BSTo20
H3	BSTo19
H4	BSTo18
H5	GND
H22	GND
H23	VDD_IO
H24	LSTo31
H25	LSTi33
H26	LSTi32
J1	BSTo22
J2	BSTo23
J3	BSTi25
J4	BSTi24
J5	VDD_IO
J22	VDD_CORE
J23	LSTo30
J24	LSTo29
J25	LSTi31
J26	LSTi28
K1	BSTo25
K2	BSTo24
K3	BSTi27
K4	BSTi26
K5	GND

Ball Number	Signal Name
K10	GND
K11	GND
K12	GND
K13	GND
K14	GND
K15	GND
K16	GND
K17	GND
K22	LSTo28
K23	LSTo27
K24	LSTo26
K25	LSTi30
K26	LSTi27
L1	BSTo27
L2	BSTo26
L3	BSTi28
L4	BSTi29
L5	VDD_IO
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	GND
L16	GND
L17	GND
L22	VDD_IO
L23	LSTo24

Ball Number	Signal Name
L24	LSTo25
L25	LSTi29
L26	LSTi26
M1	BSTo29
M2	BSTo28
M3	BSTi30
M4	BSTi31
M5	VDD_CORE
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	GND
M16	GND
M17	GND
M22	VDD_CORE
M23	LSTo23
M24	LSTo22
M25	LSTi25
M26	LSTi24
N1	BSTo30
N2	BSTo31
N3	BSTi33
N4	BSTi32
N5	GND
N10	GND
N11	GND

Ball Number	Signal Name
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N22	VDD_IO
N23	LSTo21
N24	LSTo20
N25	LSTi23
N26	LSTi20
P1	BSTo33
P2	BSTo32
P3	BSTi34
P4	BSTi35
P5	GND
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P22	GND
P23	LSTo18
P24	LSTo19
P25	LSTi22

Ball Number	Signal Name
P26	LSTi19
R1	BSTo35
R2	BSTo34
R3	BSTi37
R4	BSTi36
R5	VDD_CORE
R10	GND
R11	GND
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R22	VDD_CORE
R23	LSTo17
R24	LSTo16
R25	LSTi21
R26	LSTi18
T1	BSTo37
T2	BSTo36
T3	BSTi39
T4	BSTi38
T5	VDD_IO
T10	GND
T11	GND
T12	GND
T13	GND

Ball Number	Signal Name
T14	GND
T15	GND
T16	GND
T17	GND
T22	VDD_IO
T23	LSTo15
T24	LSTo14
T25	LSTi17
T26	LSTi16
U1	BSTo38
U2	BSTo39
U3	BSTi40
U4	BSTi41
U5	GND
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U22	GND
U23	LSTo12
U24	LSTo13
U25	LSTi15
U26	LSTi12
V1	BSTo41

Ball Number	Signal Name
V2	BSTo40
V3	BSTi42
V4	BSTi45
V5	VDD_IO
V22	VDD_CORE
V23	LSTo8
V24	LSTo11
V25	LSTi14
V26	LSTi11
W1	BSTo43
W2	BSTo42
W3	BSTi43
W4	BSTi47
W5	GND
W22	GND
W23	VDD_IO
W24	LSTo10
W25	LSTi13
W26	LSTi10
Y1	BSTo45
Y2	BSTo44
Y3	BSTi44
Y4	VDD_CORE
Y23	VDD_CORE
Y24	LSTo9
Y25	LSTi9
Y26	LSTi8
AA1	BSTo46

Ball Number	Signal Name
AA2	BSTo47
AA3	BSTi46
AA4	GND
AA23	GND
AA24	LSTo7
AA25	LSTo6
AA26	LSTo5
AB1	BSTi48
AB2	BSTi49
AB3	BSTi50
AB4	VDD_IO
AB8	GND
AB9	VDD_IO
AB10	GND
AB11	VDD_CORE
AB12	GND
AB13	VDD_CORE
AB14	GND
AB15	VDD_CORE
AB16	VDD_IO
AB17	GND
AB18	VDD_IO
AB19	GND
AB23	VDD_IO
AB24	LSTo4
AB25	LSTo3
AB26	LSTo2
AC1	BSTi51

Ball Number	Signal Name
AC2	BSTi52
AC3	BSTi53
AC4	VDD_CORE
AC5	VDD_IO
AC6	GND
AC7	VDD_CORE
AC8	$\overline{\text{FP8i}}$
AC9	A4
AC10	A7
AC11	A5
AC12	VDD_CORE
AC13	A10
AC14	A9
AC15	A14
AC16	D3
AC17	D7
AC18	D11
AC19	D15
AC20	VDD_CORE
AC21	GND
AC22	GND
AC23	GND
AC24	LSTo1
AC25	LSTi7
AC26	LSTi6
AD1	BSTi54
AD2	BSTi55
AD3	BSTi57

Ball Number	Signal Name
AD4	BSTi56
AD5	BSTi58
AD6	BSTi62
AD7	ODE
AD8	BIME
AD9	A8
AD10	A6
AD11	A1
AD12	A2
AD13	A3
AD14	A11
AD15	A15
AD16	D2
AD17	D6
AD18	D10
AD19	D14
AD20	LCSTo0
AD21	LCSTo1
AD22	LCSTo2
AD23	LCSTo3
AD24	LSTo0
AD25	LSTi5
AD26	LSTi4
AE1	BSTo48
AE2	BSTo50
AE3	BSTo53
AE4	BSTo54
AE5	BSTi59

Ball Number	Signal Name
AE6	BSTi63
AE7	BSTo56
AE8	BSTo59
AE9	BSTo63
AE10	BSTo62
AE11	DT1
AE12	$\overline{\text{C8i}}$
AE13	CLKBYPS
AE14	A0
AE15	A13
AE16	D1
AE17	D5
AE18	D9
AE19	D13
AE20	$\overline{\text{DTA}}$
AE21	$\overline{\text{DS}}$
AE22	$\overline{\text{C4o}}$
AE23	$\overline{\text{C8o}}$
AE24	$\overline{\text{C16o}}$
AE25	LSTi3
AE26	LSTi2
AF1	BSTo49
AF2	BSTo51
AF3	BSTo52
AF4	BSTo55
AF5	BSTi60
AF6	BSTi61
AF7	BSTo57

Ball Number	Signal Name
AF8	BSTo58
AF9	BSTO60
AF10	BSTO61
AF11	SG1
AF12	TM2
AF13	TM1
AF14	AT1
AF15	A12
AF16	D0
AF17	D4
AF18	D8
AF19	D12
AF20	R/$\overline{\text{W}}$
AF21	$\overline{\text{CS}}$
AF22	$\overline{\text{FP4o}}$
AF23	$\overline{\text{FP8o}}$
AF24	$\overline{\text{FP16o}}$
AF25	LSTi0
AF26	LSTi1

Pin Description

PBGA Ball Number	Name	Description
E12, E15, E20, E7, G23, G4, J22, M22, M5, R22, R5, V22, Y23, Y4, AB11, AB13, AB15, AC20, AC4, AC7.	V_{DD_CORE}	**Power Supply for Core Logic Circuits:** +1.8 V
D22, D5, E11, E16, E18, E23, E4, E9, H23, J5, L22, L5, N22, T22, T5, V5, W23, AB16, AB18, AB23, AB4, AB9, AC5.	V_{DD_IO}	**Power Supply for Pads:** +3.3 V. The V_{DD_IO} supply has to be either established before the power up of the V_{DD_CORE} supply or the V_{DD_CORE} should not "lead" the V_{DD_IO} by more than 0.3 V.
M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, N5, P10, P11, P12, P13, P14, P15, P16, P17, P22, P5, R10, R11, R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17, U22, U5, W22, W5.	V_{ss} (GND)	**Ground**
C11, B10, C10, A10, C9, B9, A9, C8, B5, A5, B4, A4, C4, A3, B3, C3, D3, E3, E2, E1, F3, F2, F1, G3, J4, J3, K4, K3, L3, L4, M3, M4, N4, N3, P3, P4, R4, R3, T4, T3, U3, U4, V3, W3, Y3, V4, AA3, W4, AB1, AB2, AB3, AC1, AC2, AC3, AD1, AD2, AD4, AD3, AD5, AE5, AF5, AF6, AD6, AE6.	BSTi0 - 63	**Backplane Serial Input Streams 0 to 63 (5 V Tolerant Inputs):** In 16 Mb/s mode, these pins accept serial TDM data streams at 16.384 Mb/s with 256 channels per stream. In 32 Mb/s mode, these pins accept serial TDM data streams at 32.768 Mb/s with 512 channels per stream.
B8, A8, B7, A7, C6, B6, A6, C5, A1, A2, B1, B2, C2, C1, D2, D1, G2, G1, H4, H3, H2, H1, J1, J2, K2, K1, L2, L1, M2, M1, N1, N2, P2, P1, R2, R1, T2, T1, U1, U2, V2, V1, W2, W1, Y2, Y1, AA1, AA2, AE1, AF1, AE2, AF2, AF3, AE3, AE4, AF4, AE7, AF7, AF8, AE8, AF9, AF10, AE10, AE9.	BSTo0 - 63	**Backplane Serial Output Streams 0 to 63 (5 V Tolerant Three-state Outputs):** In 16 Mb/s mode, these pins have data rate of 16.384 Mb/s with 256 channels per stream. In 32 Mb/s mode, these pins have data rate of 32.768 Mb/s with 512 channels per stream.
AC8	$\overline{FP8i}$	**Frame Pulse Input (5 V Tolerant Input):** This pin accepts the backplane frame pulse which is low for 122 ns (one 8.192 MHz period) at the frame boundary. The frame pulse frequency is 8 kHz.
AE12	$\overline{C8i}$	**Master Clock Input (5 V Tolerant Input):** This pin accepts an 8.192 MHz clock. The clock falling edge is aligned with the backplane frame boundary. This input must be provided for any function to operate.

Pin Description (continued)

PBGA Ball Number	Name	Description
AE13	CLKBYPS	**APLL Bypass clock (5 V Tolerant Input):** This pin accepts a 131.072 MHz clock for device testing purpose. In normal operation, this input MUST be low.
AF13	TM1	**APLL Test Pin 1 (3.3 V Tolerant Input):** Used for APLL testing only. In normal operation, this input MUST be low.
AF12	TM2	**APLL Test Pin 2 (3.3 V Tolerant Input):** Used for APLL testing only. In normal operation, this input MUST be low.
AF11	SG1	**APLL Test Control (3.3 V Tolerant Input):** Used for APLL testing only. In normal operation, this input MUST be low.
AF14	AT1	**Analog Test Access (3.3 V Tolerant I/O):** Used for APLL testing only. This pin is pulled low by an internal pull-down resistor. No connection for normal operation.
AE11	DT1	**Digital Test Access (3.3 V Output):** Used for APLL testing only. No connect for normal operation.
AF21	$\overline{CS}$	**Chip Select (5 V Tolerant Input):** Active low input used by the microprocessor to enable the microprocessor port access.
AE21	$\overline{DS}$	**Data Strobe (5 V Tolerant Input):** This active low input works in conjunction with $\overline{CS}$ to enable the microprocessor port read and write operations.
AF20	R/$\overline{W}$	**Read/Write (5 V Tolerant Input):** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
AE14, AD11, AD12, AD13, AC9, AC11, AD10, AC10, AD9, AC14, AC13, AD14, AF15, AE15, AC15, AD15.	A0 - A15	**Address 0 - 15 (5 V Tolerant Inputs):** These pins form the 16-bit address bus of the microprocessor port.
AF16, AE16, AD16, AC16, AF17, AE17, AD17, AC17, AF18, AE18, AD18, AC18, AF19, AE19, AD19, AC19.	D0 - D15	**Data Bus 0 - 15 (5 V Tolerant I/Os):** These pins form the 16-bit data bus of the microprocessor port.
AE20	$\overline{DTA}$	**Data Transfer Acknowledgment (5 V Tolerant Output):** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required to hold at HIGH level.
B12	TMS	**Test Mode Select (5 V Tolerant Input with internal pull-up):** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.

Pin Description (continued)

PBGA Ball Number	Name	Description
A12	TCK	**Test Clock (5 V Tolerant Input):** Provides the clock to the JTAG test logic.
A11	TDi	**Test Serial Data In (5 V Input with internal pull-up):** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
A13	TDo	**Test Serial Data Out (5 V Tolerant Three-state Output):** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
B11	$\overline{\text{TRST}}$	**Test Reset (5 V Tolerant Input with internal pull-up):** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode.
B13	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input with internal pull-up):** This input (active LOW) puts the device in its reset state that disables the LSTo0 - 63 driver and drives the BSTo0 - 63, LCSTo-3 outputs to high. It also clears the device registers and internal counters. To ensure proper reset action, the reset pin must be held low for longer than 500 ns. A delay of 100 µs must also be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high, this delay is required for the initialization of the APLL.
D11	IC0	In normal operation, this input MUST be connected to ground.
D9	IC1	In normal operation, this input MUST be connected to ground.
D10	IC2	In normal operation, this input MUST be connected to ground.
C7	IC3	In normal operation, this input MUST be connected to ground.
D7	IC4	In normal operation, this input MUST be connected to ground.
D8	IC5	In normal operation, this input MUST be connected to ground.

Pin Description (continued)

PBGA Ball Number	Name	Description
AF25, AF26, AE26, AE25, AD26, AD25, AC26, AC25, Y26, Y25, W26, V26, U26, W25, V25, U25,T26,T25, R26, P26, N26, R25, P25, N25, M26, M25, L26, K26, J26, L25, K25, J25, H26, H25, G26, G25, G24, F26, F25, F24, B26, B25, A26, B24, A25, B23, A24, A23, C20, B20, A20, C19, B19, A19, A18, B18, B17, A17, B16, A16, B15, A15, A14, B14.	LSTi0 - 63	**Local Serial Input Streams 0 to 63 (5 V Tolerant Inputs):** These inputs accept data rates of 8.192 Mb/s with 128 channels per stream.
AD24, AC24, AB26, AB25, AB24, AA26, AA25, AA24, V23, Y24, W24, V24, U23, U24, T24, T23, R24, R23, P23, P24, N24, N23, M24, M23, L23, L24, K24, K23, K22, J24, J23, H24, E26, E25, E24, D26, D25, D24, C26, C25, C24, C23, C22, C21, B22, B21, A22, A21, D20, D19, D18, C18, D17, C17, D16, C16, D15, C15, D14, C14, C13, D13, D12, C12	LSTo0 - 63	**Local Serial Output Streams 0 to 63 (5 V Tolerant Three-state Outputs):** These outputs have data rates of 8.192 Mb/s with 128 channels per stream.
AE24	$\overline{\text{C16o}}$	**Local $\overline{\text{C16o}}$ Clock (3.3 V Three-state Output):** A 16.384MHz clock output. The clock falling edge is aligned with the local frame boundary.
AE23	$\overline{\text{C8o}}$	**Local $\overline{\text{C8o}}$ Clock (3.3 V Three-state Output):** A 8.192 MHz clock output. The clock falling edge is aligned with the local frame boundary.
AE22	$\overline{\text{C4o}}$	**Local $\overline{\text{C4o}}$ Clock (3.3 V Three-state Output):** A 4.096 MHz clock output. The clock falling edge is aligned with the local frame boundary.
AF24	$\overline{\text{FP16o}}$	**Local ST-Bus Frame Pulse Output (3.3 V Three-state Output):** Local port ST-BUS frame pulse output which is low for 61 ns at the frame boundary. Its frequency is 8 KHz.
AF23	$\overline{\text{FP8o}}$	**Local CT-Bus Frame Pulse Output (3.3 V Three-state Output):** Local port ST-BUS frame pulse output which is low for 122 ns at the frame boundary. Its frequency is 8 KHz.
AF22	$\overline{\text{FP4o}}$	**Local ST-Bus Frame Pulse Output (3.3 V Three-state Output):** Local port ST-BUS frame pulse output which is low for 244 ns at the frame boundary. Its frequency is 8 KHz.

Pin Description (continued)

PBGA Ball Number	Name	Description
AD20- AD23	LCSTo0 - 3	**Local Tristate Control Streams 0 to 3 (3.3 V Three-state Outputs):** These pins are used for per-channel external tristate control of the local output streams. The bit rate is 16.384 MHz. When RESET pin or ODE pin is low, the LCSTo0 - 3 are driven high.
AD7	ODE	**Output Drive Enable (5 V Tolerant Input):** This is the asynchronously output enable control for the BSTo0 - 63 and LSTo0 - 63 serial outputs. When it is high, the BSTo0 - 63, LSTo0 - 63 and LCSTo0-3 are enabled. When it is low, the BSTo0 - 63 are tristated or driven high, the LSTo0 - 63 are tristated and the LCSTo0 - 3 are driven high.
AD8	BIME	**Bit Interleaving Mode Enable (5 V Tolerant Input with internal pull down):** When BIME and the BMS bit in the control register are both high, the bit interleaving mode is enabled. See Figure 26 for the bit interleaving mode timing diagram. When it is low, the bit interleaving mode is disabled and the BMS bit in the control register selects the 16 Mb/s or 32 Mb/s mode for the backplane streams.

1.0 Device Overview

The MT90868 can switch up to 32,768 × 8,192 channels while providing a rate conversion capability. It is designed to switch 64 kb/s PCM or N X 64 kb/s data between the backplane and local switching applications. The device maintains frame integrity in data applications and minimum throughput delay for voice application on a per channel basis.

The backplane interface can operate at 16.384 Mb/s or 32.768 Mb/s on ST-BUS and is arranged in 125µs wide frames that contain 256 or 512 channels respectively. A built-in rate conversion circuit allows users to interface between backplane and local interfaces which operates at 8.192 Mb/s.

By using Zarlink's message mode capability, the microprocessor can access input and output time slots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices.

1.1 Functional Description

A Functional Block Diagram of the MT90868 is shown in Figure 1. It is designed to interface ST-BUS serial streams from a backplane source and ST-BUS serial streams from a local source.

1.2 Frame Alignment Timing

In the ST-BUS mode, the C8i pin accepts a 8.192 MHz clock for the frame pulse alignment. The FP8i is a 8 kHz frame pulse signal which goes low at the frame boundary for 122 ns. The frame boundary is defined by the falling edge of the C8i clock during the low cycle of the frame pulse. Figure **3** shows the backplane port timing diagram with the data rate of 16 Mb/s and 32 Mb/s.

The BFP8C bit in the block programming mode register (BPR) allows the device to accept different frame pulse formats. If the BFP8C bit in the block programming register is low, the device accepts a negative frame pulse. If the BFP8C bit is high, the device accepts a positive frame pulse as described in Figure 3.

The device accepts the backplane frame pulse input and generates the local frame pulse outputs. When the 16 Mb/s or 32 Mb/s mode is selected for the backplane port, the delay between the backplane and local frame pulse signals is two 16 Mb/s or 32 Mb/s backplane channels plus 10 cycles of C8i respectively. Figures 4 and 5 show the backplane and local frame pulse alignment for the 16 Mb/s and the 32 Mb/s timing mode respectively.

1.3 Local Interface Output Timing

The local frame pulses, FP4o, FP8o and FP16o are 8 kHz output signals that have a pulse width of 244 ns, 122 ns and 61ns respectively at the frame boundary. The frame boundary is defined by the falling edge of the C8o output clock during the low cycle of the frame pulse FP8o. At the frame boundary, the falling edges of the C4o and C16o output clocks are aligned with the falling edge of the C8o output clock.

In addition, the C8o clock can be inverted by programming the C8C bit to high in the BPR register. When the LFP4C, LFP8C and LFP16C bits are programmed to high in the BPR register, the device will provide positive frame pulse for the FP4o, FP8o and FP16o outputs. The local port timing diagram is shown in Figure 6.

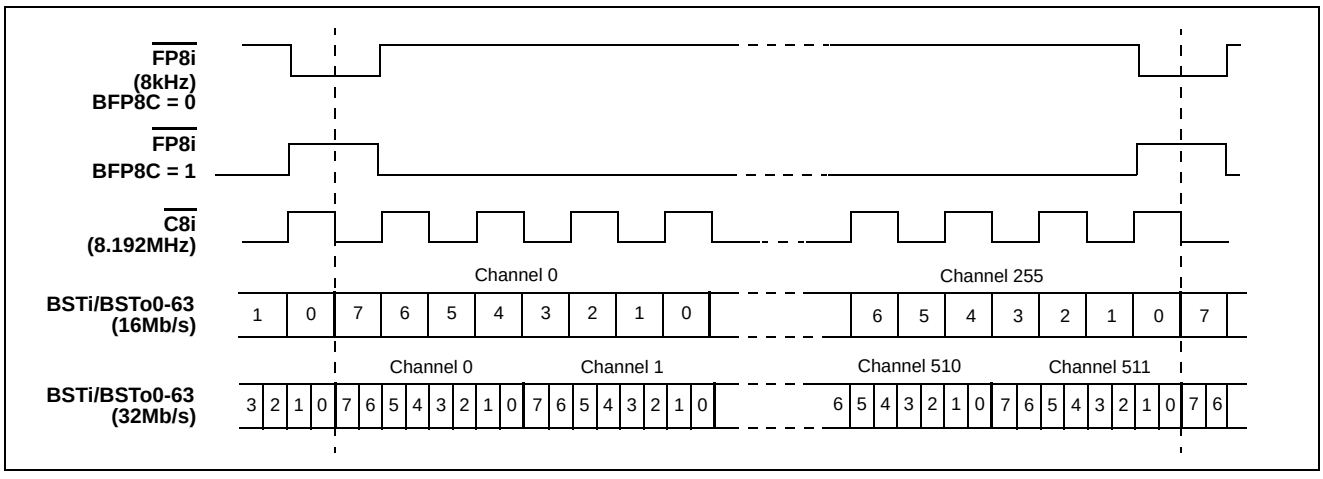


Figure 3 - Backplane Port Timing Diagram for 16 Mb/s and 32 Mb/s modes

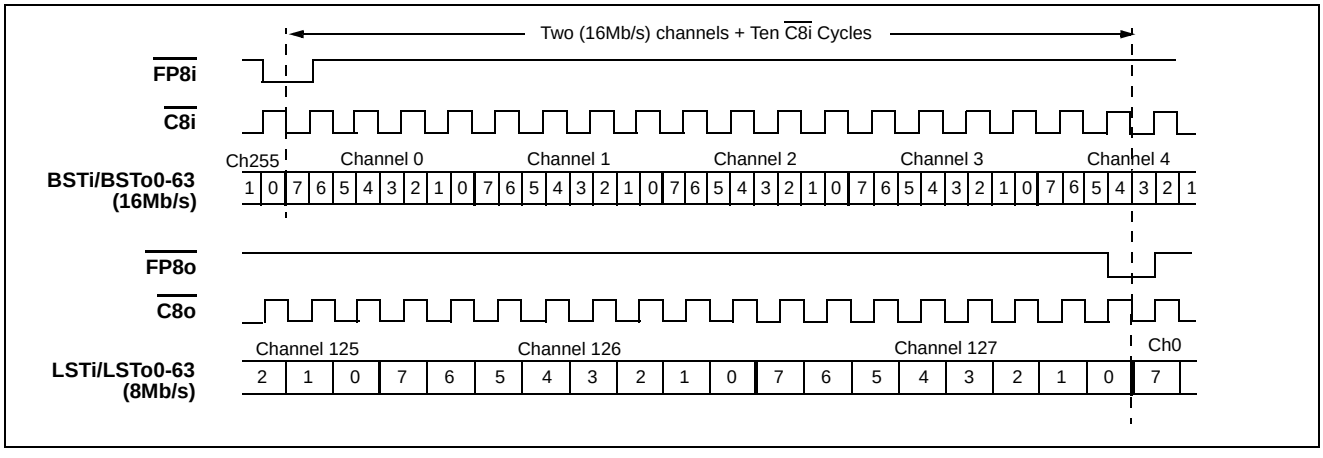


Figure 4 - Backplane and Local Frame Pulse Alignment, Backplane Data Rate is 16 Mb/s

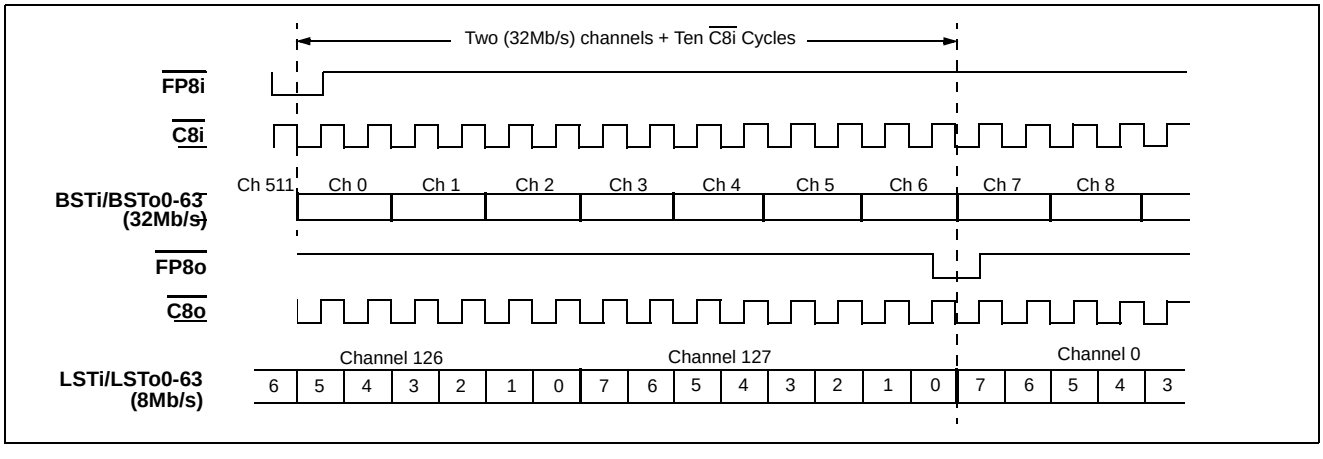


Figure 5 - Backplane and Local Frame Pulse Alignment, Backplane Date Rate is 32 Mb/s

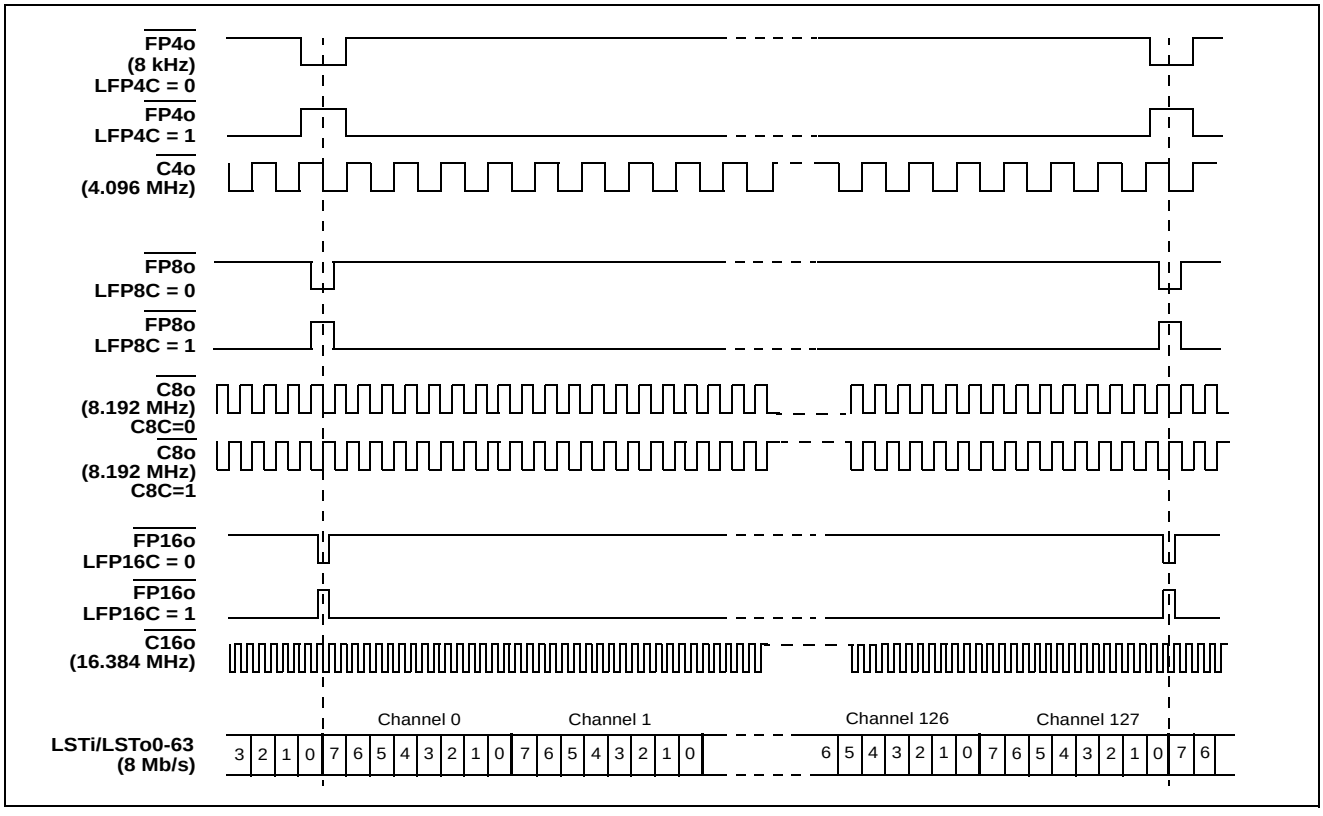


Figure 6 - Local Port Timing Diagram

2.0 Switching Configuration

The MT90868 has two operation modes at different data rates for the backplane interface and one operation mode for the local interface. The two operation modes for the backplane interface can be selected via the backplane mode selection bit (BMS) in the Control Register (CR).

2.1 Backplane Interface

The backplane interface can be programmed to accept data streams of 16 Mb/s or 32 Mb/s. When BMS bit of the CR register is low, the 16 Mb/s mode is enabled, BSTi0-63 and BSTo0-63 have a data rate of 16.384 Mb/s. When BMS = 1, the 32 Mb/s mode is enabled, BSTi0-63 and BSTo0-63 have a data rate of 32.768 Mb/s. Table 1 describes the data rates and mode selections for the backplane interface.

2.2 Local Interface

The local interface has one mode of operation which can only operate at the data rate of 8.192 Mb/s.

2.3 Output Bit Advancement Selection

The device allows users to advance individual backplane or local output streams with respect to the frame boundary. This feature is useful in compensating variable output delays caused by various output loading conditions. Each output stream can have its own advancement value programmed by the output advancement registers. The backplane output advancement registers (BOAR0 to BOAR7) are used to program the backplane output advancement. The local output advancement registers (LOAR0 to LOAR7) are used to program the local output advancement. See Tables 17 and Table 19 for the descriptions of the LOAR and BOAR registers.

Possible adjustment for local is -1/8, -1/4 or -3/8 bit and the resolution is 1/8 bit (or 1/8 of C8o cycle). For backplane, the possible adjustment is -1/4, -1/2 or -3/4 bit when the output data rate is 16.384 Mb/s. When the backplane data rate is 32.768 Mb/s, the possible adjustment is -1/2, -1 or -1 1/2 bit. For both data rates, the resolution is 1/8 of C8i cycle. The advancement is independent of the output data rate. Figures 7, 8 and 9 describe the details of the output advancement programming for the local and the backplane interfaces respectively.

2.4 Input Bit Delay Selection

The MT90868 input bit delay features allow users to have more flexibility when designing the switch matrices at high speed, in which the delay lines are easily created on PCM highways which are connected to the switch matrix cards. Each input data stream can have its own input bit delay value programmed by the input delay registers. The local input delay registers (LIDR0 - LIDR21) are used to program the local input delay. The backplane input delay registers (BIDR0 - BIDR21) are used to program the backplane input delay. See Tables 8, 12 and Tables 14, 15 for the descriptions of the LIDR and BIDR registers.

BMS bit of the Control Register	Modes	Backplane Interface
0	16.384 Mb/s	BSTi0 - 63 and BSTo0 - 63
1	32.768 Mb/s	BSTi0 - 63 and BSTo0 - 63

Table 1 - Mode Selection for Backplane Streams

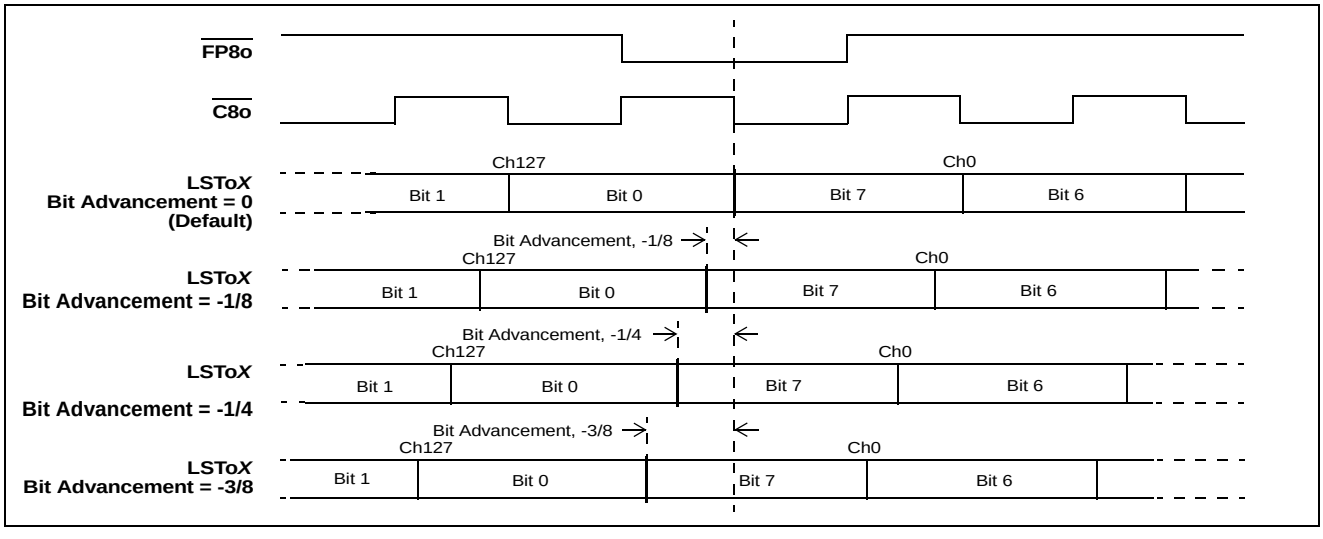


Figure 7 - Local Output Advancement Timing Diagram when the Data Rate is 8 Mb/s

Possible adjustment of the local input data streams, LSTi0 - LSTi63 is up to 7 3/4 bits. The resolution is 1/4 bit or 1/4 C8o cycle. For backplane, the possible adjustment of the input data streams, BSTi0 - BSTi63 is up to 7 3/4 bits with a resolution of 1/4 bit (or 1/8 C8i clock cycle) when the input data rate is 16.384 Mb/s. When the input data rate is 32.768 Mb/s, the possible adjustment is up to 7 1/2 bits with a resolution of 1/2 bit (or 1/8 C8i clock cycle). Figures 10, 11 and 12 describe the details of the input bit delay programming for the local and the backplane interfaces respectively.

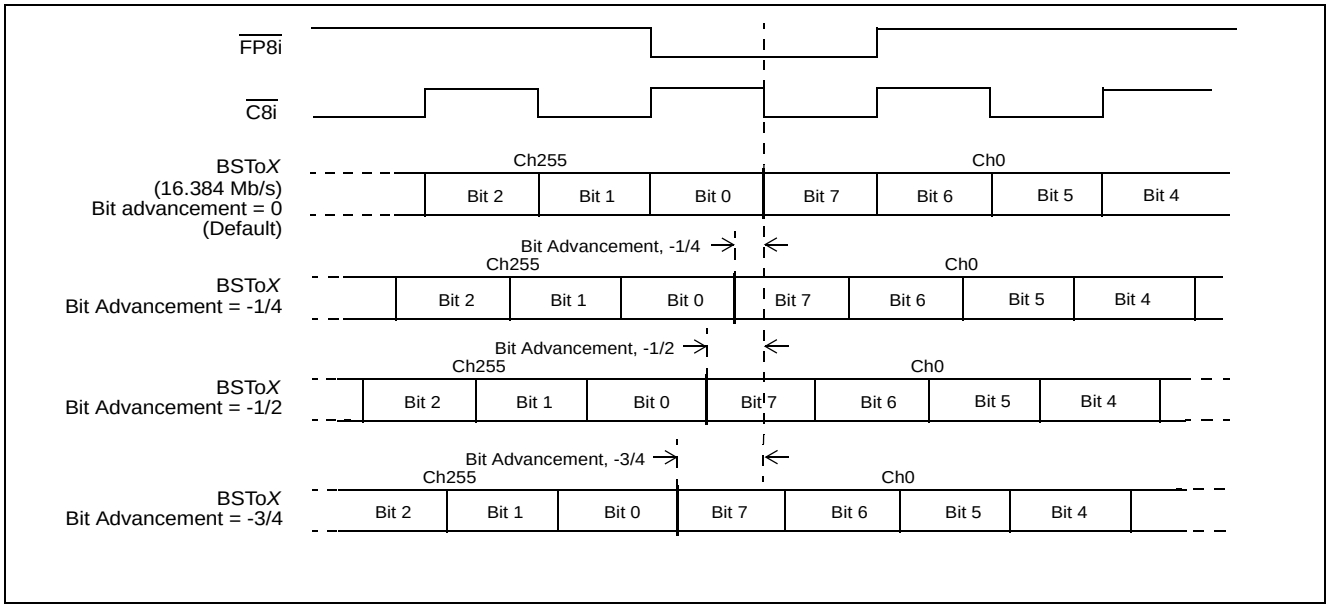


Figure 8 - Backplane Output Advancement Timing Diagram when the Data Rate is 16 Mb/s

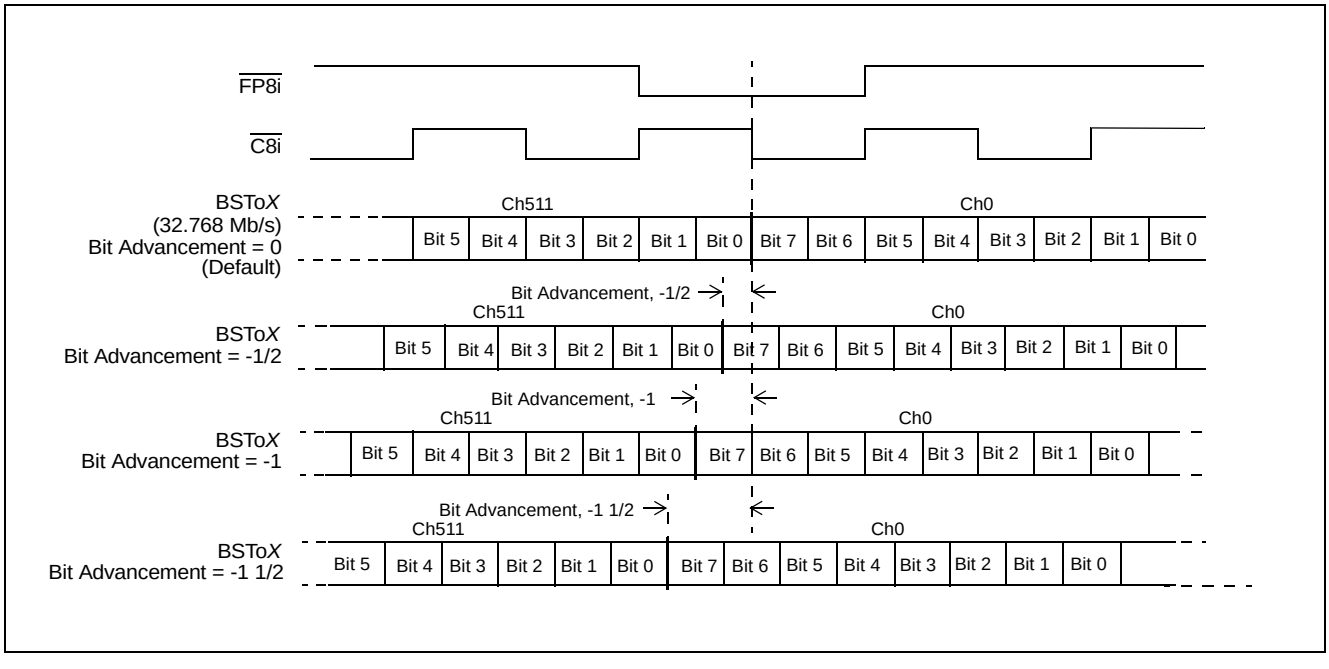


Figure 9 - Backplane Output Advancement Timing Diagram when the Data Rate is 32 Mb/s

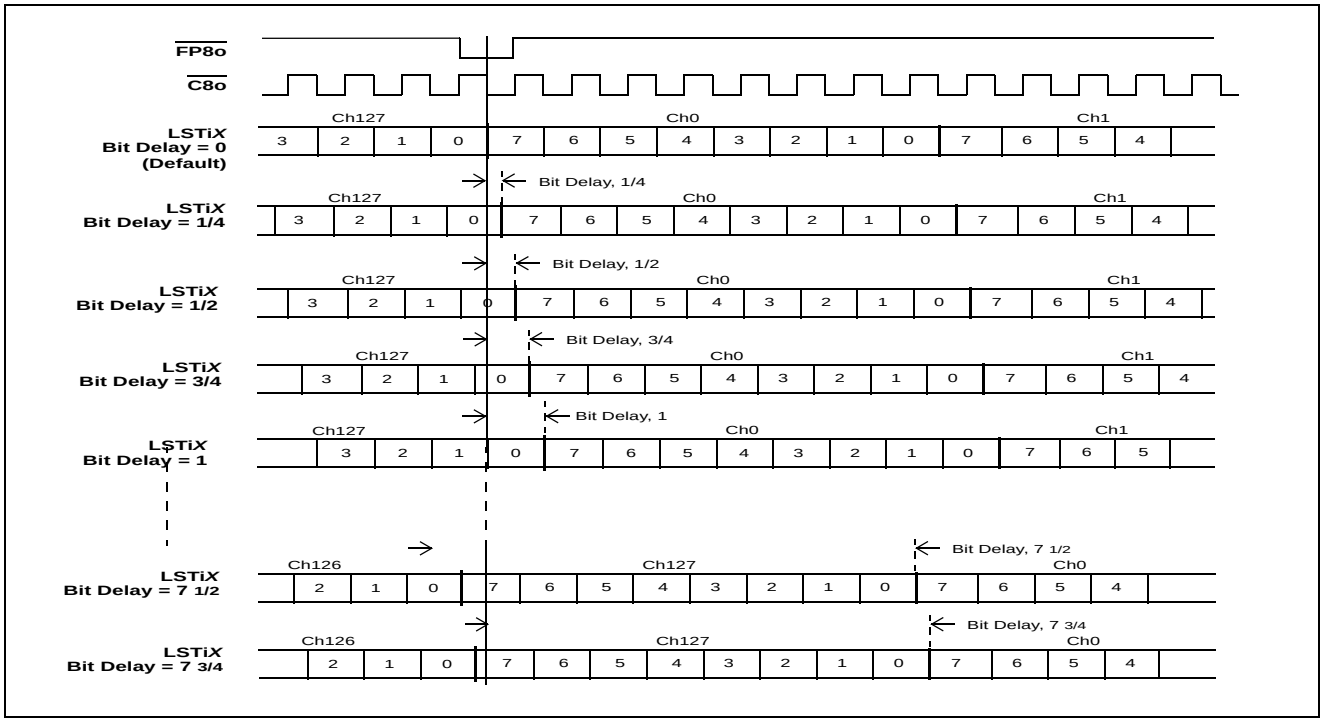


Figure 10 - Local Input Bit Delay Timing Diagram (The Data Rate is 8 Mb/s)

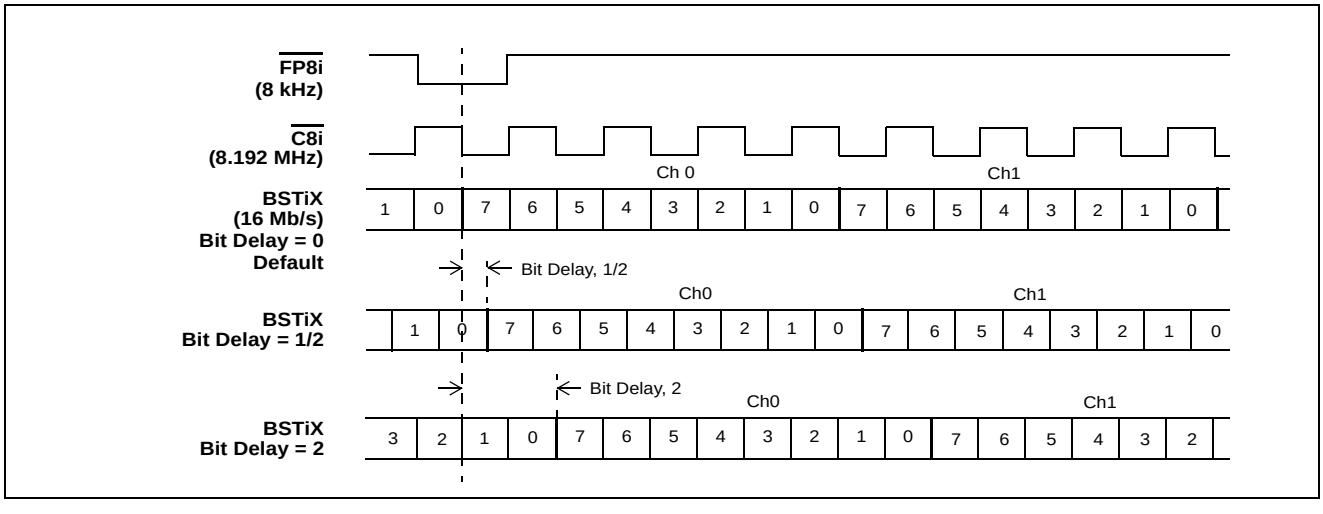


Figure 11 - Backplane Input Bit Delay Timing Diagram when the Data Rate is 16 Mb/s

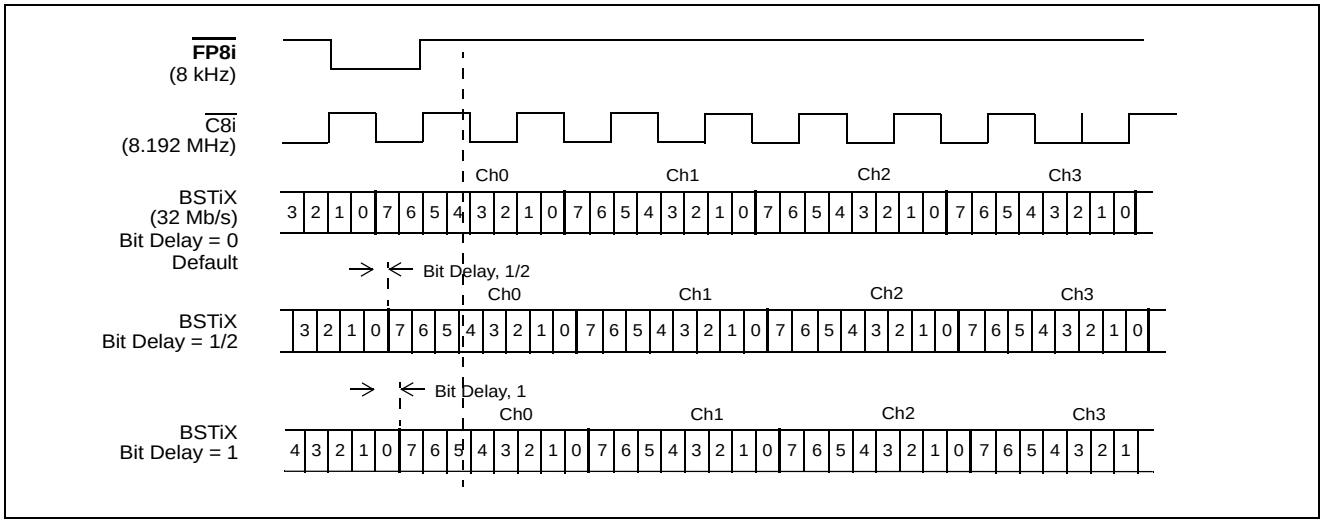


Figure 12 - Backplane Input Bit Delay Timing Diagram when the Data Rate is 32 Mb/s

2.5 Local Input Channel Delay and Local Channel Output Advancement

The MT90868 provides users with the capability of programming the local input channel delay and the local output channel advancement.

The local input channel delay programming allows all local input streams to have a different frame boundary with respect to the local frame pulse ($\overline{F8o}$). It is enabled when the LICDEN bit in the control register (CR) is high. The local input channel delay registers (LICDR0 - LICDR31) allows the users to delay the input channel from 0 to 127 channel for every local input stream. Figure 13 describes the local channel delay timing with different delay values.

The local output channel advancement programming allows all local output streams to have a different frame boundary with respect to the local frame pulse ($\overline{F8o}$). It is enabled when the LOCAEN bit in the CR register is set to high. The local output channel advancement registers (LOCAR0 - LOCAR31) allows the users to advance the output channel from 0 to 127 channels for every local output stream. Figure 14 describes the local channel output advancement timing with different channel advancement values.

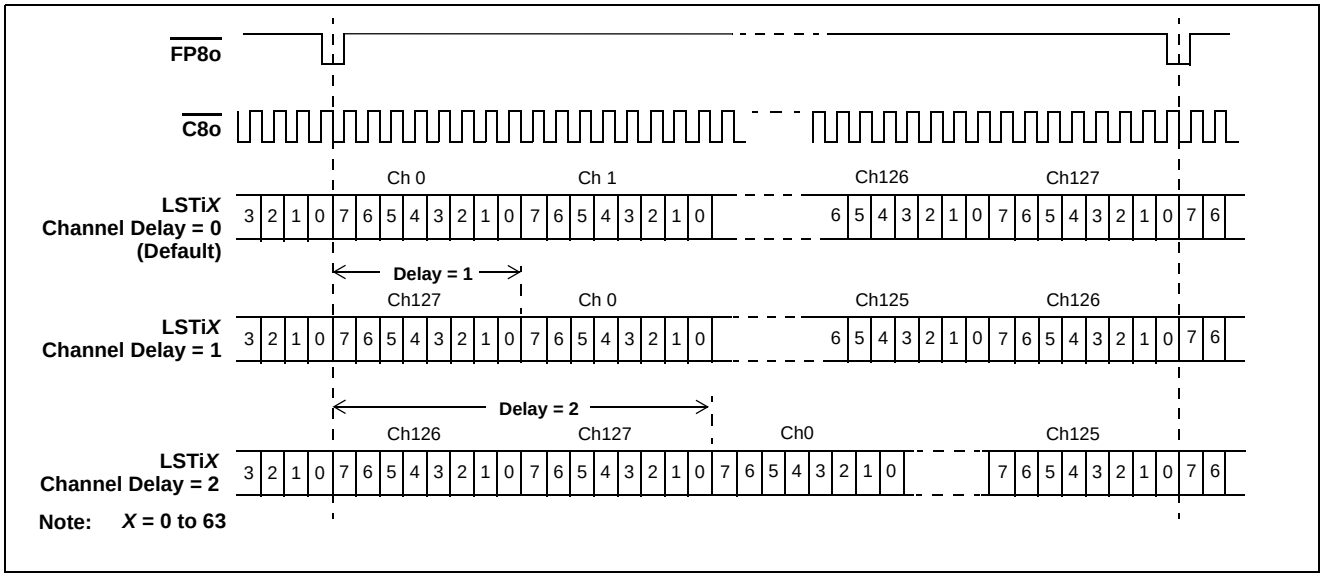


Figure 13 - Local Input Channel Delay Timing Diagram

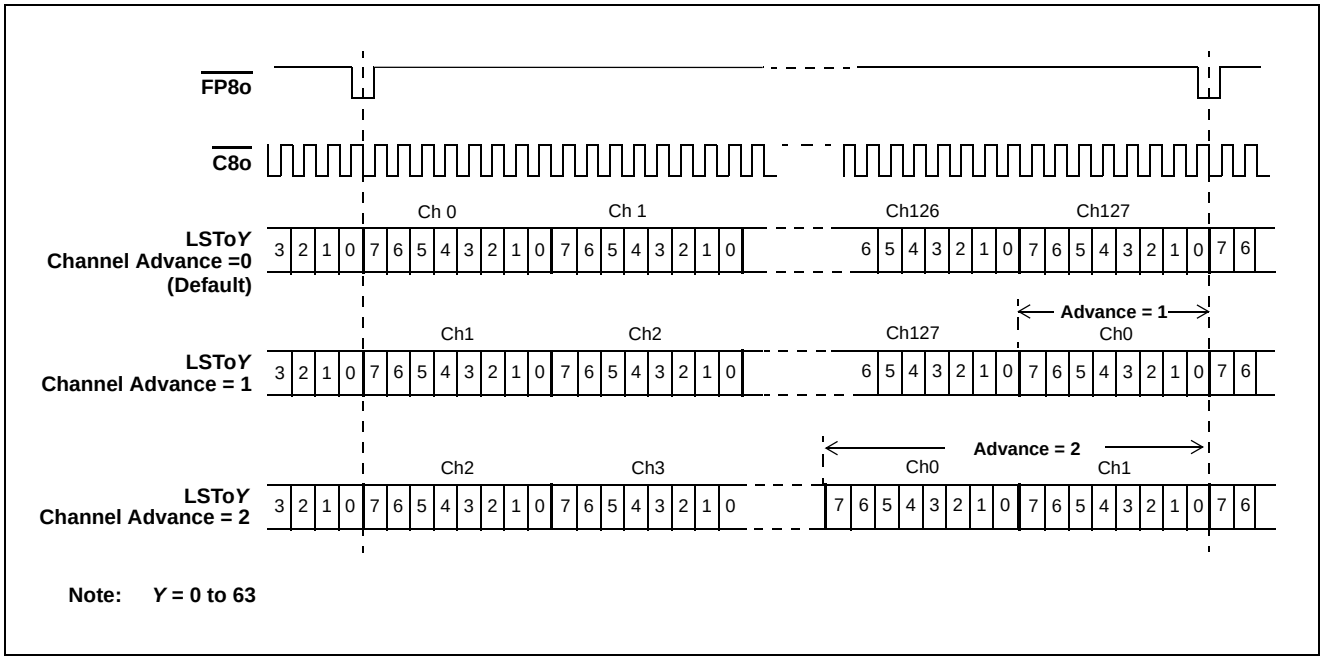


Figure 14 - Local Output Channel Advancement Timing Diagram

2.6 Memory Block Programming

The block programming register (BPR) provides users with the capability of initializing the local and backplane connection memories in two frames. The local connection memory is partitioned into local connection memory high (LCMH) and the local connection memory low (LCML). Bit 13 - bit 15 of every backplane connection memory location will be programmed with the pattern stored in bit 4 - bit 6 of the BPR register. Bit 15 of every LCML location and bit 0 - bit 1 of every LCMH location will be programmed with the pattern stored in bits 1 to 3 of the BPR register. The other bit positions of the backplane connection memory, the local connection memory low and all bits of the local connection memory high are loaded with zeros. See Figure 15 for the connection memory contents when the device is in the block programming mode.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register to high. When the block programming enable (BPE) bit of the BPR register is set to high, the block programming data will be loaded into bits 13 to 15 of every backplane connection memory location and bits 15 of every local connection memory low and bit 0 to bit 1 of every local connection memory high location. The other connection memory bits are loaded with zeros. It takes two frames (250µs) to allow the backplane and local connection memories to be loaded. Upon the completion of the memory block programming, the device resets the BPE bit to low to indicating that the process is finished. See Table 6 for the bit assignment of the BPR register.

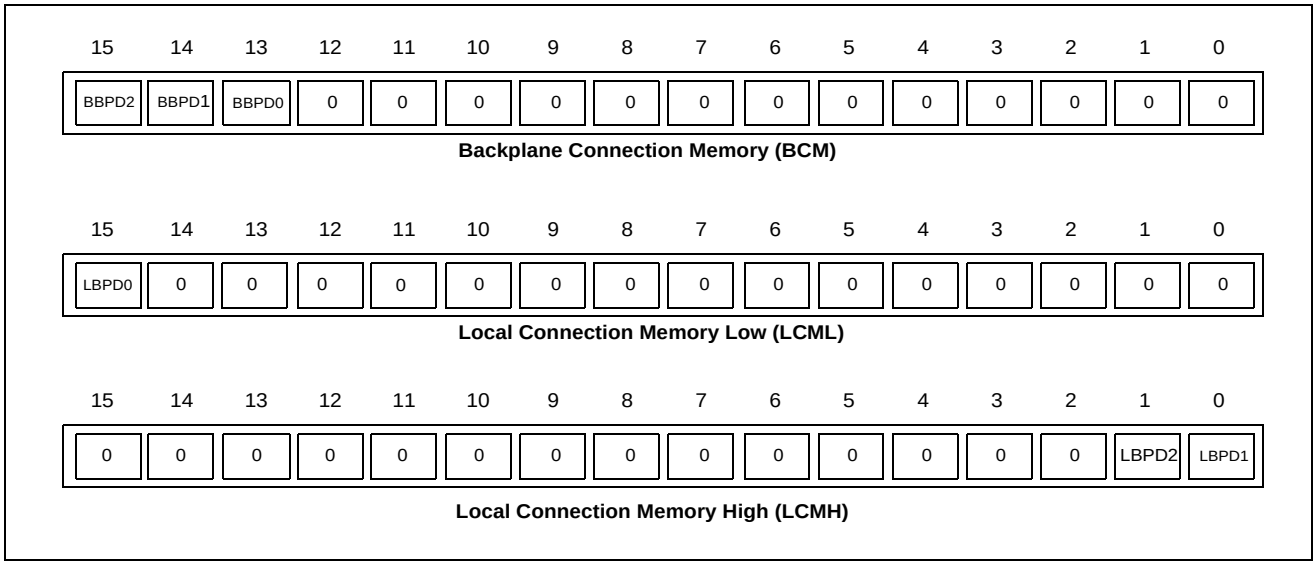


Figure 15 - Block Programming Data in the Connection Memories

3.0 Switching Paths

The MT90868 provides users with four switching paths, namely "backplane-to-local", "local-to-backplane", "backplane-to-backplane" and "local-to-local". The switching configuration is controlled by programming the local connection and the backplane connection memories.

The "backplane-to-local" switching path allows the device to perform data switching between the backplane input port and the local output port among 32,768 backplane input channels and 8,192 local output channels. The local connection memory determines the switching configurations. See Table 30 and Table 31 for the details.

The "local-to-backplane" switching path allows users to perform data switching between the local input port and the backplane output port among 8,192 local input channels and 16,380 or 32,760 backplane output channels when operated in the 16 Mb/s or 32 Mb/s mode respectively. The last channel (Ch255 or Ch511) of the backplane output streams BSTo60 to BSTo63 or BSTo58 to BSTo63 contains invalid output data for the 16 Mb/s or 32 Mb/s mode respectively. Avoid using the last channel of these streams for the "local-to-backplane" data switching. The backplane connection memory determines the switching configurations. See Table 32 for the details.

The "local-to-local" switching path allows users to perform data switching between the local input and the local output ports among 8,192 local input and 8,192 local output ports. The local connection memory determines the switching configurations. See Table 30 and Table 31 for the details.

The "backplane-to-backplane" switching path allows users to perform data switching between the backplane input and the backplane output ports. In this switching mode, only two backplane input streams can be selected by the backplane data input selection register (BDISR). The switching capacity is 512 x 512 or 1,024 x 1,024 backplane channels for the 16 Mb/s or 32 Mb/s mode respectively. The BDISR register selects two backplane input data streams, namely, Stream A and Stream B to support the "backplane-to-backplane" switching. The backplane connection memory determines the switching configurations. See Table 33 for the details.

3.1 Throughput Delay

The usage of the local input channel delay buffer and the local output channel advancement buffer affects the data throughput delay for the four data switching paths. The usage of these two buffers is controlled by the LICDEN and the LOCAEN bits in the control register (CR). When LICDEN and LOCAEN bits are low, the "backplane-to-local" switching path has a throughput delay of one frame plus 2 channel slots; the "local-to-backplane", the "backplane-to-backplane" and the "local-to-local" switching paths have the throughput delay of two frames.

Switching Path	Data Delay			
	Input Buffer** OFF Output Buffer** OFF (LICDEN = 0) (LOCAEN = 0)	Input Buffer **ON** Output Buffer OFF (LICDEN = 1) (LOCAEN = 0)	Input Buffer OFF Output Buffer **ON** (LICDEN = 0) (LOCAEN = 1)	Input Buffer **ON** Output Buffer **ON** (LICDEN = 1) (LOCAEN = 1)
Local-to-Backplane	2 Frames	3 Frames	2 Frames	3 Frames
Local-to-Local	2 Frames	3 Frames	3 Frames	4 Frames
Backplane-to-Local	1 Frame + 2 Ch	1 Frame + 2 Ch	**2 Frames** + 2 Ch	**2 Frames** + 2 Ch
Backplane-to-backplane	2 Frames	2 Frames	2 Frames	2 Frames
** Note: Input Buffer = Local input channel delay buffer Output Buffer = Local output channel advancement buffer.				

Table 2 - Data Delay Through the Device via Different Switching Paths

When the local input data streams pass through the local input channel delay buffer to perform the input channel adjustment by setting the LICDEN bit to high, the device will add one more frame data to the "local-to-backplane" and the "local-to-local" data switching paths. When the local output data streams pass through the local output channel advancement buffer to perform the output channel adjustment by setting the LOCAEN bit to high, the device will add one more frame data delay to the "backplane-to-local" and the "local-to-local" switching paths. Table 2 describes the different delay throughput for the various data switching paths.

4.0 Microprocessor Interface

The MT90868 provides a microprocessor port interface for non-multiplexed bus structures. This interface is compatible to Motorola non-multiplexed bus structure specification. The required microprocessor signals are the 16-bit parallel data bus (D15 - D0), 16-bit address bus (A15 - A0) and four control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 23 for details on the Motorola non-multiplexed bus timing.

The MT90868 synchronous microprocessor port provides access to the internal registers, the connection and the data memories. All memory mapping locations are read/write accessible except the local and backplane bit error rate count registers (LBCR and BBCR) and data memories which can only be read by the users.

4.1 Address Mapping of Registers and Memories

The address bus of the microprocessor port interface selects the internal registers and the memories. If the address bit, A15 is low, then the registers are addressed by A14 to A0 as shown in Table 3.

If A15 is high, the remaining address input lines are used to select the data and connection memory positions corresponding to the serial input or output data streams as shown in Table 4.

A15-A0	Internal Register
0000_H	Control Register, CR
0001_H	Block Programming Register, BPR
0002_H	Local Input Channel Delay Register 0, LICDR0
0003_H	Local Input Channel Delay Register 1, LICDR1
0004_H	Local Input Channel Delay Register 2, LICDR2
0005_H	Local Input Channel Delay Register 3, LICDR3
0006_H	Local Input Channel Delay Register 4, LICDR4
0007_H	Local Input Channel Delay Register 5, LICDR5
0008_H	Local Input Channel Delay Register 6, LICDR6
0009_H	Local Input Channel Delay Register 7, LICDR7
$000A_H$	Local Input Channel Delay Register 8, LICDR8
$000B_H$	Local Input Channel Delay Register 9, LICDR9
$000C_H$	Local Input Channel Delay Register 10, LICDR10
$000D_H$	Local Input Channel Delay Register 11, LICDR11
$000E_H$	Local Input Channel Delay Register 12, LICDR12
$000F_H$	Local Input Channel Delay Register 13, LICDR13
0010_H	Local Input Channel Delay Register 14, LICDR14
0011_H	Local Input Channel Delay Register 15, LICDR15
0012_H	Local Input Channel Delay Register 16, LICDR16
0013_H	Local Input Channel Delay Register 17, LICDR17
0014_H	Local Input Channel Delay Register 18, LICDR18
0015_H	Local Input Channel Delay Register 19, LICDR19
0016_H	Local Input Channel Delay Register 20, LICDR20
0017_H	Local Input Channel Delay Register 21, LICDR21
0018_H	Local Input Channel Delay Register 22, LICDR22

Table 3 - Address Map for Internal Registers, when A15 = 0

A15-A0	Internal Register
0019_H	Local Input Channel Delay Register 23, LICDR23
$001A_H$	Local Input Channel Delay Register 24, LICDR24
$001B_H$	Local Input Channel Delay Register 25, LICDR25
$001C_H$	Local Input Channel Delay Register 26, LICDR26
$001D_H$	Local Input Channel Delay Register 27, LICDR27
$001E_H$	Local Input Channel Delay Register 28, LICDR28
$001F_H$	Local Input Channel Delay Register 29, LICDR29
0020_H	Local Input Channel Delay Register 30, LICDR30
0021_H	Local Input Channel Delay Register 31, LICDR31
0022_H	Local Output Channel Advancement Register 0, LOCAR0
0023_H	Local Output Channel Advancement Register 1, LOCAR1
0024_H	Local Output Channel Advancement Register 2, LOCAR2
0025_H	Local Output Channel Advancement Register 3, LOCAR3
0026_H	Local Output Channel Advancement Register 4, LOCAR4
0027_H	Local Output Channel Advancement Register 5, LOCAR5
0028_H	Local Output Channel Advancement Register 6, LOCAR6
0029_H	Local Output Channel Advancement Register 7, LOCAR7
$002A_H$	Local Output Channel Advancement Register 8, LOCAR8
$002B_H$	Local Output Channel Advancement Register 9, LOCAR9
$002C_H$	Local Output Channel Advancement Register 10, LOCAR10
$002D_H$	Local Output Channel Advancement Register 11, LOCAR11
$002E_H$	Local Output Channel Advancement Register 12, LOCAR12
$002F_H$	Local Output Channel Advancement Register 13, LOCAR13
0030_H	Local Output Channel Advancement Register 14, LOCAR14
0031_H	Local Output Channel Advancement Register 15, LOCAR15

Table 3 - Address Map for Internal Registers, when A15 = 0

A15-A0	Internal Register
0032_H	Local Output Channel Advancement Register 16, LOCAR16
0033_H	Local Output Channel Advancement Register 17, LOCAR17
0034_H	Local Output Channel Advancement Register 18, LOCAR18
0035_H	Local Output Channel Advancement Register 19, LOCAR19
0036_H	Local Output Channel Advancement Register 20, LOCAR20
0037_H	Local Output Channel Advancement Register 21, LOCAR21
0038_H	Local Output Channel Advancement Register 22, LOCAR22
0039_H	Local Output Channel Advancement Register 23, LOCAR23
$003A_H$	Local Output Channel Advancement Register 24, LOCAR24
$003B_H$	Local Output Channel Advancement Register 25, LOCAR25
$003C_H$	Local Output Channel Advancement Register 26, LOCAR26
$003D_H$	Local Output Channel Advancement Register 27, LOCAR27
$003E_H$	Local Output Channel Advancement Register 28, LOCAR28
$003F_H$	Local Output Channel Advancement Register 29, LOCAR29
0040_H	Local Output Channel Advancement Register 30, LOCAR30
0041_H	Local Output Channel Advancement Register 31, LOCAR31
0042_H	Local Input Bit Delay Register 0, LIDR0
0043_H	Local Input Bit Delay Register 1, LIDR1
0044_H	Local Input Bit Delay Register 2, LIDR2
0045_H	Local Input Bit Delay Register 3, LIDR3
0046_H	Local Input Bit Delay Register 4, LIDR4
0047_H	Local Input Bit Delay Register 5, LIDR5
0048_H	Local Input Bit Delay Register 6, LIDR6
0049_H	Local Input Bit Delay Register 7, LIDR7
$004A_H$	Local Input Bit Delay Register 8, LIDR8

Table 3 - Address Map for Internal Registers, when A15 = 0

A15-A0	Internal Register
$004B_H$	Local Input Bit Delay Register 9, LIDR9
$004C_H$	Local Input Bit Delay Register 10, LIDR10
$004D_H$	Local Input Bit Delay Register 11, LIDR11
$004E_H$	Local Input Bit Delay Register 12, LIDR12
$004F_H$	Local Input Bit Delay Register 13, LIDR13
0050_H	Local Input Bit Delay Register 14, LIDR14
0051_H	Local Input Bit Delay Register 15, LIDR15
0052_H	Local Input Bit Delay Register 16, LIDR16
0053_H	Local Input Bit Delay Register 17, LIDR17
0054_H	Local Input Bit Delay Register 18, LIDR18
0055_H	Local Input Bit Delay Register 19, LIDR19
0056_H	Local Input Bit Delay Register 20, LIDR20
0057_H	Local Input Bit Delay Register 21, LIDR21
0058_H	Backplane Input Bit Delay Register 0, BIDR0
0059_H	Backplane Input Bit Delay Register 1, BIDR1
$005A_H$	Backplane Input Bit Delay Register 2, BIDR2
$005B_H$	Backplane Input Bit Delay Register 3, BIDR3
$005C_H$	Backplane Input Bit Delay Register 4, BIDR4
$005D_H$	Backplane Input Bit Delay Register 5, BIDR5
$005E_H$	Backplane Input Bit Delay Register 6, BIDR6
$005F_H$	Backplane Input Bit Delay Register 7, BIDR7
0060_H	Backplane Input Bit Delay Register 8, BIDR8
0061_H	Backplane Input Bit Delay Register 9, BIDR9
0062_H	Backplane Input Bit Delay Register 10, BIDR10
0063_H	Backplane Input Bit Delay Register 11, BIDR11

Table 3 - Address Map for Internal Registers, when A15 = 0

A15-A0	Internal Register
0064_H	Backplane Input Bit Delay Register 12, BIDR12
0065_H	Backplane Input Bit Delay Register 13, BIDR13
0066_H	Backplane Input Bit Delay Register 14, BIDR14
0067_H	Backplane Input Bit Delay Register 15, BIDR15
0068_H	Backplane Input Bit Delay Register 16, BIDR16
0069_H	Backplane Input Bit Delay Register 17, BIDR17
$006A_H$	Backplane Input Bit Delay Register 18, BIDR18
$006B_H$	Backplane Input Bit Delay Register 19, BIDR19
$006C_H$	Backplane Input Bit Delay Register 20, BIDR20
$006D_H$	Backplane Input Bit Delay Register 21, BIDR21
$006E_H$	Local Output Advancement Register 0, LOAR0
$006F_H$	Local Output Advancement Register 1, LOAR1
0070_H	Local Output Advancement Register 2, LOAR2
0071_H	Local Output Advancement Register 3, LOAR3
0072_H	Local Output Advancement Register 4, LOAR4
0073_H	Local Output Advancement Register 5, LOAR5
0074_H	Local Output Advancement Register 6, LOAR6
0075_H	Local Output Advancement Register 7, LOAR7
0076_H	Backplane Output Advancement Register 0, BOAR0
0077_H	Backplane Output Advancement Register 1, BOAR1
0078_H	Backplane Output Advancement Register 2, BOAR2
0079_H	Backplane Output Advancement Register 3, BOAR3
$007A_H$	Backplane Output Advancement Register 4, BOAR4
$007B_H$	Backplane Output Advancement Register 5, BOAR5
$007C_H$	Backplane Output Advancement Register 6, BOAR6

Table 3 - Address Map for Internal Registers, when A15 = 0

A15-A0	Internal Register
$007D_H$	Backplane Output Advancement Register 7, BOAR7
$007E_H$	Backplane Data Input Selection Register, BDISR
$007F_H$	Backplane Data Memory Read Selection Register, BDMRSR
0080_H	Local Data Memory Read Selection Register, LDMRSR
0081_H	Local BER Start Receive Register, LBSRR
0082_H	Local BER Length Register, LBLR
0083_H	Local BER Count Register, LBCR
0084_H	Backplane BER Start Receive Register, BBSRR
0085_H	Backplane BER Length Register, BBLR
0086_H	Backplane BER Count Register, BBCR
0087_H	Reserved
$7FFF_H$	Reserved

Table 3 - Address Map for Internal Registers, when A15 = 0

The Control Register (CR) and the Block Programming Register (BPR) control all the major functions of the device. The Control Register (CR) and the Block Programming Register (BPR) should be programmed immediately after system power up to establish the desired switching configuration as explained in the Frame Alignment Timing and the Switching Configurations sections.

The Control Register is used to select Data or Connection Memory for microport operations through the memory select bits. The register also enables the local input channel delay, the output channel advancement, the backplane per-channel output tristate or per-channel driven-high control selection, the memory block programming mode and the BER test.

The Block Programming Register consists of the block programming data bits (LPBD2 - LPBD0, BBPD2 - BBPD0) and the block programming enable bit (BPE). The BPE bit allows users to program the entire backplane and local connection memories. See Memory Block Programming section. The BPR register also controls the local and the backplane frame pulse polarities.

A15 (Note 1)	Stream Address (Stream 0 - 63)							Channel Address (Channel 0 - 511)									
	A14	A13	A12	A11	A10	A9	Stream #	A8	A7	A6	A5	A4	A3	A2	A1	A0	Channel #
1	0	0	0	0	0	0	Stream 0, C or E (Note 5)	0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	0	1	Stream 1, D or F (Note 5)	0	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	0	1	0	Stream 2	0	0	0	0	0	0	0	1	0	Ch 2
1	0	0	0	0	1	1	Stream 3	0	0	0	0	0	0	0	1	1	Ch 3
.							.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	0	Ch 124
.	.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	1	Ch 125
.	.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	0	Ch 126
.	.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	1	Ch 127 (Note 2)
1	0	1	1	1	0	1	Stream 29	0	1	0	0	0	0	0	0	0	Ch 128
1	0	1	1	1	1	0	Stream 30	0	1	0	0	0	0	0	0	1	Ch 129
1	0	1	1	1	1	1	Stream 31	0	1	0	0	0	0	0	1	0	Ch 130
1	1	0	0	0	0	0	Stream 32	0	1	0	0	0	0	0	1	1	Ch 131
1	1	0	0	0	0	1	Stream 33	.	.	.	.	.	.	.	.	.	.
1	1	0	0	0	1	0	Stream 34	.	.	.	.	.	.	.	.	.	.
1	1	0	0	0	1	1	Stream 35	.	.	.	.	.	.	.	.	.	.
1	1	0	0	1	0	0	Stream 36	0	1	1	1	1	1	1	0	0	Ch 252
.	.	.	.	.	.	.	.	0	1	0	1	1	1	1	0	1	Ch 253
.	.	.	.	.	.	.	.	0	1	1	1	1	1	1	1	0	Ch 254
.	.	.	.	.	.	.	.	0	1	1	1	1	1	1	1	1	Ch 255 (Note 3)
.	.	.	.	.	.	.	.	1	0	0	0	0	0	0	0	0	Ch 256
.	.	.	.	.	.	.	.	1	0	0	0	0	0	0	0	1	Ch 257
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	0	Stream 60	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	1	Stream 61	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	Stream 62	1	1	1	1	1	1	1	1	0	Ch 510
1	1	1	1	1	1	1	Stream 63	1	1	1	1	1	1	1	1	1	Ch 511 (Note 4)

Notes:
1. Bit A15 must be high to access the data memory and connection memory positions. (A15 must be low to access registers.)
2. Channels 0 to 127 are used when serial stream is at 8.192Mb/s.
3. Channels 0 to 255 are used when serial stream is at 16.384Mb/s.
4. Channels 0 to 511 are used when serial stream is at 32.768Mb/s.
5. Stream C&D or Stream E&F are selected by the backplane data memory read selection register (BDMRSR) or the local data memory read selection register (LDMRSR) respectively. These streams are selected to support the microprocessor port data memory read operation.

Table 4 - Address Map for Memory Locations, when A15 = 1

4.2 Backplane Connection Memory

The Backplane Connection Memory (BCM) is 16-bit wide. It controls the switching configuration of the backplane interface through the Backplane Source Control (BSRC) bit. When this bit is low, the input source is from the local input port and the "local-to-backplane" switching paths can be configured. When this bit is high, the input source is from the backplane input port and the "backplane-to-backplane" switching paths can be configured. Locations in the backplane connection memory are associated with particular BSTo streams.

The BTM1 - BTM0 bits of each backplane connection memory determine the per-channel tristate (or driven-high) control and the per-channel message and the normal modes.

In the switching mode, the contents of the backplane connection memory stream address bits (BSAB0 - BSAB5) and channel address bits (BCAB0 - BCAB6) define the source information (stream and channel) of the time slot that will be switched to the backplane BSTo streams. During the message mode, only the lower 8 least significant bits of the backplane connection memory will be transferred to the BSTo pins.

4.3 Local Connection Memory

The local connection memory controls the local interface switching configurations through the Local Mode Selection Control (LMSC) bit. When this bit is low, the input source is from the backplane input port and the "backplane-to-local" switching path can be configured. When it is high, the input source is from the local input port and the "local-to-local" switching path can be configured. The local connection memory consists of two parts, namely, the Local Connection memory Low (LCML) and the Local Connection Memory High (LCMH). Each of them is 16-bit wide. Locations in the local connection memory are associated with particular LSTo output streams.

The LTM1 - LTM0 bits of each Local Connection Memory High (LCMH) determine the per-channel message mode, the pre-channel tristate and the normal modes.

In the switching mode, the stream address bits (LSAB0 - LSAB5) and channel address bits (LCAB0 - LCAB8) of the local connection memory low (LCML) define the source information (stream and channel) of the time slot that will be switched to the local LSTo streams. During the message mode, only the lower 8 least significant bits of the Local Connection Memory Low are transferred to the LSTo pins.

4.4 Data Memory Read Operation

All connection memory content can be read from the microprocessor port. However, only limited data memory contents can be read from the micro- processor port at any one time. The backplane data memory has 1,024 locations and the local data memory has 256 locations to support the data memory reads.

The Backplane Data Memory Read Selection register (BDMRSR) selects the two backplane input streams which will be read (or monitored) from the microprocessor port. The selected backplane input streams are labelled as Stream C and Stream D. The Local Data Memory Read Selection register (LDMRSR) selects the two local input streams which will be read (or monitored) from the microprocessor port. The selected backplane input streams are labelled as Stream E and Stream F.

Users need to program the BDMRSR and LDMRSR registers before the proper data memory read operations can occur. See Tables 22 and 23 for the description of the memory read selection registers. Also, see Table 4 for the microprocessor addresses required to access Stream C&D or Stream E&F. Refer to the MS0 - 2 bits in the control registers for the selection of the data memory to be read from the microprocessor port.

4.5 Data Transfer Acknowledge

The $\overline{\text{DTA}}$ pin of the microprocessor is driven low by the internal logic to indicate that a data bus transfer cycle is completed. When the bus cycle is ended, the $\overline{\text{DTA}}$ switches to the high impedance state. An external pull-up is required at this output.

4.6 Local External Tristate Control

The MT90868 allows users the flexibility to perform the per-channel tristate operation for the local interface when external drivers or buffers are used for the LSTo0-64 outputs.

The device provides four output control signals, LCSTo0 - LCSTo3 which have the data rate of 16.384Mb/s with 8,192 control bits per frame. Each control bit position is corresponding to a specific output stream and channel location as defined in the local connection memory. When the LTM0 and LTM1 bits in the LCMH are programmed to

tristate selected local output channels, the corresponding LCSTo control bits will set to high for the selected tristate output channels. For example, if we program channel 0 of the LSTo4 to be tristated, the control bit LSTo4_Ch0 will set to high.

With the local output channel advancement feature disabled, the LCSTo0 output is advanced by nine $\overline{C8o}$ cycles from the frame boundary to send out the control bit for the channel 0 of the LSTo0 stream. Similarly, the LCSTo1, LCSTo2 and LCSTo3 outputs are advanced by nine C8o cycles for the channel 0 of the LSTo1; LSTo2 and LSTo3 output streams respectively. The advancement in the LCSTo streams allows the external drivers or buffers to process the LCSTo control bits accordingly before the actual LSTo data is output from the device.

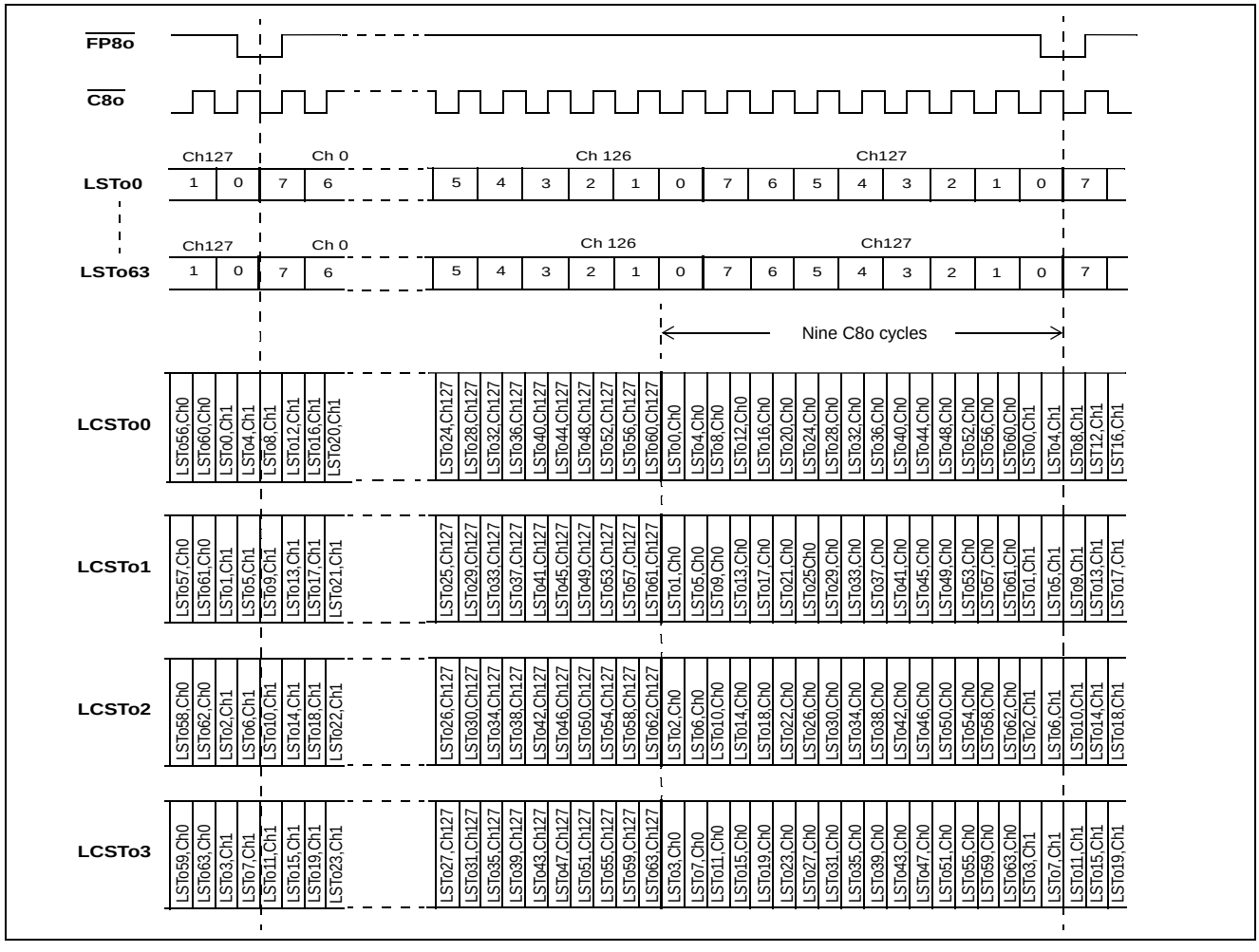


Figure 16 - Local External Tristate Control Timing

When the local output channel advancement feature is enabled, LCSTo signals for those advanced output channels will also be advanced together with the actual channel outputs. Figure 16 describes the Local External Tristate Control Timing.

The ODE and $\overline{RESET}$ pins also control the LCSTo pins. See Table 5, the OSB bit description in the control register.

4.7 Bit Error Rate Test

The MT90868 offers users the Bit Error Rate (BER) test feature for the backplane and local interfaces. The circuitry of the BER test consists of a transmitter and a receiver on both interfaces which can transmit and receive the BER patterns independently. The transmitter can output pseudo random patterns of the form 2^{15} - 1 which can start

anywhere in the frame and last a minimum of one channel and a maximum of one frame time (125 μs). The BER test mode is activated by setting the LTM1 - LTM0 bits to "11" or the BTM1 - BTM0 bits to "11" in the local and the backplane connection memory respectively and also setting the SBERL bit (for local) or the SBERB bit (for backplane) in the Control Register (CR) to high.

For the test, the users can program the BER pattern for multiple consecutive output channels through the connection memory. However, the number of consecutive output channels must be the same as the number of input channels defined in the local and backplane BER length registers (LBLR and BBLR) which define how many BER channels to be monitored by the BER receivers.

There are three types of registers to control the BER transmitter and receiver circuits. The BER Start Receive Registers for the local (LBSRR) and the backplane (BBSRR) define the input stream and channel from where the BER sequence will start to compare. The BER Length Registers for the local (LBLR) and the backplane (BBLR) define the number of input channels which the sequence will be last. The BER Count Registers for the local (LBCR) and the backplane (BBCR) contain the number of counted BER errors after the comparison. To prevent overflow, the internal BER counter will stop updating the error count when the error count reaches 0xFFFF. In additional to the BER registers, the CBERL bit and the CBERB bit of the Control Register are used to clear the backplane and the local bit error count registers; the SBERB and SBERL are used to enable the backplane and the local BER transmitters and receivers. See Table 24, 25, 26, 27, 28 and 29 for the detailed descriptions of the BER registers.

The BER test should be carried out as follows:

- Set the SBERB and the SBERL bits to zero to disable the backplane and the local BER transmitters during the programming of the backplane and local connection memories for the BER test; when the BER transmitters are disabled, the transmitter outputs are set to zero,
- Set the SBERB and SBERL bit from zero to one to enable the BER transmitters and receivers upon the completion of the programming of the connection memories,
- Allow the BER transmitters and receivers to run for at least two frames (or the delay between the serial data output and the serial date input) before the BER receivers can correctly identify errors in the BER pattern but ignore the error counts displayed in the BER count registers during this training period,
- After the training period, clear the BER count registers by setting the CBERL and the CBERB bit of the control register from zero to one,
- Set the CBERL and CBERB bits from one to zero to release the BER counter; the BER receivers receive the BER sequence and perform the comparison,
- Record the bit errors by reading the BER count registers upon the completion of the BER test,
- Clear the BER counters by setting the CBERB and CBERL from zero to one upon the completion of the BER test,

(Note: The transmitter and receiver for both local and backplane interface can be controlled independently to each other.)

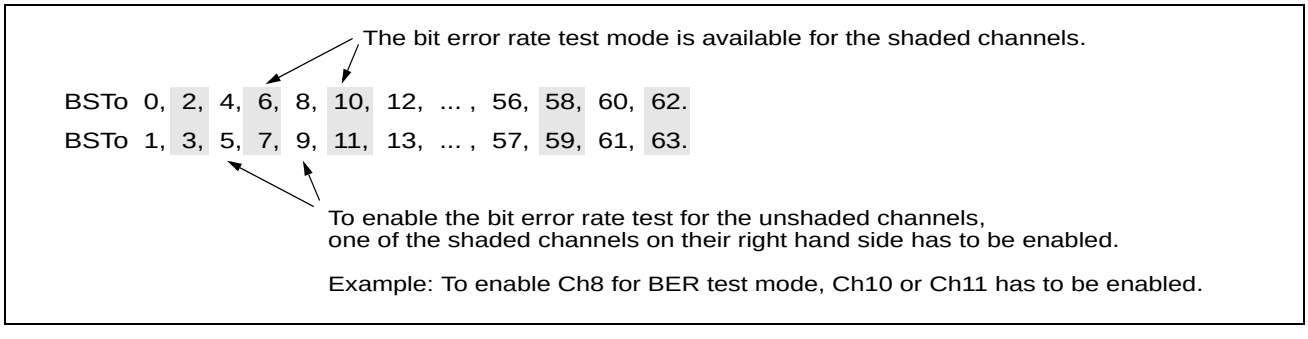


Figure 17 - Backplane Output Streams Availability for BER Test at 32Mb/s mode

When the backplane port is in the 32Mb/s mode, the bit error rate test mode is not available for the backplane output streams *BSTo0, 1, 4, 5, 8, 9, ...* , $4n+0$, $4n+1$ unless the output stream $4n+2$ or $4n+3$ (for $0 \le n \le 15$) is enabled for the BER test mode. Figure 17 explains the details. When the backplane port is in the 16Mb/s mode, all backplane output streams are available.

4.8 Device Initialization

The $\overline{\text{RESET}}$ pin is a synchronous system reset signal that puts the MT90868 into its reset state. When $\overline{\text{RESET}}$ goes low, it disables the LSTo0-63 and LCSTo0-3 outputs and drives the BSTo0-63 outputs to high. It also clears the internal device registers and the internal counters. See Figure 25 for the reset timing.

Upon powering up, the MT90868 must be initialized according to the following initialization sequences:

- Set the ODE pin to low to tristate the LSTo0- 63, LCSTo0-3 and BSTo0-63 outputs.
- Set the $\overline{\text{TRST}}$ pin to low to disable the internal JTAG TAP controller,
- Set $\overline{\text{RESET}}$ pin to low to reset the device, To ensure proper reset action, the reset pin must be held low for longer than 500 ns. A delay of 100 µs must also be applied before the first microprocessor access is performed after the $\overline{\text{RESET}}$ pin is set high, this delay is required for the initialization of the APLL.
- Use the Block Programming mode as described in the Memory Block Programming section to initialize the local and the backplane connection memories,
- Set the ODE pin to high after the connection memories are programmed to release the tristate on LSTo0-63, LCSTo0-3 and BSTo)-63 outputs.
- Set bit 11, STBY, of the Control Register (CR) to high for normal functional mode.

4.9 JTAG Support

The MT90868 JTAG interface conforms to the Boundary-Scan IEEE1149.1 standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller. See Figure 24 for the JTAG test port timing.

4.9.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the MT90868 test functions. It consists of four input pins and one output pin as follows:

- **Test Clock Input (TCK)**
  TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Select Input (TMS)**
  The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Input (TDi)**
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.
- **Test Data Output (TDo)**
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.

- **Test Reset ($\overline{TRST}$)**
  It resets the JTAG scan structure. This pin is internally pulled to Vdd when it is not driven from an external source.

4.9.2 Instruction Register

The MT90868 uses the public instructions defined in the IEEE 1149.1 standard. The JTAG Interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

4.9.3 Test Data Register

As specified in IEEE 1149.1, the MT90868 JTAG Interface contains three test data registers:

- **The Boundary-Scan Register**
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90868 core logic.
- **The Bypass Register**
  The Bypass register is a single stage shift register that provides a one-bit path from TDi to its TDo.
- **The Device Identification Register**
  The JTAG device ID for the MT90868 is 0086814BH.

Version<31:28>: 0000
Part No. <27:12>: 0000 1000 0110 1000
Manufacturer ID<11:1>: 0001 0100 101
LSB<0>: 1

4.9.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Zarlink Semiconductor to support the use of the IEEE 1149 test interface.

Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHIZ	LOCAEN	LICDEN	**0**	STBY	PRST	CBERB	SBERB	CBERL	SBERL	BMS	MBP	OSB	MS2	MS1	MS0

Bit	Name	Description
15	BHIZ	**Backplane Tristate or Driven-High Control:** When this bit is low, the backplane outputs support the per-channel tristate feature. When this bit is high, the backplane outputs support the per-channel driven high feature.
14	LOCAEN	**Local Output Channel Advancement Enable:** When this bit is high, the Local Output Channel Advancement is enabled and the local output data will pass through the local output channel advancement buffer as shown in Figure 1. The local output channel advancement registers (LOCAR31 - LOCAR0) control the channel advancement from 0 to 127 channels. When this bit is low, the channel advancement is disabled (default condition) and the local output data will bypass the local output channel advancement buffer.

Table 5 - Control Register (CR) Bits

Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHIZ	LOCAEN	LICDEN	**0**	STBY	PRST	CBERB	SBERB	CBERL	SBERL	BMS	MBP	OSB	MS2	MS1	MS0

Bit	Name	Description
13	LICDEN	**Local Input Channel Delay Enable:** When this bit is high, the Local Input Channel Advancement is enabled and the local input data will pass through the local input channel delay buffer as shown in Figure 1. The local input channel delay registers (LICDR31 - LICDR0) control the channel delay from 0 to 127 channels. When this bit is low, the channel delay is disabled (default condition) and the local input data will bypass the local input channel delay buffer.
12	Unused	**Reserved.** In normal functional mode, this bit MUST be set to **zero**.
11	STBY	**StandBy:** In normal functional mode, this bit MUST be set to **one** after power up.
10	PRST	**PRBS Reset:** When this bit is high, the output of the BER transmitter will be initialized.
9	CBERB	**Backplane Bit Error Rate Clear:** When this bit is high, it resets the backplane internal bit error counter and the content of the backplane bit error count register (BBCR) to zero. Upon completion of the reset, set this bit to zero.
8	SBERB	**Backplane Bit Error Rate Test Start:** When this bit is high, it enables the backplane BER transmitter and receiver; starts the backplane bit error rate test. The bit error test result is kept in the backplane bit error count (BBCR) register. Upon the completion of the BER test, set this bit to zero.
7	CBERL	**Local Bit Error Rate Clear:** When this bit is high, it resets the local internal bit error counter and the content of the local bit error count register (LBCR) to zero. Upon completion of the reset, set this bit to zero.
6	SBERL	**Local Start Bit Error Rate Test:** When this bit is high, it enables the local BER transmitter and receiver; starts the local bit error rate test. The bit error test result is kept in the local bit error count (LBCR) register. Upon the completion of the BER test, set this bit to zero.
5	BMS	**Backplane Mode Select:** When the BIME pin is low and this bit is low, it enables the 16 Mb/s mode and BSTi0-63 and BSTo0-63 have data rate of 16.384 Mb/s. When the BIME pin is low and this bit is high, it enables the 32 Mb/s mode and BSTi0-63 and BSTo0-63 have data rate of 32.768 Mb/s. When the BIME pin is high, set this bit to high to enable the bit interleaving mode operation.
4	MBP	**Memory Block Programming:** When this bit is high, the connection memory block programming mode is enabled to program Bit 15 of the Local Connection Memory Low, Bit 0 and Bit 1 of the Local Connection Memory High and Bit 13 to Bit 15 of the Backplane Connection Memory. When it is low, the memory block programming mode is disabled. Refer to Figure 15 for details.

Table 5 - Control Register (CR) Bits (continued)

Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BHIZ	LOCAEN	LICDEN	**0**	STBY	PRST	CBERB	SBERB	CBERL	SBERL	BMS	MBP	OSB	MS2	MS1	MS0

Bit	Name	Description
3	OSB	**Output Stand By Bit:** This bit enables the BSTo0 - BSTOo63 and the LSTo0 - LSTo63 serial outputs. The following table describes the HiZ control of the serial data outputs:
2 - 0	MS2 - 0	**Memory Select Bit:** These three bits are used to select different connection and data memories: 000, Local Connection Memory Low (LCML) is selected for read or write operations. 001, Local Connection Memory high (LCMH) is selected for read or write operations. 010, Backplane Connection Memory (BCM) is selected for read or write operations. 011, Local Data Memory is selected for read operation; Streams E and F are selected by the LDMRSR register can be read. 100, Backplane Data Memory is selected for read operation; Streams C and D are selected by the BDMRSR registers can be read.

BIME Pin	$\overline{\text{RESET}}$ Pin	ODE Pin	OSB Bit	BHIZ Bit	LSTo0 to LSTo63	BSTo0 to BSTo63	LCSTo0 to LCSTo3
1	0	X	X	X	HiZ	Driven High	Driven High
1	1	0	X	X	HiZ	Driven High	Driven High
1	1	1	0	X	HiZ	Driven High	Driven High
1	1	1	1	X	Active	Active	Active
0	0	X	X	X	HiZ	HiZ	Driven High
0	1	0	X	0	HiZ	HiZ	Driven High
0	1	0	X	1	HiZ	Driven High	Driven High
0	1	1	0	0	HiZ	HiZ	Driven High
0	1	1	0	1	HiZ	Driven High	Driven High
0	1	1	1	X	Active	Active	Active

Table 5 - Control Register (CR) Bits (continued)

Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LC8C	BFP 8C	LFP 16C	LFP 8C	LFP 4C	BBPD 2	BBPD 1	BBPD 0	LBPD 2	LBPD 1	LBPD 0	BPE

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
11	LC8C	**Local 8M Output ($\overline{C8o}$) Polarity Control:** When this bit is low, the $\overline{C8o}$ falling edge aligns with the frame boundary. When it is high, the C8o rising edge aligns with the frame boundary.
10	BFP8C	**Backplane Frame Pulse ($\overline{FP8i}$) Polarity Control:** When this bit is low, the input frame pulse should have the negative frame pulse format; the frame pulse goes low for 122 ns at the frame boundary. When it is high, the input frame pulse should have the positive frame pulse format; the frame pulse goes high for 122 ns at the frame boundary.
9	LFP16C	**Local Frame Pulse ($\overline{FP16o}$) Polarity Control**: When this bit is low, the output frame pulse has the negative frame pulse format. The frame pulse goes low for 61 ns at the frame boundary. When it is high, the output frame pulse has the positive frame pulse format. The frame pulse goes high for 61 ns at the frame boundary.
8	LFP8C	**Local Frame Pulse ($\overline{FP8o}$) Polarity Control:** When this bit is low, the output frame pulse has the negative frame pulse format. The frame pulse goes low for 122 ns at the frame boundary. When it is high, the output frame pulse has the positive frame pulse format. The frame pulse goes high for 122 ns at the frame boundary.
7	LFP4c	**Local Frame Pulse ($\overline{FP4o}$) Polarity Control:** When this bit is low, the output frame pulse has the negative frame pulse format. The frame pulse goes low for 244 ns at the frame boundary. When it is high, the output frame pulse has the positive frame pulse format. The frame pulse goes high for 244 ns at the frame boundary.
6 - 4	BBPD2 - 0	**Backplane Block Programming Data:** These bits refer to the value to be loaded into the backplane connection memory (BCM) whenever the memory block programming feature is activated. After the MBP bit in the control register is set to high and the BPE bit is set to high, the contents of the bits BBPD2-0 are loaded into Bit 13 to Bit 15 of the BCM. Bit 0-12 of the BCM are zeroed.
3 - 1	LBPD2 - 0	**Local Block Programming Data:** These bits refer to the value to be loaded into the local connection memory, i.e. Local Connection Memory Low (LCML) and Local Connection Memory High (LCMH), whenever the memory block programming feature is activated. After the MBP bit in the control register is set to high and the BPE bit is set to high, the contents of the bits LBPD0 is loaded into Bit 15 of the LCML and the LBPD1 to LBPD2 are loaded into Bit 0 to Bit 1 of the LCMH. Bit 0 to Bit 14 of LCML and Bit 2 to Bit 14 of LCMH are zeroed.

Table 6 - Block Programming Register (BPR) Bits

Bit	Name	Description
0	BPE	**Block Programming Enable.:** A zero to one transition of this bit enables the memory block programming function. The BPE, LBPD2-0 and BBPD2-0 bits in the BPR register must be defined in the same write operation. Once the BPE bit is set to high, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to low indicating the operation is completed. When the BPE is high, the BPE or MBP can be set to low to abort the programming operation. When BPE is high, the other bits in the BPR register must not be changed for two frames to ensure a proper block programming operation. Whenever the microprocessor writes a one to the BPE bit, the block programming function is started, the user must maintain the same logical value to the other bits in the BPR register to avoid any change in the device setting.

Table 6 - Block Programming Register (BPR) Bits (continued)

Read/Write Address: 0002_H - 00011_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LICDR0	0	LICD 16	LICD 15	LICD 14	LICD 13	LICD 12	LICD 11	LICD 10	0	LICD 06	LICD 05	LICD 04	LICD 03	LICD 02	LICD 01	LICD 00
LICDR1	0	LICD 36	LICD 35	LICD 34	LICD 33	LICD 32	LICD 31	LICD 30	0	LICD 26	LICD 25	LICD 24	LICD 23	LICD 22	LICD 21	LICD 20
LICDR2	0	LICD 56	LICD 55	LICD 54	LICD 53	LICD 52	LICD 51	LICD 50	0	LICD 46	LICD 45	LICD 44	LICD 43	LICD 42	LICD 41	LICD 40
LICDR3	0	LICD 76	LICD 75	LICD 74	LICD 73	LICD 72	LICD 71	LICD 70	0	LICD 66	LICD 65	LICD 64	LICD 63	LICD 62	LICD 61	LICD 60
LICDR4	0	LICD 96	LICD 95	LICD 94	LICD 93	LICD 92	LICD 91	LICD 90	0	LICD 86	LICD 85	LICD 84	LICD 83	LICD 82	LICD 81	LICD 80
LICDR5	0	LICD 116	LICD 115	LICD 114	LICD 113	LICD 112	LICD 111	LICD 110	0	LICD 106	LICD 105	LICD 104	LICD 103	LICD 102	LICD 101	LICD 100
LICDR6	0	LICD 136	LICD 135	LICD 134	LICD 133	LICD 132	LICD 131	LICD 130	0	LICD 126	LICD 125	LICD 124	LICD 123	LICD 122	LICD 121	LICD 120
LICDR7	0	LICD 156	LICD 155	LICD 154	LICD 153	LICD 152	LICD 151	LICD 150	0	LICD 146	LICD 145	LICD 144	LICD 143	LICD 142	LICD 141	LICD 140
LICDR8	0	LICD 176	LICD 175	LICD 174	LICD 173	LICD 172	LICD 171	LICD 170	0	LICD 166	LICD 165	LICD 164	LICD 163	LICD 162	LICD 161	LICD 160
LICDR9	0	LICD 196	LICD 195	LICD 194	LICD 193	LICD 192	LICD 191	LICD 190	0	LICD 186	LICD 185	LICD 184	LICD 183	LICD 182	LICD 181	LICD 180
LICDR10	0	LICD 216	LICD 215	LICD 214	LICD 213	LICD 212	LICD 211	LICD 210	0	LICD 206	LICD 205	LICD 204	LICD 203	LICD 202	LICD 201	LICD 200
LICDR11	0	LICD 236	LICD 235	LICD 234	LICD 233	LICD 232	LICD 231	LICD 230	0	LICD 226	LICD 225	LICD 224	LICD 223	LICD 222	LICD 221	LICD 220
LICDR12	0	LICD 256	LICD 255	LICD 254	LICD 253	LICD 252	LICD 251	LICD 250	0	LICD 246	LICD 245	LICD 244	LICD 243	LICD 242	LICD 241	LICD 240
LICDR13	0	LICD 276	LICD 275	LICD 274	LICD 273	LICD 272	LICD 271	LICD 270	0	LICD 266	LICD 265	LICD 264	LICD 263	LICD 262	LICD 261	LICD 260
LICDR14	0	LICD 296	LICD 295	LICD 294	LICD 293	LICD 292	LICD 291	LICD 290	0	LICD 286	LICD 285	LICD 284	LICD 283	LICD 282	LICD 281	LICD 280
LICDR15	0	LICD 316	LICD 315	LICD 314	LICD 313	LICD 312	LICD 311	LICD 310	0	LICD 306	LICD 305	LICD 304	LICD 303	LICD 302	LICD 301	LICD 300

Name	Description
LICDx6 - LICDx0 (See Note 1)	Local Input Channel Delay Bits 6 - 0: The binary value of these seven bits defines the local input channel delay of the local data inputs. The input channel delay can be selected from Ch0 to Ch127 away from the local frame boundary. The local input channel offset delay value is only valid when the LICDEN bit is high in the control register.

Note 1: x denotes a LSTi stream number from 0 to 31.

Table 7 - Local Input Channel Delay Registers (LICDR0 to LICDR15)

Read/Write Address: 0012_H - 00021_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LICDR16	0	LICD 336	LICD 335	LICD 334	LICD 333	LICD 332	LICD 331	LICD 330	0	LICD 326	LICD 325	LICD 324	LICD 323	LICD 322	LICD 321	LICD 320
LICDR17	0	LICD 356	LICD 355	LICD 354	LICD 353	LICD 352	LICD 351	LICD 350	0	LICD 346	LICD 345	LICD 344	LICD 343	LICD 342	LICD 341	LICD 340
LICDR18	0	LICD 376	LICD 375	LICD 374	LICD 373	LICD 372	LICD 371	LICD 370	0	LICD 366	LICD 365	LICD 364	LICD 363	LICD 362	LICD 361	LICD 360
LICDR19	0	LICD 396	LICD 395	LICD 394	LICD 393	LICD 392	LICD 391	LICD 390	0	LICD 386	LICD 385	LICD 384	LICD 383	LICD 382	LICD 381	LICD 380
LICDR20	0	LICD 416	LICD 415	LICD 414	LICD 413	LICD 412	LICD 411	LICD 410	0	LICD 406	LICD 405	LICD 404	LICD 403	LICD 402	LICD 401	LICD 400
LICDR21	0	LICD 436	LICD 435	LICD 434	LICD 433	LICD 432	LICD 431	LICD 430	0	LICD 426	LICD 425	LICD 424	LICD 423	LICD 422	LICD 421	LICD 420
LICDR22	0	LICD 456	LICD 455	LICD 454	LICD 453	LICD 452	LICD 451	LICD 450	0	LICD 446	LICD 445	LICD 444	LICD 443	LICD 442	LICD 441	LICD 440
LICDR23	0	LICD 476	LICD 475	LICD 474	LICD 473	LICD 472	LICD 471	LICD 470	0	LICD 466	LICD 465	LICD 464	LICD 463	LICD 462	LICD 461	LICD 460
LICDR24	0	LICD 496	LICD 495	LICD 494	LICD 493	LICD 492	LICD 491	LICD 490	0	LICD 486	LICD 485	LICD 484	LICD 483	LICD 482	LICD 481	LICD 480
LICDR25	0	LICD 516	LICD 515	LICD 514	LICD 513	LICD 512	LICD 511	LICD 510	0	LICD 506	LICD 505	LICD 504	LICD 503	LICD 502	LICD 501	LICD 500
LICDR26	0	LICD 536	LICD 535	LICD 534	LICD 533	LICD 532	LICD 531	LICD 530	0	LICD 526	LICD 525	LICD 524	LICD 523	LICD 522	LICD 521	LICD 520
LICDR27	0	LICD 556	LICD 555	LICD 554	LICD 553	LICD 552	LICD 551	LICD 550	0	LICD 546	LICD 545	LICD 544	LICD 543	LICD 542	LICD 541	LICD 540
LICDR28	0	LICD 576	LICD 575	LICD 574	LICD 573	LICD 572	LICD 571	LICD 570	0	LICD 566	LICD 565	LICD 564	LICD 563	LICD 562	LICD 561	LICD 560
LICDR29	0	LICD 596	LICD 595	LICD 594	LICD 593	LICD 592	LICD 591	LICD 590	0	LICD 586	LICD 585	LICD 584	LICD 583	LICD 582	LICD 581	LICD 580
LICDR30	0	LICD 616	LICD 615	LICD 614	LICD 613	LICD 612	LICD 611	LICD 610	0	LICD 606	LICD 605	LICD 604	LICD 603	LICD 602	LICD 601	LICD 600
LICDR31	0	LICD 636	LICD 635	LICD 634	LICD 633	LICD 632	LICD 631	LICD 630	0	LICD 626	LICD 625	LICD 624	LICD 623	LICD 622	LICD 621	LICD 620

Name	Description
LICDy6 - LICDy0 (See Note 1)	**Local Input Channel Delay Bits 6 - 0:** The binary value of these seven bits defines the local input channel delay of the local data inputs. The input channel delay can be selected from Ch0 to Ch127 away from the local frame boundary. The local input channel offset delay value is only valid when the LICDEN bit is high in the control register.

Table 8 - Local Input Channel Delay Registers (LICDR16 to LICDR31)

Read/Write Address: 0012_H - 00021_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LICDR16	0	LICD 336	LICD 335	LICD 334	LICD 333	LICD 332	LICD 331	LICD 330	0	LICD 326	LICD 325	LICD 324	LICD 323	LICD 322	LICD 321	LICD 320
LICDR17	0	LICD 356	LICD 355	LICD 354	LICD 353	LICD 352	LICD 351	LICD 350	0	LICD 346	LICD 345	LICD 344	LICD 343	LICD 342	LICD 341	LICD 340
LICDR18	0	LICD 376	LICD 375	LICD 374	LICD 373	LICD 372	LICD 371	LICD 370	0	LICD 366	LICD 365	LICD 364	LICD 363	LICD 362	LICD 361	LICD 360
LICDR19	0	LICD 396	LICD 395	LICD 394	LICD 393	LICD 392	LICD 391	LICD 390	0	LICD 386	LICD 385	LICD 384	LICD 383	LICD 382	LICD 381	LICD 380
LICDR20	0	LICD 416	LICD 415	LICD 414	LICD 413	LICD 412	LICD 411	LICD 410	0	LICD 406	LICD 405	LICD 404	LICD 403	LICD 402	LICD 401	LICD 400
LICDR21	0	LICD 436	LICD 435	LICD 434	LICD 433	LICD 432	LICD 431	LICD 430	0	LICD 426	LICD 425	LICD 424	LICD 423	LICD 422	LICD 421	LICD 420
LICDR22	0	LICD 456	LICD 455	LICD 454	LICD 453	LICD 452	LICD 451	LICD 450	0	LICD 446	LICD 445	LICD 444	LICD 443	LICD 442	LICD 441	LICD 440
LICDR23	0	LICD 476	LICD 475	LICD 474	LICD 473	LICD 472	LICD 471	LICD 470	0	LICD 466	LICD 465	LICD 464	LICD 463	LICD 462	LICD 461	LICD 460
LICDR24	0	LICD 496	LICD 495	LICD 494	LICD 493	LICD 492	LICD 491	LICD 490	0	LICD 486	LICD 485	LICD 484	LICD 483	LICD 482	LICD 481	LICD 480
LICDR25	0	LICD 516	LICD 515	LICD 514	LICD 513	LICD 512	LICD 511	LICD 510	0	LICD 506	LICD 505	LICD 504	LICD 503	LICD 502	LICD 501	LICD 500
LICDR26	0	LICD 536	LICD 535	LICD 534	LICD 533	LICD 532	LICD 531	LICD 530	0	LICD 526	LICD 525	LICD 524	LICD 523	LICD 522	LICD 521	LICD 520
LICDR27	0	LICD 556	LICD 555	LICD 554	LICD 553	LICD 552	LICD 551	LICD 550	0	LICD 546	LICD 545	LICD 544	LICD 543	LICD 542	LICD 541	LICD 540
LICDR28	0	LICD 576	LICD 575	LICD 574	LICD 573	LICD 572	LICD 571	LICD 570	0	LICD 566	LICD 565	LICD 564	LICD 563	LICD 562	LICD 561	LICD 560
LICDR29	0	LICD 596	LICD 595	LICD 594	LICD 593	LICD 592	LICD 591	LICD 590	0	LICD 586	LICD 585	LICD 584	LICD 583	LICD 582	LICD 581	LICD 580
LICDR30	0	LICD 616	LICD 615	LICD 614	LICD 613	LICD 612	LICD 611	LICD 610	0	LICD 606	LICD 605	LICD 604	LICD 603	LICD 602	LICD 601	LICD 600
LICDR31	0	LICD 636	LICD 635	LICD 634	LICD 633	LICD 632	LICD 631	LICD 630	0	LICD 626	LICD 625	LICD 624	LICD 623	LICD 622	LICD 621	LICD 620

Name	Description
Note 1: y denotes a LSTi stream number from 32 to 63.	

Table 8 - Local Input Channel Delay Registers (LICDR16 to LICDR31) (continued)

Read/Write Address: 0022_H - 00031_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAR0	0	LOCA 16	LOCA 15	LOCA 14	LOCA 13	LOCA 12	LOCA 11	LOCA 10	0	LOCA 06	LOCA 05	LOCA 04	LOCA 03	LOCA 02	LOCA 01	LOCA 00
LOCAR1	0	LOCA 36	LOCA 35	LOCA 34	LOCA 33	LOCA 32	LOCA 31	LOCA 30	0	LOCA 26	LOCA 25	LOCA 24	LOCA 23	LOCA 22	LOCA 21	LOCA 20
LOCAR2	0	LOCA 56	LOCA 55	LOCA 54	LOCA 53	LOCA 52	LOCA 51	LOCA 50	0	LOCA 46	LOCA 45	LOCA 44	LOCA 43	LOCA 42	LOCA 41	LOCA 40
LOCAR3	0	LOCA 76	LOCA 75	LOCA 74	LOCA 73	LOCA 72	LOCA 71	LOCA 70	0	LOCA 66	LOCA 65	LOCA 64	LOCA 63	LOCA 62	LOCA 61	LOCA 60
LOCAR4	0	LOCA 96	LOCA 95	LOCA 94	LOCA 93	LOCA 92	LOCA 91	LOCA 90	0	LOCA 86	LOCA 85	LOCA 84	LOCA 83	LOCA 82	LOCA 81	LOCA 80
LOCAR5	0	LOCA 116	LOCA 115	LOCA 114	LOCA 113	LOCA 112	LOCA 111	LOCA 110	0	LOCA 106	LOCA 105	LOCA 104	LOCA 103	LOCA 102	LOCA 101	LOCA 100
LOCAR6	0	LOCA 136	LOCA 135	LOCA 134	LOCA 133	LOCA 132	LOCA 131	LOCA 130	0	LOCA 126	LOCA 125	LOCA 124	LOCA 123	LOCA 122	LOCA 121	LOCA 120
LOCAR7	0	LOCA 156	LOCA 155	LOCA 154	LOCA 153	LOCA 152	LOCA 151	LOCA 150	0	LOCA 146	LOCA 145	LOCA 144	LOCA 143	LOCA 142	LOCA 141	LOCA 140
LOCAR8	0	LOCA 176	LOCA 175	LOCA 174	LOCA 173	LOCA 172	LOCA 171	LOCA 170	0	LOCA 166	LOCA 165	LOCA 164	LOCA 163	LOCA 162	LOCA 161	LOCA 160
LOCAR9	0	LOCA 196	LOCA 195	LOCA 194	LOCA 193	LOCA 192	LOCA 191	LOCA 190	0	LOCA 186	LOCA 185	LOCA 184	LOCA 183	LOCA 182	LOCA 181	LOCA 180
LOCAR10	0	LOCA 216	LOCA 215	LOCA 214	LOCA 213	LOCA 212	LOCA 211	LOCA 210	0	LOCA 206	LOCA 205	LOCA 204	LOCA 203	LOCA 202	LOCA 201	LOCA 200
LOCAR11	0	LOCA 236	LOCA 235	LOCA 234	LOCA 233	LOCA 232	LOCA 231	LOCA 230	0	LOCA 226	LOCA 225	LOCA 224	LOCA 223	LOCA 222	LOCA 221	LOCA 220
LOCAR12	0	LOCA 256	LOCA 255	LOCA 254	LOCA 253	LOCA 252	LOCA 251	LOCA 250	0	LOCA 246	LOCA 245	LOCA 244	LOCA 243	LOCA 242	LOCA 241	LOCA 240
LOCAR13	0	LOCA 276	LOCA 275	LOCA 274	LOCA 273	LOCA 272	LOCA 271	LOCA 270	0	LOCA 266	LOCA 265	LOCA 264	LOCA 263	LOCA 262	LOCA 261	LOCA 260
LOCAR14	0	LOCA 296	LOCA 295	LOCA 294	LOCA 293	LOCA 292	LOCA 291	LOCA 290	0	LOCA 286	LOCA 285	LOCA 284	LOCA 283	LOCA 282	LOCA 281	LOCA 280
LOCAR15	0	LOCA 316	LOCA 315	LOCA 314	LOCA 313	LOCA 312	LOCA 311	LOCA 310	0	LOCA 306	LOCA 305	LOCA 304	LOCA 303	LOCA 302	LOCA 301	LOCA 300

Name	Description
LOCAx6 - LOCAx0 (See Note 1)	**Local Output Channel Advancement Bits 6 - 0:** The binary value of these seven bits defines the local output channel advancement of the local data outputs. The output channel advancement can be selected from Ch0 to Ch127 before the local frame boundary. The local output channel advancement value is only valid when the LOCAEN bit is high in the control register.

Note 1: x denotes a LSTo stream number from 0 to 31.

Table 9 - Local Output Channel Advancement Registers (LOCAR0 to LOCAR16)

Read/Write Address: 0032_H - 00041_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAR16	0	LOCA 336	LOCA 335	LOCA 334	LOCA 333	LOCA 332	LOCA 331	LOCA 330	0	LOCA 326	LOCA 325	LOCA 324	LOCA 323	LOCA 322	LOCA 321	LOCA 320
LOCAR17	0	LOCA 356	LOCA 355	LOCA 354	LOCA 353	LOCA 352	LOCA 351	LOCA 350	0	LOCA 346	LOCA 345	LOCA 344	LOCA 343	LOCA 342	LOCA 341	LOCA 340
LOCAR18	0	LOCA 376	LOCA 375	LOCA 374	LOCA 373	LOCA 372	LOCA 371	LOCA 370	0	LOCA 366	LOCA 365	LOCA 364	LOCA 363	LOCA 362	LOCA 361	LOCA 360
LOCAR19	0	LOCA 396	LOCA 395	LOCA 394	LOCA 393	LOCA 392	LOCA 391	LOCA 390	0	LOCA 386	LOCA 385	LOCA 384	LOCA 383	LOCA 382	LOCA 381	LOCA 380
LOCAR20	0	LOCA 416	LOCA 415	LOCA 414	LOCA 413	LOCA 412	LOCA 411	LOCA 410	0	LOCA 406	LOCA 405	LOCA 404	LOCA 403	LOCA 402	LOCA 401	LOCA 400
LOCAR21	0	LOCA 436	LOCA 435	LOCA 434	LOCA 433	LOCA 432	LOCA 431	LOCA 430	0	LOCA 426	LOCA 425	LOCA 424	LOCA 423	LOCA 422	LOCA 421	LOCA 420
LOCAR22	0	LOCA 456	LOCA 455	LOCA 454	LOCA 453	LOCA 452	LOCA 451	LOCA 450	0	LOCA 446	LOCA 445	LOCA 444	LOCA 443	LOCA 442	LOCA 441	LOCA 440
LOCAR23	0	LOCA 476	LOCA 475	LOCA 474	LOCA 473	LOCA 472	LOCA 471	LOCA 470	0	LOCA 466	LOCA 465	LOCA 464	LOCA 463	LOCA 462	LOCA 461	LOCA 460
LOCAR24	0	LOCA 496	LOCA 495	LOCA 494	LOCA 493	LOCA 492	LOCA 491	LOCA 490	0	LOCA 486	LOCA 485	LOCA 484	LOCA 483	LOCA 482	LOCA 481	LOCA 480
LOCAR25	0	LOCA 516	LOCA 515	LOCA 514	LOCA 513	LOCA 512	LOCA 511	LOCA 510	0	LOCA 506	LOCA 505	LOCA 504	LOCA 503	LOCA 502	LOCA 501	LOCA 500
LOCAR26	0	LOCA 536	LOCA 535	LOCA 534	LOCA 533	LOCA 532	LOCA 531	LOCA 530	0	LOCA 526	LOCA 525	LOCA 524	LOCA 523	LOCA 522	LOCA 521	LOCA 520
LOCAR27	0	LOCA 556	LOCA 555	LOCA 554	LOCA 553	LOCA 552	LOCA 551	LOCA 550	0	LOCA 546	LOCA 545	LOCA 544	LOCA 543	LOCA 542	LOCA 541	LOCA 540
LOCAR28	0	LOCA 576	LOCA 575	LOCA 574	LOCA 573	LOCA 572	LOCA 571	LOCA 570	0	LOCA 566	LOCA 565	LOCA 564	LOCA 563	LOCA 562	LOCA 561	LOCA 560
LOCAR29	0	LOCA 596	LOCA 595	LOCA 594	LOCA 593	LOCA 592	LOCA 591	LOCA 590	0	LOCA 586	LOCA 585	LOCA 584	LOCA 583	LOCA 582	LOCA 581	LOCA 580
LOCAR30	0	LOCA 616	LOCA 615	LOCA 614	LOCA 613	LOCA 612	LOCA 611	LOCA 610	0	LOCA 606	LOCA 605	LOCA 604	LOCA 603	LOCA 602	LOCA 601	LOCA 600
LOCAR31	0	LOCA 636	LOCA 635	LOCA 634	LOCA 633	LOCA 632	LOCA 631	LOCA 630	0	LOCA 626	LOCA 625	LOCA 624	LOCA 623	LOCA 622	LOCA 621	LOCA 620

Name	Description
LOCAy6 - LOCAy0 (See Note 1)	Local Output Channel Advancement Bits 6 - 0: The binary value of these seven bits defines the local output channel advancement of the local data outputs. The output channel advancement can be selected from Ch0 to Ch127 before the local frame boundary. The local output channel advancement value is only valid when the LOCAEN bit is high in the control register.

Note 1: y denotes a LSTo stream number from 32 to 63.

Table 10 - Local Output Channel Advancement Registers (LOCAR15 to LOCAR31)

Read/Write Address: 0042_H - 00051_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIDR0	0	LID 24	LID 23	LID 22	LID 21	LID 20	LID 14	LID 13	LID1 2	LID 11	LID 10	LID 04	LID 03	LID 02	LID 01	LID 00
LIDR1	0	LID 54	LID 53	LID 52	LID 51	LID 50	LID 44	LID 43	LID4 2	LID 41	LID 40	LID 34	LID 33	LID 32	LID 31	LID 30
LIDR2	0	LID 84	LID 83	LID 82	LID 81	LID 80	LID 74	LID 73	LID7 2	LID 71	LID 70	LID 64	LID 63	LID 62	LID 61	LID 60
LIDR3	0	LID 114	LID 113	LID 112	LID 111	LID 110	LID 104	LID 103	LID1 02	LID 101	LID 100	LID 94	LID 93	LID 92	LID 91	LID 90
LIDR4	0	LID 144	LID 143	LID 142	LID 141	LID 140	LID 134	LID 133	LID1 32	LID 131	LID 130	LID 124	LID 123	LID 122	LID 121	LID 120
LIDR5	0	LID 174	LID 173	LID 172	LID 171	LID 170	LID 164	LID 163	LID1 62	LID 161	LID 160	LID 154	LID 153	LID 152	LID 151	LID 150
LIDR6	0	LID 204	LID 203	LID 202	LID 201	LID 200	LID 194	LID 193	LID1 92	LID 191	LID 190	LID 184	LID 183	LID 182	LID 181	LID 180
LIDR7	0	LID 234	LID 233	LID 232	LID 231	LID 230	LID 224	LID 223	LID2 22	LID 221	LID 220	LID 214	LID 213	LID 212	LID 211	LID 210
LIDR8	0	LID 264	LID 263	LID 262	LID 261	LID 260	LID 254	LID 253	LID2 52	LID 251	LID 250	LID 244	LID 243	LID 242	LID 241	LID 240
LIDR9	0	LID 294	LID 293	LID 292	LID 291	LID 290	LID 284	LID 283	LID2 82	LID 281	LID 280	LID 274	LID 273	LID 272	LID 271	LID 270
LIDR10	0	LID 324	LID 323	LID 322	LID 321	LID 320	LID 314	LID 313	LID3 12	LID 311	LID 310	LID 304	LID 303	LID 302	LID 301	LID 300
LIDR11	0	LID 354	LID 353	LID 352	LID 351	LID 350	LID 344	LID 343	LID3 42	LID 341	LID 340	LID 334	LID 333	LID 332	LID 331	LID 330
LIDR12	0	LID 384	LID 383	LID 382	LID 381	LID 380	LID 374	LID 373	LID3 72	LID 371	LID 370	LID 364	LID 363	LID 362	LID 361	LID 360
LIDR13	0	LID 414	LID 413	LID 412	LID 411	LID 410	LID 404	LID 403	LID4 02	LID 401	LID 400	LID 394	LID 393	LID 392	LID 391	LID 390
LIDR14	0	LID 444	LID 443	LID 442	LID 441	LID 440	LID 434	LID 433	LID4 32	LID 431	LID 430	LID 424	LID 423	LID 422	LID 421	LID 420
LIDR15	0	LID 474	LID 473	LID 472	LID 471	LID 470	LID 464	LID 463	LID4 62	LID 461	LID 460	LID 454	LID 453	LID 452	LID 451	LID 450

Name	Description
LIDn4 - LIDn0 (See Note 1)	Local Input Bit Delay Bits 4 - 0: The binary value of these five bits defines the local input bit delay of the LSTi inputs. The local input bit delay can be selected from 0 to 7 3/4 C8o clock periods. See Table 13 for details

Table 11 - Local Input Bit Delay Registers (LIDR0 to LIDR15)

Read/Write Address: 0042_H - 00051_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIDR0	0	LID 24	LID 23	LID 22	LID 21	LID 20	LID 14	LID 13	LID1 2	LID 11	LID 10	LID 04	LID 03	LID 02	LID 01	LID 00
LIDR1	0	LID 54	LID 53	LID 52	LID 51	LID 50	LID 44	LID 43	LID4 2	LID 41	LID 40	LID 34	LID 33	LID 32	LID 31	LID 30
LIDR2	0	LID 84	LID 83	LID 82	LID 81	LID 80	LID 74	LID 73	LID7 2	LID 71	LID 70	LID 64	LID 63	LID 62	LID 61	LID 60
LIDR3	0	LID 114	LID 113	LID 112	LID 111	LID 110	LID 104	LID 103	LID1 02	LID 101	LID 100	LID 94	LID 93	LID 92	LID 91	LID 90
LIDR4	0	LID 144	LID 143	LID 142	LID 141	LID 140	LID 134	LID 133	LID1 32	LID 131	LID 130	LID 124	LID 123	LID 122	LID 121	LID 120
LIDR5	0	LID 174	LID 173	LID 172	LID 171	LID 170	LID 164	LID 163	LID1 62	LID 161	LID 160	LID 154	LID 153	LID 152	LID 151	LID 150
LIDR6	0	LID 204	LID 203	LID 202	LID 201	LID 200	LID 194	LID 193	LID1 92	LID 191	LID 190	LID 184	LID 183	LID 182	LID 181	LID 180
LIDR7	0	LID 234	LID 233	LID 232	LID 231	LID 230	LID 224	LID 223	LID2 22	LID 221	LID 220	LID 214	LID 213	LID 212	LID 211	LID 210
LIDR8	0	LID 264	LID 263	LID 262	LID 261	LID 260	LID 254	LID 253	LID2 52	LID 251	LID 250	LID 244	LID 243	LID 242	LID 241	LID 240
LIDR9	0	LID 294	LID 293	LID 292	LID 291	LID 290	LID 284	LID 283	LID2 82	LID 281	LID 280	LID 274	LID 273	LID 272	LID 271	LID 270
LIDR10	0	LID 324	LID 323	LID 322	LID 321	LID 320	LID 314	LID 313	LID3 12	LID 311	LID 310	LID 304	LID 303	LID 302	LID 301	LID 300
LIDR11	0	LID 354	LID 353	LID 352	LID 351	LID 350	LID 344	LID 343	LID3 42	LID 341	LID 340	LID 334	LID 333	LID 332	LID 331	LID 330
LIDR12	0	LID 384	LID 383	LID 382	LID 381	LID 380	LID 374	LID 373	LID3 72	LID 371	LID 370	LID 364	LID 363	LID 362	LID 361	LID 360
LIDR13	0	LID 414	LID 413	LID 412	LID 411	LID 410	LID 404	LID 403	LID4 02	LID 401	LID 400	LID 394	LID 393	LID 392	LID 391	LID 390
LIDR14	0	LID 444	LID 443	LID 442	LID 441	LID 440	LID 434	LID 433	LID4 32	LID 431	LID 430	LID 424	LID 423	LID 422	LID 421	LID 420
LIDR15	0	LID 474	LID 473	LID 472	LID 471	LID 470	LID 464	LID 463	LID4 62	LID 461	LID 460	LID 454	LID 453	LID 452	LID 451	LID 450

Name	Description
Note 1: n denotes a LSTi stream number from 0 to 47.	

Table 11 - Local Input Bit Delay Registers (LIDR0 to LIDR15)

Read/Write Address: 0052_H - 00057_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIDR16	0	LID 504	LID 503	LID 502	LID 501	LID 500	LID 494	LID 493	LID4 92	LID 491	LID 490	LID 484	LID 483	LID 482	LID 481	LID 480
LIDR17	0	LID 534	LID 533	LID 532	LID 531	LID 530	LID 524	LID 523	LID5 22	LID 521	LID 520	LID 514	LID 513	LID 512	LID 511	LID 510
LIDR18	0	LID 564	LID 563	LID 562	LID 561	LID 560	LID 554	LID 553	LID5 52	LID 551	LID 550	LID 544	LID 543	LID 542	LID 541	LID 540
LIDR19	0	LID 594	LID 593	LID 592	LID 591	LID 590	LID 584	LID 583	LID5 82	LID 581	LID 580	LID 574	LID 573	LID 572	LID 571	LID 570
LIDR20	0	LID 624	LID 623	LID 622	LID 621	LID 620	LID 614	LID 613	LID6 12	LID 611	LID 610	LID 604	LID 603	LID 602	LID 601	LID 600
LIDR21	0	0	0	0	0	0	0	0	0	0	0	LID 634	LID 633	LID 632	LID 631	LID 630

Name	Description
LIDn4 - LIDn0 (See Note 1)	**Local Input Bit Delay Bits 4 - 0:** The binary value of these five bits defines the local input bit delay of the LSTi inputs. The local input bit delay can be selected from 0 to 7 3/4 $\overline{C8o}$ clock periods. See Table 13 for details.

Note 1: n denotes a LSTi stream number from 48 to 63.

Table 12 - Local Input Bit Delay Registers (LIDR16 to LIDR21)

Local Input Delay		Corresponding Delay Bits				
$\overline{C8o}$ (period)	8.192 Mb/s (bit)	LIDn4	LIDn3	LIDn2	LIDn1	LIDn0
0 (Default)	0	0	0	0	0	0
1/4	1/4	0	0	0	0	1
1/2	1/2	0	0	0	1	0
3/4	3/4	0	0	0	1	1
1	1	0	0	1	0	0
1 1/4	1 1/4	0	0	1	0	1
1 1/2	1 1/2	0	0	1	1	0
1 3/4	1 3/4	0	0	1	1	1
2	2	0	1	0	0	0
2 1/4	2 1/4	0	1	0	0	1
2 1/2	2 1/2	0	1	0	1	0
2 3/4	2 3/4	0	1	0	1	1
3	3	0	1	1	0	0

Table 13 - Local Input Bit Delay Programming Table

Local Input Delay		Corresponding Delay Bits				
$\overline{\text{C8o}}$ (period)	8.192 Mb/s (bit)	LIDn4	LIDn3	LIDn2	LIDn1	LIDn0
3 1/4	3 1/4	0	1	1	0	1
3 1/2	3 1/2	0	1	1	1	0
3 3/4	3 3/4	0	1	1	1	1
4	4	1	0	0	0	0
4 1/4	4 1/4	1	0	0	0	1
4 1/2	4 1/2	1	0	0	1	0
4 3/4	4 3/4	1	0	0	1	1
5	5	1	0	1	0	0
5 1/4	5 1/4	1	0	1	0	1
5 1/2	5 1/2	1	0	1	1	0
5 3/4	5 3/4	1	0	1	1	1
6	6	1	1	0	0	0
6 1/4	6 1/4	1	1	0	0	1
6 1/2	6 1/2	1	1	0	1	0
6 3/4	6 3/4	1	1	0	1	1
7	7	1	1	1	0	0
7 1/4	7 1/4	1	1	1	0	1
7 1/2	7 1/2	1	1	1	1	0
7 3/4	7 3/4	1	1	1	1	1

Table 13 - Local Input Bit Delay Programming Table (continued)

Read/Write Address: 0058_H - $0005D_H$
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDR0	0	BID 24	BID 23	BID 22	BID 21	BID 20	BID 14	BID 13	BID 12	BID 11	BID 10	BID 04	BID 03	BID 02	BID 01	BID 00
BIDR1	0	BID 54	BID 53	BID 52	BID 51	BID 50	BID 44	BID 43	BID 42	BID 41	BID 40	BID 34	BID 33	BID 32	BID 31	BID 30
BIDR2	0	BID 84	BID 83	BID 82	BID 81	BID 80	BID 74	BID 73	BID 72	BID 71	BID 70	BID 64	BID 63	BID 62	BID 61	BID 60
BIDR3	0	BID 114	BID 113	BID 112	BID 111	BID 110	BID 104	BID 103	BID 102	BID 101	BID 100	BID 94	BID 93	BID 92	BID 91	BID 90
BIDR4	0	BID 144	BID 143	BID 142	BID 141	BID 140	BID 134	BID 133	BID 132	BID 131	BID 130	BID 124	BID 123	BID 122	BID 121	BID 120
BIDR5	0	BID 174	BID 173	BID 172	BID 171	BID 170	BID 164	BID 163	BID 162	BID 161	BID 160	BID 154	BID 153	BID 152	BID 151	BID 150

Name	Description
BIDn4 - BIDn0 (See Note 1)	**Backplane Input Bit Delay Bits 4 - 0:** The binary value of these five bits defines the backplane input bit delay of the BSTi inputs. The backplane input bit delay can be selected from 0 to 3 7/8 C8i clock periods. See Table 16 for details.

Note 1: n denotes a BSTi stream number from 0 to 17.

Table 14 - Backplane Input Bit Delay Registers (BIDR0 to BIDR5)

Read/Write Address: $005E_H$ - $0006D_H$
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDR6	0	BID 204	BID 203	BID 202	BID 201	BID 200	BID 194	BID 193	BID 192	BID 191	BID 190	BID 184	BID 183	BID 182	BID 181	BID 180
BIDR7	0	BID 234	BID 233	BID 232	BID 231	BID 230	BID 224	BID 223	BID 222	BID 221	BID 220	BID 214	BID 213	BID 212	BID 211	BID 210
BIDR8	0	BID 264	BID 263	BID 262	BID 261	BID 260	BID 254	BID 253	BID 252	BID 251	BID 250	BID 244	BID 243	BID 242	BID 241	BID 240
BIDR9	0	BID 294	BID 293	BID 292	BID 291	BID 290	BID 284	BID 283	BID 282	BID 281	BID 280	BID 274	BID 273	BID 272	BID 271	BID 270
BIDR10	0	BID 324	BID 323	BID 322	BID 321	BID 320	BID 314	BID 313	BID 312	BID 311	BID 310	BID 304	BID 303	BID 302	BID 301	BID 300
BIDR11	0	BID 354	BID 353	BID 352	BID 351	BID 350	BID 344	BID 343	BID 342	BID 341	BID 340	BID 334	BID 333	BID 332	BID 331	BID 330
BIDR12	0	BID 384	BID 383	BID 382	BID 381	BID 380	BID 374	BID 373	BID 372	BID 371	BID 370	BID 364	BID 363	BID 362	BID 361	BID 360
BIDR13	0	BID 414	BID 413	BID 412	BID 411	BID 410	BID 404	BID 403	BID 402	BID 401	BID 400	BID 394	BID 393	BID 392	BID 391	BID 390
BIDR14	0	BID 444	BID 443	BID 442	BID 441	BID 140	BID 434	BID 433	BID 432	BID 431	BID 430	BID 424	BID 423	BID 422	BID 421	BID 420
BIDR15	0	BID 474	BID 473	BID 472	BID 471	BID 470	BID 464	BID 463	BID 462	BID 461	BID 460	BID 454	BID 453	BID 452	BID 451	BID 450
BIDR16	0	BID 504	BID 503	BID 502	BID 501	BID 500	BID 494	BID 493	BID 492	BID 491	BID 490	BID 484	BID 483	BID 482	BID 481	BID 480
BIDR17	0	BID 534	BID 533	BID 532	BID 531	BID 530	BID 524	BID 523	BID 522	BID 521	BID 520	BID 514	BID 513	BID 512	BID 511	BID 510
BIDR18	0	BID 564	BID 563	BID 562	BID 561	BID 560	BID 554	BID 553	BID 552	BID 551	BID 550	BID 544	BID 543	BID 542	BID 541	BID 540
BIDR19	0	BID 594	BID 593	BID 592	BID 591	BID 590	BID 584	BID 583	BID 582	BID 581	BID 580	BID 574	BID 573	BID 572	BID 571	BID 570
BIDR20	0	BID 624	BID 623	BID 622	BID 621	BID 620	BID 614	BID 613	BID 612	BID 611	BID 610	BID 604	BID 603	BID 602	BID 601	BID 600
BIDR21	0	0	0	0	0	0	0	0	0	0	0	BID 634	BID 633	BID 632	BID 631	BID 630

Name	Description
BIDn4 - BIDn0 (See Note 1)	**Backplane Input Bit Delay Bits 4 - 0:** The binary value of these five bits defines the backplane input bit delay of the BSTi inputs. The backplane input bit delay can be selected from 0 to 3 7/8 C8i clock periods. See Table 16 for details.

Table 15 - Backplane Input Bit Delay Registers (BIDR0 to BIDR5)

Read/Write Address: $005E_H$ - $0006D_H$
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDR6	0	BID 204	BID 203	BID 202	BID 201	BID 200	BID 194	BID 193	BID 192	BID 191	BID 190	BID 184	BID 183	BID 182	BID 181	BID 180
BIDR7	0	BID 234	BID 233	BID 232	BID 231	BID 230	BID 224	BID 223	BID 222	BID 221	BID 220	BID 214	BID 213	BID 212	BID 211	BID 210
BIDR8	0	BID 264	BID 263	BID 262	BID 261	BID 260	BID 254	BID 253	BID 252	BID 251	BID 250	BID 244	BID 243	BID 242	BID 241	BID 240
BIDR9	0	BID 294	BID 293	BID 292	BID 291	BID 290	BID 284	BID 283	BID 282	BID 281	BID 280	BID 274	BID 273	BID 272	BID 271	BID 270
BIDR10	0	BID 324	BID 323	BID 322	BID 321	BID 320	BID 314	BID 313	BID 312	BID 311	BID 310	BID 304	BID 303	BID 302	BID 301	BID 300
BIDR11	0	BID 354	BID 353	BID 352	BID 351	BID 350	BID 344	BID 343	BID 342	BID 341	BID 340	BID 334	BID 333	BID 332	BID 331	BID 330
BIDR12	0	BID 384	BID 383	BID 382	BID 381	BID 380	BID 374	BID 373	BID 372	BID 371	BID 370	BID 364	BID 363	BID 362	BID 361	BID 360
BIDR13	0	BID 414	BID 413	BID 412	BID 411	BID 410	BID 404	BID 403	BID 402	BID 401	BID 400	BID 394	BID 393	BID 392	BID 391	BID 390
BIDR14	0	BID 444	BID 443	BID 442	BID 441	BID 140	BID 434	BID 433	BID 432	BID 431	BID 430	BID 424	BID 423	BID 422	BID 421	BID 420
BIDR15	0	BID 474	BID 473	BID 472	BID 471	BID 470	BID 464	BID 463	BID 462	BID 461	BID 460	BID 454	BID 453	BID 452	BID 451	BID 450
BIDR16	0	BID 504	BID 503	BID 502	BID 501	BID 500	BID 494	BID 493	BID 492	BID 491	BID 490	BID 484	BID 483	BID 482	BID 481	BID 480
BIDR17	0	BID 534	BID 533	BID 532	BID 531	BID 530	BID 524	BID 523	BID 522	BID 521	BID 520	BID 514	BID 513	BID 512	BID 511	BID 510
BIDR18	0	BID 564	BID 563	BID 562	BID 561	BID 560	BID 554	BID 553	BID 552	BID 551	BID 550	BID 544	BID 543	BID 542	BID 541	BID 540
BIDR19	0	BID 594	BID 593	BID 592	BID 591	BID 590	BID 584	BID 583	BID 582	BID 581	BID 580	BID 574	BID 573	BID 572	BID 571	BID 570
BIDR20	0	BID 624	BID 623	BID 622	BID 621	BID 620	BID 614	BID 613	BID 612	BID 611	BID 610	BID 604	BID 603	BID 602	BID 601	BID 600
BIDR21	0	0	0	0	0	0	0	0	0	0	0	BID 634	BID 633	BID 632	BID 631	BID 630

Name	Description
Note 1: n denotes a BSTi stream number from 18 to 63.	

Table 15 - Backplane Input Bit Delay Registers (BIDR0 to BIDR5) (continued)

Backplane Input Delay			Corresponding Delay Bits				
$\overline{C8i}$ (period)	16.384Mb/s (bit)	32.768Mb/s (bit)	BIDn4	BIDn3	BIDn2	BIDn1	BIDn0
0 (Default)	0	0	0	0	0	0	0
1/8	1/4	1/2	0	0	0	0	1
1/4	1/2	1	0	0	0	1	0
3/8	3/4	1 1/2	0	0	0	1	1
1/2	1	2	0	0	1	0	0
5/8	1 1/4	2 1/2	0	0	1	0	1
3/4	1 1/2	3	0	0	1	1	0
7/8	1 3/4	3 1/2	0	0	1	1	1
1	2	4	0	1	0	0	0
1 1/8	2 1/4	4 1/2	0	1	0	0	1
1 1/4	2 1/2	5	0	1	0	1	0
1 3/8	2 3/4	5 1/2	0	1	0	1	1
1 1/2	3	6	0	1	1	0	0
1 5/8	3 1/4	6 1/2	0	1	1	0	1
1 3/4	3 1/2	7	0	1	1	1	0
1 7/8	3 3/4	7 1/2	0	1	1	1	1
2	4	N/A	1	0	0	0	0
2 1/8	4 1/4		1	0	0	0	1
2 1/4	4 1/2		1	0	0	1	0
2 3/8	4 3/4		1	0	0	1	1
2 1/2	5		1	0	1	0	0
2 5/8	5 1/4		1	0	1	0	1
2 3/4	5 1/2		1	0	1	1	0
2 7/8	5 3/4		1	0	1	1	1
3	6		1	1	0	0	0
3 1/8	6 1/4		1	1	0	0	1
3 1/4	6 1/2		1	1	0	1	0
3 3/8	6 3/4		1	1	0	1	1
3 1/2	7		1	1	1	0	0
3 5/8	7 1/4		1	1	1	0	1
3 3/4	7 1/2		1	1	1	1	
3 7/8	7 3/4		1	1	1	1	

Table 16 - Backplane Input Bit Delay Programming Table

Read/Write Address: $006E_H$ - 00075_H
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAR0	LOA 71	LOA 70	LOA 61	LOA 60	LOA 51	LOA 50	LOA 41	LOA 40	LOA 31	LOA 30	LOA 21	LOA 20	LOA 11	LOA 10	LOA 01	LOA 00
LOAR1	LOA 151	LOA 150	LOA 141	LOA 140	LOA 131	LOA 130	LOA 121	LOA 120	LOA 111	LOA 110	LOA 101	LOA 100	LOA 91	LOA 90	LOA 81	LOA 80
LOAR2	LOA 231	LOA 230	LOA 221	LOA 220	LOA 211	LOA 210	LOA 201	LOA 200	LOA 191	LOA 190	LOA 181	LOA 180	LOA 171	LOA 170	LOA 161	LOA 160
LOAR3	LOA 311	LOA 310	LOA 301	LOA 300	LOA 291	LOA 290	LOA 281	LOA 280	LOA 271	LOA 270	LOA 271	LOA 260	LOA 251	LOA 250	LOA 241	LOA 240
LOAR4	LOA 391	LOA 390	LOA 381	LOA 380	LOA 371	LOA 370	LOA 361	LOA 360	LOA 351	LOA 350	LOA 341	LOA 340	LOA 331	LOA 330	LOA 321	LOA 320
LOAR5	LOA 471	LOA 470	LOA 461	LOA 460	LOA 451	LOA 450	LOA 441	LOA 440	LOA 431	LOA 430	LOA 421	LOA 420	LOA 411	LOA 410	LOA 401	LOA 400
LOAR6	LOA 551	LOA 550	LOA 541	LOA 540	LOA 531	LOA 530	LOA 521	LOA 520	LOA 511	LOA 510	LOA 501	LOA 500	LOA 491	LOA 490	LOA 481	LOA 480
LOAR7	LOA 631	LOA 630	LOA 621	LOA 620	LOA 611	LOA 610	LOA 601	LOA 600	LOA 591	LOA 590	LOA 581	LOA 580	LOA 571	LOA 570	LOA 561	LOA 560

Name	Description
LOAn1 - LOAn0 (See Note 1)	**Local Output Advancement Bits 1 - 0:** The binary value of these two bits defines the local output advancement of the LSTo outputs. The local output advancement can be selected from 0 to - 3/8 $\overline{C8o}$ clock periods. See Table 18 for details.

Note 1: n denotes a LSTo stream number from 0 to 63.

Table 17 - Local Output Advancement Registers (LOAR0 to LOAR7)

Local Output Advancement		Corresponding Advancement Bits	
$\overline{C8o}$ (period)	**8.192Mb/s (bit)**	**LOAn1**	**LOAn0**
0 (Default)	0	0	0
- 1/8	- 1/8	0	1
- 1/4	- 1/4	1	0
- 3/8	- 3/8	1	1

Table 18 - Local Output Advancement Programming Table

Read/Write Address: 0076_H - $0007D_H$
Reset Value: 0000_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOAR0	BOA 71	BOA 70	BOA 61	BOA 60	BOA 51	BOA 50	BOA 41	BOA 40	BOA 31	BOA 30	BOA 21	BOA 20	BOA 11	BOA 10	BOA 01	BOA 00
BOAR1	BOA 151	BOA 150	BOA 141	BOA 140	BOA 131	BOA 130	BOA 121	BOA 120	BOA 111	BOA 110	BOA 101	BOA 100	BOA 91	BOA 90	BOA 81	BOA 80
BOAR2	BOA 231	BOA 230	BOA 221	BOA 220	BOA 211	BOA 210	BOA 201	BOA 200	BOA 191	BOA 190	BOA 181	BOA 180	BOA 171	BOA 170	BOA 161	BOA 160
BOAR3	BOA 311	BOA 310	BOA 301	BOA 300	BOA 291	BOA 290	BOA 281	BOA 280	BOA 271	BOA 270	BOA 271	BOA 260	BOA 251	BOA 250	BOA 241	BOA 240
BOAR4	BOA 391	BOA 390	BOA 381	BOA 380	BOA 371	BOA 370	BOA 361	BOA 360	BOA 351	BOA 350	BOA 341	BOA 340	BOA 331	BOA 330	BOA 321	BOA 320
BOAR5	BOA 471	BOA 470	BOA 461	BOA 460	BOA 451	BOA 450	BOA 441	BOA 440	BOA 431	BOA 430	BOA 421	BOA 420	BOA 411	BOA 410	BOA 401	BOA 400
BOAR6	BOA 551	BOA 550	BOA 541	BOA 540	BOA 531	BOA 530	BOA 521	BOA 520	BOA 511	BOA 510	BOA 501	BOA 500	BOA 491	BOA 490	BOA 481	BOA 480
BOAR7	BOA 631	BOA 630	BOA 621	BOA 620	BOA 611	BOA 610	BOA 601	BOA 600	BOA 591	BOA 590	BOA 581	BOA 580	BOA 571	BOA 570	BOA 561	BOA 560

Name	Description
BOAn1 - BOAn0 (See Note 1)	**Backplane Output Advancement Bits 1 - 0:** The binary value of these two bits defines the backplane output advancement of the BSTo outputs. The backplane output advancement can be selected from 0 to - 3/8 C8i clock periods. See Table 20 for details.

Note 1: n denotes a BSTo stream number from 0 to 63.

Table 19 - Backplane Output Advancement Registers (BOAR0 to BOAR7)

Backplane Output Advancement			Corresponding Advancement Bits	
$\overline{\text{C8i}}$ (period)	16.384 Mb/s (bit)	32.768 Mb/s (bit)	BOAn1	BOAn0
0 (Default)	0	0	0	0
- 1/8	- 1/4	- 1/2	0	1
- 1/4	- 1/2	- 1	1	0
- 3/8	- 3/4	- 1 1/2	1	1

Table 20 - Backplane Output Advancement Programming Table

Read/Write Address: $007E_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	BDS B5	BDS B4	BDS B3	BDS B2	BDS B1	BDS B0	BDS A5	BDS A4	BDS A3	BDS A2	BDS A1	BDS A0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
11 - 6	BDSB5 - 0	**Backplane Data Stream Address Bits for Stream B:** The binary value of these bits refers to the backplane input data stream.
5 - 0	BDSA5 - 0	**Backplane Data Stream Address Bits for Stream A:** The binary value of these bits refers to the backplane input data stream.

Table 21 - Backplane Data Input Selection Register (BDISR) Bits

Read/Write Address: $007F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	BDS D5	BDS D4	BDS D3	BDS D2	BDS D1	BDS D0	BDS C5	BDS C4	BDS C3	BDS C2	BDS C1	BDS C0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
11 - 6	BDSD5 - 0	**Backplane Data Stream Address Bits for Stream D:** The binary value of these bits refers to the backplane input data stream.
5 - 0	BDSC5 - 0	**Backplane Data Stream Address Bits for Stream C:** The binary value of these bits refers to the backplane input data stream.

Table 22 - Backplane Data Memory Read Selection Register (BDMRSR) Bits

Read/Write Address: 0080_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LDS F5	LDS F4	LDS F3	LDS F2	LDS F1	LDS F0	LDS E5	LDS E4	LDS E3	LDS E2	LDS E1	LDS E0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
11 - 6	LDSF5 - 0	**Local Data Stream Address Bits for Stream F:** The binary value of these bits refers to the local input data stream.

Table 23 - Local Data Memory Read Selection Register (LDMRSR) Bits

Read/Write Address: 0080_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LDS F5	LDS F4	LDS F3	LDS F2	LDS F1	LDS F0	LDS E5	LDS E4	LDS E3	LDS E2	LDS E1	LDS E0

Bit	Name	Description
5 - 0	LDSE5 - 0	**Local Data Stream Address Bits for Stream E:** The binary value of these bits refers to the local input data stream.

Table 23 - Local Data Memory Read Selection Register (LDMRSR) Bits (continued)

Read/Write Address: 0081_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	LBR SA5	LBR SA4	LBR SA3	LBR SA2	LBR SA1	LBR SA0	LBR CA6	LBR CA5	LBR CA4	LBR CA3	LBR CA2	LBR CA1	LBR CA0

Bit	Name	Description
15 - 13	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
12 - 7	LBRSA5 - 0	**Local BER Receive Stream Address Bits:** The binary value of these bits refers to the local input stream which receives the BER data.
6 - 0	LBRCA6 - 0	**Local BER Receive Channel Address Bits:** The binary value of these bits refers to the local input channel in which the BER data starts to be compared.

Table 24 - Local BER Start Receiving Register (LBSRR) Bits

Read/Write Address: 0082_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	LBL6	LBL5	LBL4	LBL3	LBL2	LBL1	LBL0

Bit	Name	Description
15 - 7	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
6 - 0	LBL6 - 0	**Local BER Length Bits:** The binary value of these bits refers to the number of channels, the BER data will last. The maximum number of local BER channels is 127.

Table 25 - Local BER Length Register (LBLR) Bits

Read/Write Address: 0083_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LBC 15	LBC 14	LBC 13	LBC 12	LBC 11	LBC 10	LBC 9	LBC 8	LBC 7	LBC 6	LBC 5	LBC 4	LBC 3	LBC 2	LBC 1	LBC 0

Bit	Name	Description
15 - 0	LBC15 - 0	**Local Bit Error Rate Count:** The binary value of these bits refers to the local bit error count.

Table 26 - Local BER Count Register (LBCR) Bits

Read/Write Address: 0084_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	BBR SA5	BBR SA4	BBR SA3	BBR SA2	BBR SA1	BBR SA0	BBR CA8	BBR CA7	BBR CA6	BBR CA5	BBR CA4	BBR CA3	BBR CA2	BBR CA1	BBR CA0

Bit	Name	Description
15	Unused	**Reserved.** In normal functional mode, this bit MUST be set to zero.
14 - 9	BBRSA5 - 0	**Backplane BER Receive Stream Address Bits:** The binary value of these bits refers to the backplane input stream which receives the BER data.
8 - 0	BBRCA8 - 0	**Backplane BER Receive Channel Address Bits:** The binary value of these bits refers to the backplane input channel in which the BER data starts to be compared.

Table 27 - Backplane BER Start Receiving Register (BBSRR) Bits

Read/Write Address: 0085_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	BBL8	BBL7	BBL6	BBL5	BBL4	BBL3	BBL2	BBL1	BBL0

Bit	Name	Description
15 - 9	Unused	**Reserved.** In normal functional mode, these bits MUST be set to zero.
8 - 0	BBL8 - 0	**Backplane BER Length Bits:** The binary value of these bits refers to the number of channels, the BER data will last. The maximum number of backplane BER channels is 511.

Table 28 - Backplane BER Length Register (BBLR) Bits

Read/Write Address: 0086_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BBC 15	BBC 14	BBC 13	BBC 12	BBC 11	BBC 10	BBC 9	BBC 8	BBC 7	BBC 6	BBC 5	BBC 4	BBC 3	BBC 2	BBC 1	BBC 0

Bit	Name	Description
15 - 0	BBC15 - 0	**Backplane Bit Error Rate Count:** The binary value of these bits refers to the backplane bit error count.

Table 29 - Backplane BER Count Register (BBCR) Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LMSC	LSAB 5	LSAB 4	LSAB 3	LSAB 2	LSAB 1	LSAB 0	LCAB 8	LCAB 7	LCAB 6	LCAB 5	LCAB 4	LCAB 3	LCAB 2	LCAB 1	LCAB 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>15</td><td>LMSC</td><td>Local Mode Selection Control: When this bit and the LTM0, LTM1 bits in the local connection memory high are low, the "backplane-to-local" switching is enabled.
<table>
<tr><th>LMSC</th><th>LTM1 Bit in LCMH</th><th>LTM0 Bit in LCMH</th><th>Per-Channel Operation Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>'Backplane-to-local' switching</td></tr>
</table>
When this bit is high, the content of the LTM0, LTM1 bits in the local connection memory high select one of the operation modes described in the table below:.
<table>
<tr><th>LMSC</th><th>LTM1 Bit in LCMH</th><th>LTM0 Bit in LCMH</th><th>Per-Channel Operation Mode</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>'Local-to-local switching'</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>High Impedance</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Msg Mode</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>BER Test Mode</td></tr>
</table></td></tr>
<tr><td>14 - 9</td><td>LSAB5 - 0</td><td>Local Source Stream Address Bits: The binary value of these 6 bits represents the data stream number for the source (local or backplane) connection.</td></tr>
<tr><td>8 - 0*</td><td>LCAB8 - 0</td><td>Local Source Channel Address Bits: The binary value of these 9 bits represents the channel number that is the source (local or backplane) connection.</td></tr>
<tr><td colspan="3">*Note: Only Bit 7-0 will be used for per-channel message mode.</td></tr>
</table>

Table 30 - Local Connection Memory low (LCML) Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	LTM 1	LTM 0

Bit	Name	Description
15 - 2	Unused	**Reserved.**
1 - 0	LTM1 - 0	**Local TM Bits:** These two bits control the LSTo output.

LTM1	LTM0	LMSC Bit in LCML	Per-Channel Operation Mode
0	0	0	'Backplane-to-local' switching
0	0	1	'Local-to-local' switching
0	1	1	High Impedance
1	0	1	Msg Mode
1	1	1	BER Test Mode

Table 31 - Local Connection Memory High (LCMH) Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSRC = 0	BTM 1	BTM 0	BSA B5	BSA B4	BSA B3	BSA B2	BSA B1	BSA B0	BCA B6	BCA B5	BCA B4	BCA B3	BCA B2	BCA B1	BCA B0

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit:** When this bit is low, the "local-to-backplane" switching is enabled and the source is from the local input port.
14 - 13	BTM1 - 0	**Backplane TM Bits:** These two bits control the backplane outputs.

BTM1	BTM0	Per-Channel Operation Mode
0	0	Normal Output
0	1	Tristate/Driven-High (See Bit 15 (BHIZ) in Table 5)
1	0	Msg Mode
1	1	BER Test Mode

12 - 7*	BSAB5 - 0	**Backplane Source Stream Address Bits:** The binary value of these 6 bits represents the local data input stream number.
6 - 0 *	BCAB6 - 0	**Source Channel Address Bits:** The binary value of these 7 bits represents the local input channel number.

*Note: Only Bit 7-0 will be used for per-channel message mode.
*Note: The last channel (Ch255 or Ch511) of the backplane output streams BSTo60 to BSTo63 or BSTo58 to BSTo63 contains invalid output data when operated in the 16Mb/s or 32Mb/s mode respectively. Avoid using the last channel of these streams for the "local-to-backplane" switching.

Table 32 - Backplane Connection Memory (BCM) Bits for "Local-to-Backplane" Switching

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSRC = 1	BTM 1	BTM 0	0	0	0	BSA B0	BCA B8	BCA B7	BCA B6	BCA B5	BCA B4	BCA B3	BCA B2	BCA B1	BCA B0

Bit	Name	Description
15	BSRC	**Backplane Source Control Bit:** When this bit is high, the "backplane-to backplane" switching is enabled and the source is from the backplane input port.
14 - 13	BTM1 - 0	**Backplane TM Bits:** These two bits control the backplane outputs.
12-10	Unused	**Reserved.** Set to zero for normal operation.
9	BSAB0	**Backplane Source Stream Address Bits:** When this bit is low, the source stream (Stream A) is selected. Stream A is defined in the BDISR register. When this bit is high, the source stream (Stream B) is selected. Stream B is defined in the BDISR register.
8 - 0 *	BCAB8 - 0	**Source Channel Address Bits:** The binary value of these 9 bits represents the local input channel number.

BTM1	BTM0	Per-Channel Operation Mode
0	0	Normal Output
0	1	Tristate/Driven-High (See Bit 15 (BHIZ) in Table 5)
1	0	Msg Mode
1	1	BER Test Mode

*Note: Only Bit 7-0 will be used for per-channel message mode.

Table 33 - Backplane Connection Memory (BCM) Bits for "Backplane-to-Backplane" Switching

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
2	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
3	Input Voltage	V_{I_3V}	-0.5	V_{DD} + 0.5	V
4	Input Voltage (5V tolerant inputs)	V_{I_5V}	-0.5	7.0	V
5	Continuous Current at digital outputs	I_o		15	mA
6	Package power dissipation	P_D		2	W
7	Storage temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
3	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
4	Input Voltage	V_I	0	3.3	V_{DD_IO}	V
5	Input Voltage on 5 V Tolerant Inputs	V_{I_5V}	0	5.0	5.5	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Core Supply Current	I_{DD_CORE}			600	mA	Output unloaded
2	IO Pad Supply Current	I_{DD_IO}			380	mA	Output unloaded
3	Input High Voltage	V_{IH}	2.0			V	
4	Input Low Voltage	V_{IL}			0.8	V	
5	Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 \le < V_{IN} \le V_{DD\_IO}$ See Note 1
6	Weak Pulldown Current for 3 V tolerant input	I_{PD_3V}			50	µA	Input at V_{DD_IO}
7	Weak Pullup Current for 5 V tolerant input	I_{PU_5V}			-150	µA	Input at 0V
8	Weak Pulldown Current for 5 V tolerant input	I_{PD_5V}			150	µA	Input at V_{DD_IO}
9	Input Pin Capacitance	C_I			5	pF	
10	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10mA
11	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10mA
12	Output High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD\_IO}$
13	Output Pin Capacitance	C_O		5	10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figure: at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.

* Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	$0.5V_{DD\_IO}$	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD\_IO}$	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD\_IO}$	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - Backplane and Local Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Backplane Frame Pulse Width	t_{BFPW}	20	122	230	ns	
2	Backplane Frame Pulse Setup Time before $\overline{C8i}$ clock falling edge	t_{BFPS}	10		90	ns	
3	Backplane Frame Pulse Hold Time from $\overline{C8i}$ clock falling edge	t_{BFPH}	10		90	ns	
4	$\overline{C8i}$ Clock Period	t_{BCP}	120	122	124	ns	
5	$\overline{C8i}$ Clock Pulse Width High	t_{BCH}	50	61	70	ns	
6	$\overline{C8i}$ Clock Pulse Width Low	t_{BCL}	50	61	70	ns	
7	$\overline{C8i}$ Clock Rise/Fall Time	t_{rC8i}, t_{fC8i}	0	2	3	ns	
8	$\overline{C8i}$ Cycle to Cycle Variation	t_{CVC8i}	0	2	6	ns	

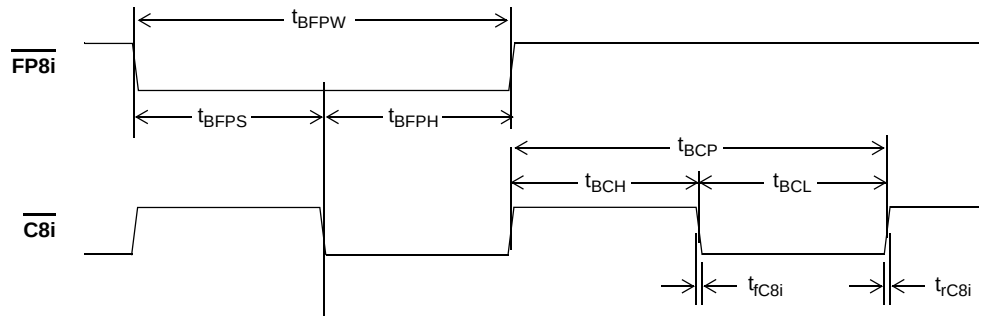
AC Electrical Characteristics† - Backplane and Local Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
9	$\overline{\text{FP4o}}$ Width	t_{FPW4}	220	244	270	ns	C_L=30pF
10	$\overline{\text{FP4o}}$ Output Setup from the $\overline{\text{FP4o}}$ falling edge to the $\overline{\text{C4o}}$ falling edge	t_{FOSF4}	110	122	135	ns	
11	$\overline{\text{FP4o}}$ Output Hold from the $\overline{\text{C4o}}$ falling edge to the $\overline{\text{FP4o}}$ rising edge	t_{FOHR4}	120	122	145	ns	
12	$\overline{\text{C4o}}$ Clock Period	t_{CP4}	239	244	249	ns	
13	$\overline{\text{C4o}}$ Clock Pulse Width High	t_{CH4}	110	122	135	ns	
14	$\overline{\text{C4o}}$ Clock Pulse Width Low	t_{CL4}	110	122	135	ns	
15	$\overline{\text{C4o}}$ Clock Rise/Fall Time	t_{rC4o}, t_{fC4o}			7	ns	
16	$\overline{\text{FP8o}}$ Width	t_{FPW8}	111	122	133	ns	
17	$\overline{\text{FP8o}}$ Output Setup from the $\overline{\text{FP8o}}$ falling edge to the $\overline{\text{C4o}}$ falling edge	t_{FOSF8}	50	61	75	ns	
18	$\overline{\text{FP8o}}$ Output Hold from the $\overline{\text{C4o}}$ falling edge to the $\overline{\text{FP8o}}$ Rising edge	t_{FOHR8}	60	61	80	ns	
19	$\overline{\text{C8o}}$ Clock Period	t_{CP8}	119	122	125	ns	
20	$\overline{\text{C8o}}$ Clock Pulse Width High	t_{CH8}	55	61	67	ns	
21	$\overline{\text{C8o}}$ Clock Pulse Width Low	t_{CL8}	55	61	67	ns	
22	$\overline{\text{C8o}}$ Clock Rise/Fall Time	t_{rC8o}, t_{fC8o}			7	ns	
23	$\overline{\text{FP16o}}$ Width	t_{FPW16}	55	61	67	ns	
24	$\overline{\text{FP16o}}$ Output Setup from the $\overline{\text{FP16o}}$ falling edge to the $\overline{\text{C4o}}$ falling edge	t_{FOSF16}	20	30	45	ns	
25	$\overline{\text{FP16o}}$ Output Hold from the $\overline{\text{C4o}}$ falling edge to the $\overline{\text{FP16o}}$ rising edge	t_{FOHR16}	30	40	50	ns	
26	$\overline{\text{C16o}}$ Clock Period	t_{CP16}	59	61	63	ns	
27	$\overline{\text{C16o}}$ Clock Pulse Width High	t_{CH16}	27	30	33	ns	
28	$\overline{\text{C16o}}$ Clock Pulse Width Low	t_{CL16}	27	30	33	ns	
29	$\overline{\text{C16o}}$ Clock Rise/Fall Time	t_{rC16o}, t_{fC16o}			7	ns	
30	$\overline{\text{C8i}}$ Cycle to Cycle Variation	t_{CVC8i}	0	2	6	ns	

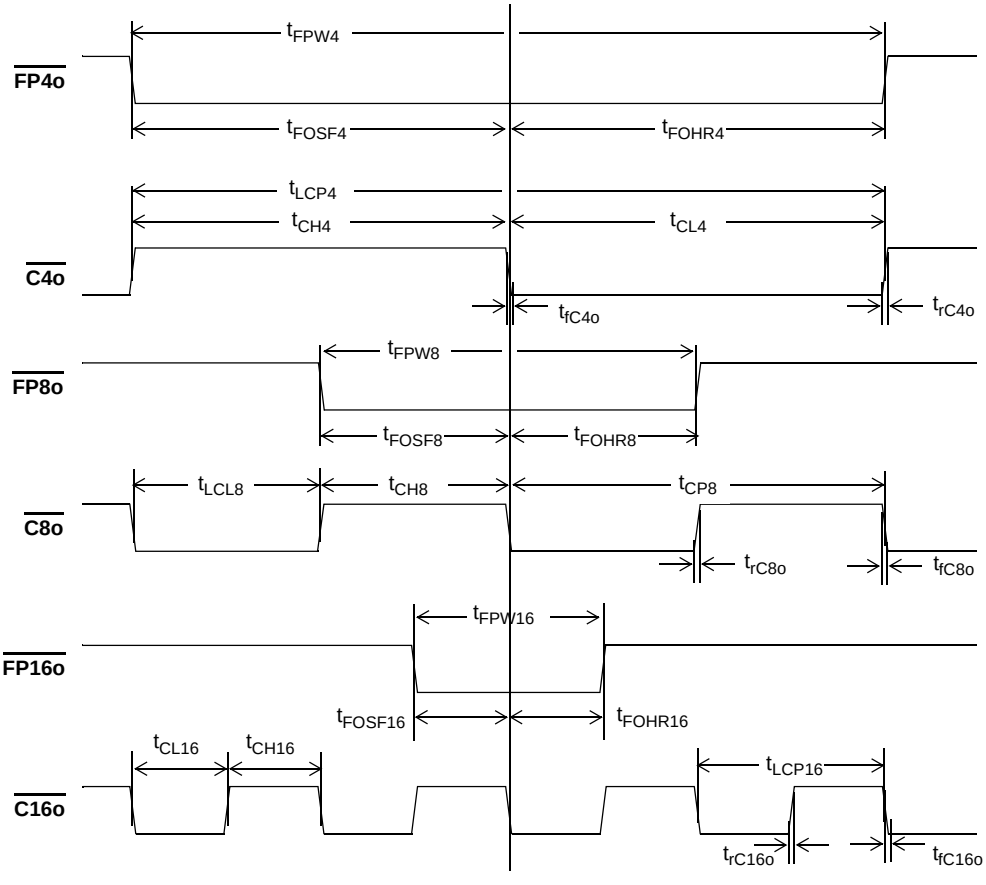
AC Electrical Characteristics† - Backplane and Local Clock Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
31	$\overline{\text{FP4o}}$ Width	t_{FPW4}	220	244	270	ns	C_L=30pF
32	$\overline{\text{FP4o}}$ Output Setup from the $\overline{\text{FP4o}}$ falling edge to the $\overline{\text{C4o}}$ falling edge	t_{FOSF4}	110	122	135	ns	
33	$\overline{\text{FP4o}}$ Output Hold from the $\overline{\text{C4o}}$ falling edge to the $\overline{\text{FP4o}}$ rising edge	t_{FOHR4}	120	122	145	ns	
34	$\overline{\text{C4o}}$ Clock Period	t_{CP4}	239	244	249	ns	
35	$\overline{\text{C4o}}$ Clock Pulse Width High	t_{CH4}	110	122	135	ns	
36	$\overline{\text{C4o}}$ Clock Pulse Width Low	t_{CL4}	110	122	135	ns	
37	$\overline{\text{C4o}}$ Clock Rise/Fall Time	t_{rC4o}, t_{fC4o}			7	ns	
38	$\overline{\text{FP8o}}$ Width	t_{FPW8}	111	122	133	ns	
39	$\overline{\text{FP8o}}$ Output Setup from the $\overline{\text{FP8o}}$ falling edge to the $\overline{\text{C4o}}$ falling edge	t_{FOSF8}	50	61	75	ns	
40	$\overline{\text{FP8o}}$ Output Hold from the $\overline{\text{C4o}}$ falling edge to the $\overline{\text{FP8o}}$ Rising edge	t_{FOHR8}	60	61	80	ns	
41	$\overline{\text{C8o}}$ Clock Period	t_{CP8}	119	122	125	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.



Backplane Port Timing



Local Port Timing

Figure 18 - Backplane and Local Clock Timing Diagram

AC Electrical Characteristics† - Backplane Data Timing for the 16 Mb/s mode

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Input data sampling point for Bit 0, Bit 2, Bit 4 and Bit 6	t_{IDS0} t_{IDS2} t_{IDS4} t_{IDS6}	106	107	108	ns	
2	Input data sampling point for Bit 1, Bit 3, Bit 5 and Bit 7	t_{IDS1} t_{IDS3} t_{IDS5} t_{IDS7}	45	46	47	ns	
3	Backplane Serial Input Set-up Time	t_{SIS}	3.5			ns	
4	Backplane Serial Input Hold Time	t_{SIH}	1.5			ns	
5	Backplane Serial Output Delay for Bit 0, Bit 2, Bit 4 and Bit 6	t_{SOD0} t_{SOD2} t_{SOD4} t_{SOD6}	68	73.5	79	ns	C_L=30pF
6	Backplane Serial Output Delay for Bit 1, Bit 3, Bit 5 and Bit 7	t_{SOD1} t_{SOD3} t_{SOD5} t_{SOD7}	7	12.5	18	ns	
See Figure 20 in the next page for the 16Mb/s mode backplane data timing diagram.							

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.

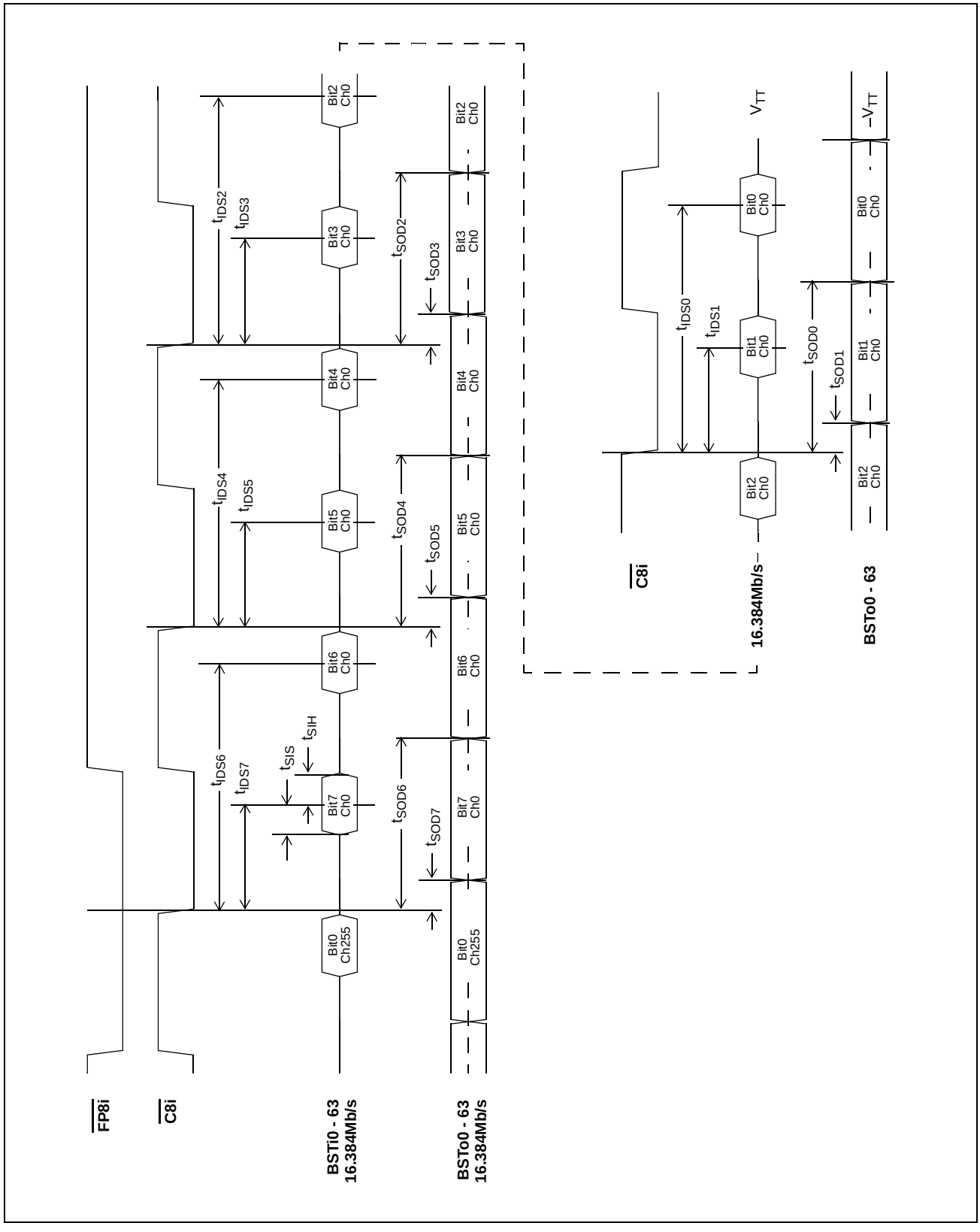


Figure 19 - Backplane Data Timing Diagram (16 Mb/s Mode)

AC Electrical Characteristics† - Backplane Data Timing for the 32 Mb/s mode

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Input data sampling point for Bit 0 and Bit 4	t_{IDS0} t_{IDS4}	113.5	114.5	115.5	ns	
2	Input data sampling point for Bit 1 and Bit 5	t_{IDS1} t_{IDS5}	82.6	83.6	84.6	ns	
3	Input data sampling point for Bit 2 and Bit 6	t_{IDS2} t_{IDS6}	52.3	53.3	54.3	ns	
4	Input data sampling point for Bit 3 and Bit 7	t_{IDS3} t_{IDS7}	21.8	22.8	23.8	ns	
5	Backplane Serial Input Set-up Time	t_{SIS}	3.5			ns	
6	Backplane Serial Input Hold Time	t_{SIH}	1.5			ns	
7	Backplane Serial Output Delay for Bit 0 and Bit 4	t_{SOD0} t_{SOD4}	99	103.5	108	ns	C_L=30pF
8	Backplane Serial Output Delay for Bit 1 and Bit 5	t_{SOD1} t_{SOD5}	69	73.5	78	ns	
9	Backplane Serial Output Delay for Bit 2 and Bit 6	t_{SOD2} t_{SOD6}	38	42.5	47	ns	
10	Backplane Serial Output Delay for Bit 3 and Bit 7	t_{SOD3} t_{SOD7}	8	12.5	17	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.

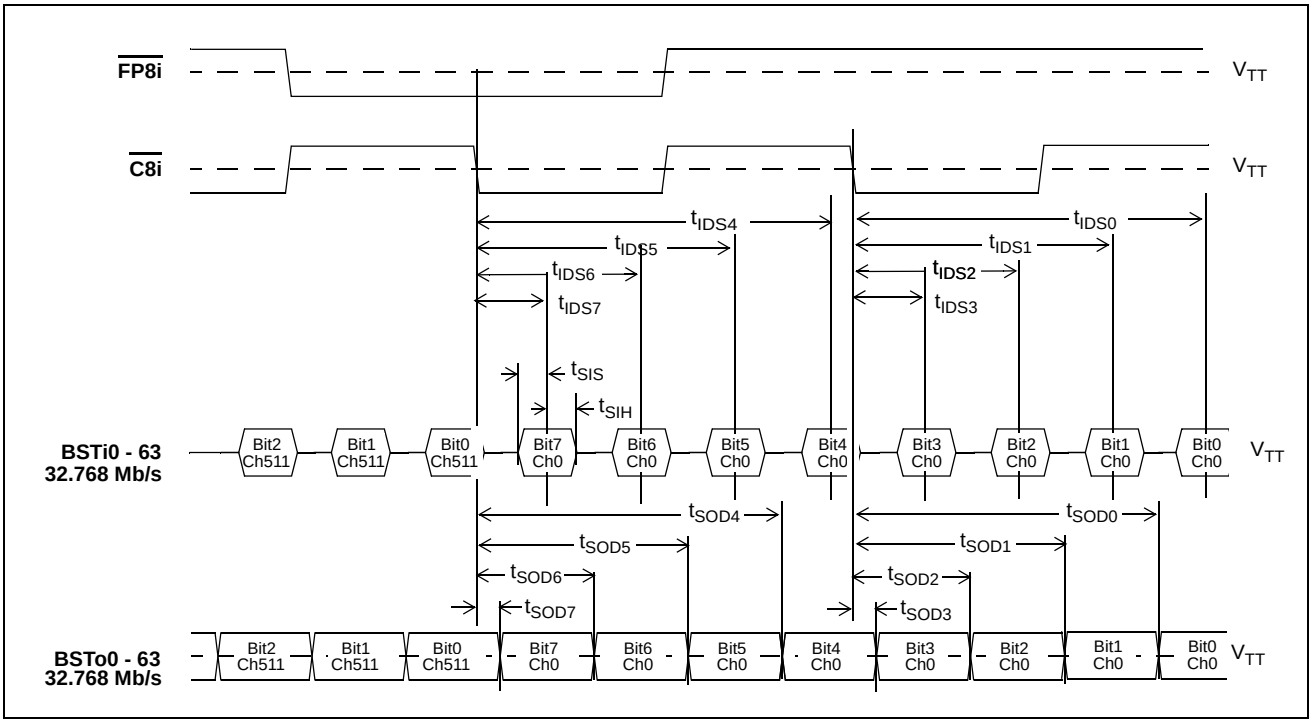


Figure 20 - Backplane Data Timing Diagram (32 Mb/s Mode)

AC Electrical Characteristics† - Local Data Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Input data sampling point	t_{IDS}	90	91.6	94	ns	
2	Local Serial Input Set-up Time	t_{SIS}	3.5			ns	
3	Local Serial Input Hold Time	t_{SIH}	1.5			ns	
4	Local Serial Output Delay	t_{SOD}	7	12.5	18	ns	C_L=30pF

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.

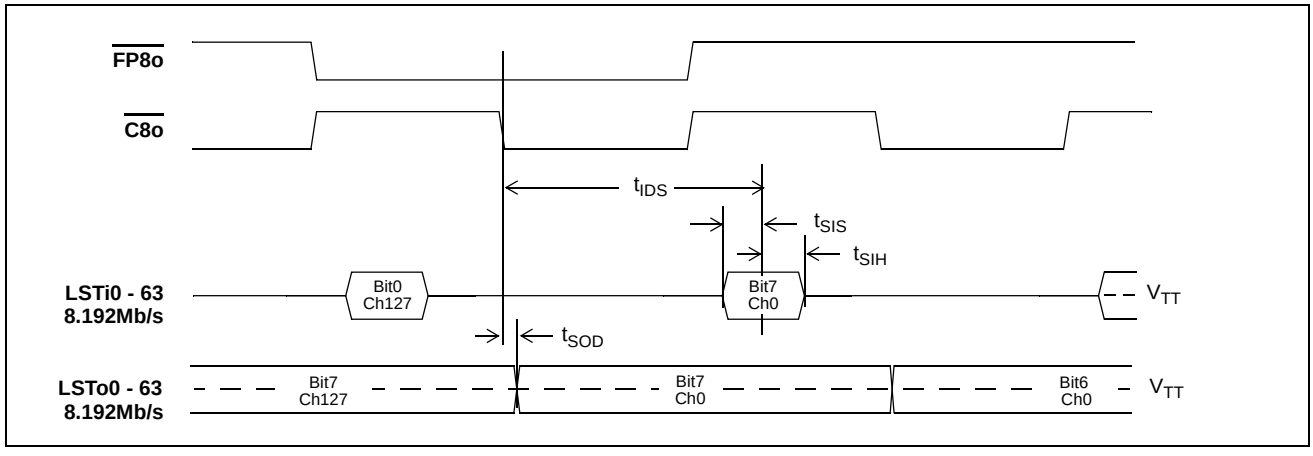


Figure 21 - Local Data Timing Diagram

AC Electrical Characteristics† - Backplane and Local Output HiZ Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	BSTo/LSTo delay - Active to High-Z - High-Z to Active	t_{DZ}, t_{ZD}			30	ns	R_L=1K, C_L=30pF, See Note 1
2	Output Driver Enable (ODE) Delay	t_{ODE}		13	25	ns	R_L=1K, C_L=30pF, See Note 1

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.
Note 1: High Impedance is measured by pulling to the appropriate rail with RL, with timing corrected to cancel time taken to discharge C_L.

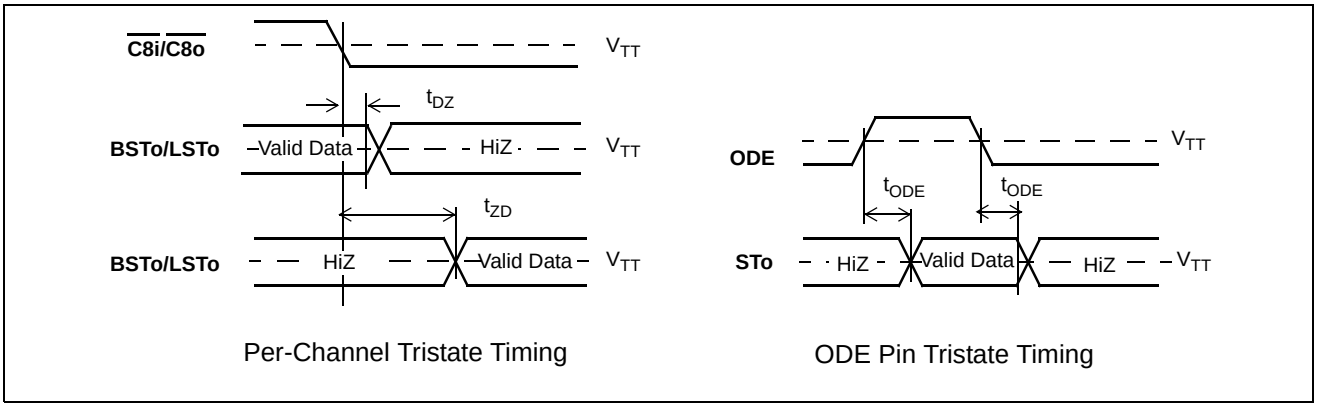


Figure 22 - Per-Channel and ODE Tristate Control Timing Diagrams

AC Electrical Characteristics† - Non-Multiplexed Microprocessor Port Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from DS falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from DS falling	t_{RWS}	15			ns	
3	Address setup from DS falling	t_{ADS}	5			ns	
4	$\overline{CS}$ hold after DS rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS rising	t_{RWH}	5			ns	
6	Address hold after DS rising	t_{ADH}	5	10		ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	4			ns	C_L=30pF
8	Data hold on read	t_{DHR}			10	ns	C_L=30pF, R_L=1K Note 1
9	Valid write data setup	t_{WDS}	25			ns	
10	Data hold on write	t_{DHW}	8			ns	
11	Acknowledgment Delay	t_{AKD}		65	70	ns	C_L=30pF
12	Acknowledgment Hold Time	t_{AKH}		14	20	ns	C_L=30pF, R_L=1K, Note 1

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, V_{DD_CORE} at 1.8V and V_{DD_IO} at 3.3V and are for design aid only: not guaranteed and not subject to production testing.

Note 1: High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

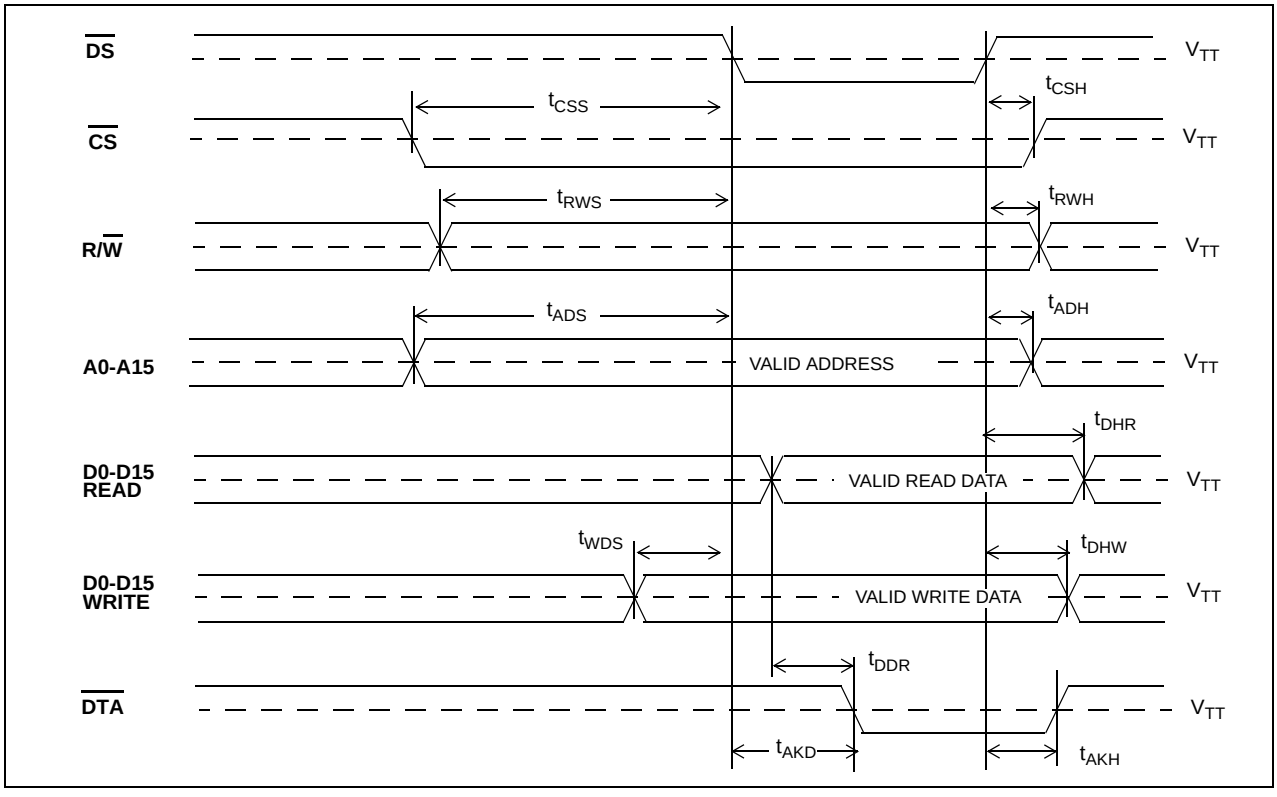


Figure 23 - Motorola Non-Multiplexed Bus Timing

AC Electrical Characteristics† - JTAG Test Port and $\overline{\text{Reset}}$ Pin Timing

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	200			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	80			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	80			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	90			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L=30pF
9	$\overline{\text{TRST}}$ pulse width	t_{TRSTW}	200			ns	C_L=30pF
10	$\overline{\text{Reset}}$ pulse width	t_{RSTW}	500			ns	C_L=30pF

† Characteristics are over recommended operating conditions unless otherwise stated.

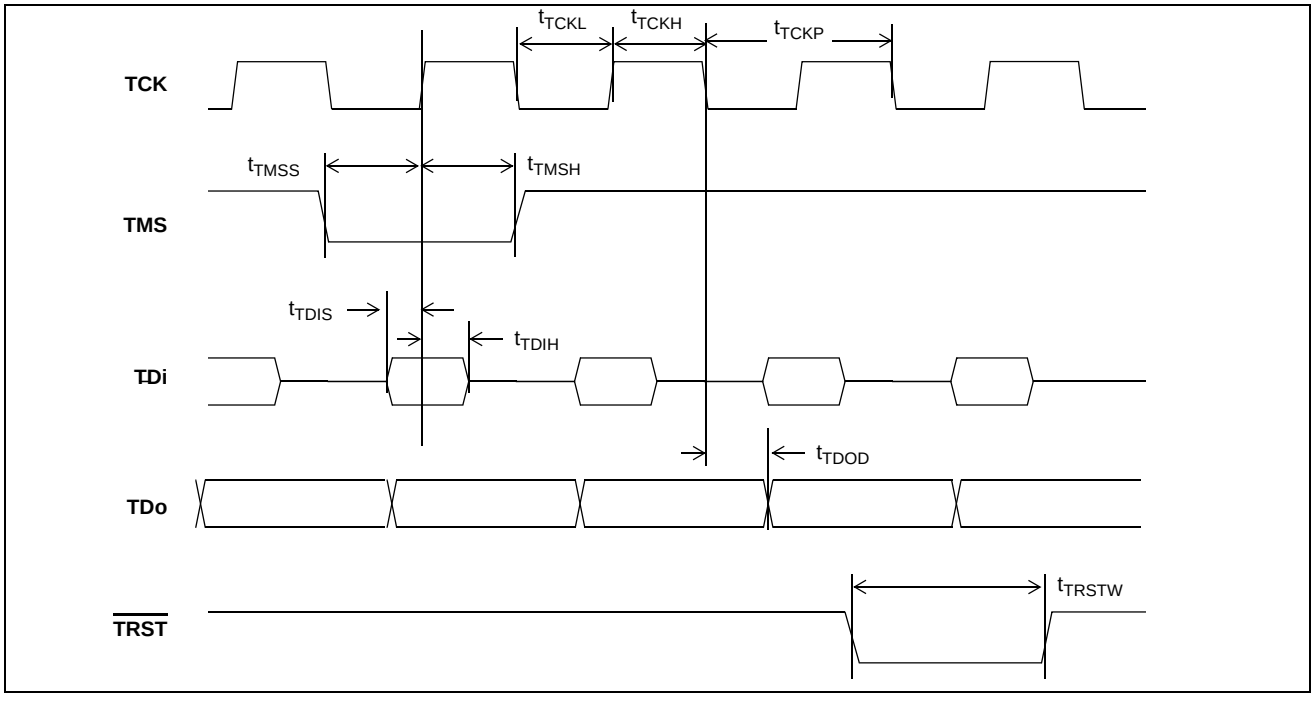


Figure 24 - JTAG Test Port Timing Diagram

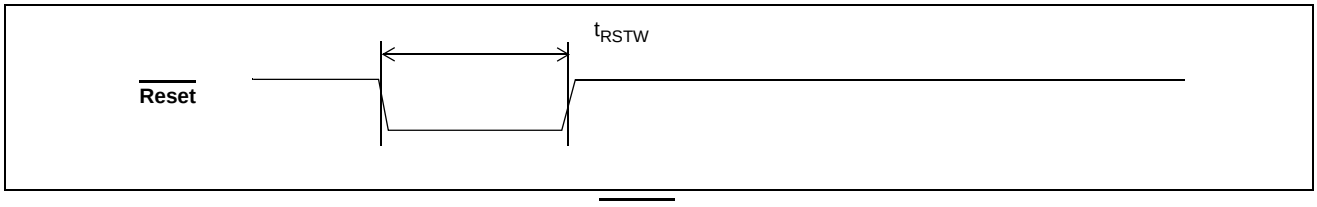


Figure 25 - $\overline{\text{Reset}}$ Pin Timing Diagram

APPENDIX - Bit Interleaving Mode

The bit interleaving mode performs the bit grooming function for the backplane input and output streams which have data rate of 32Mb/s. This mode is enabled by setting the bit interleaving mode enable (BIME) pin to one. The bit shuffling is performed for every four-channel as indicated in Figure 26. The input delay and the output advancement shown in Figure 26 are realized by programming the backplane input delay registers (LIDR0 to LIDR21) and the backplane output advancement registers (BOAR0 to BOAR7) as described in Table 11 & 12 and Table 20 respectively.

When the bit interleaving mode is selected for the backplane port, the delay between the frame pulse signals is six 32Mb/s channels plus 10 cycles of C8i. See Figure 27 for the frame pulse offset timing in the bit interleaving mode.

When the device is in the bit interleaving mode, the bit error rate test feature is not available for the backplane port BSTi0 -

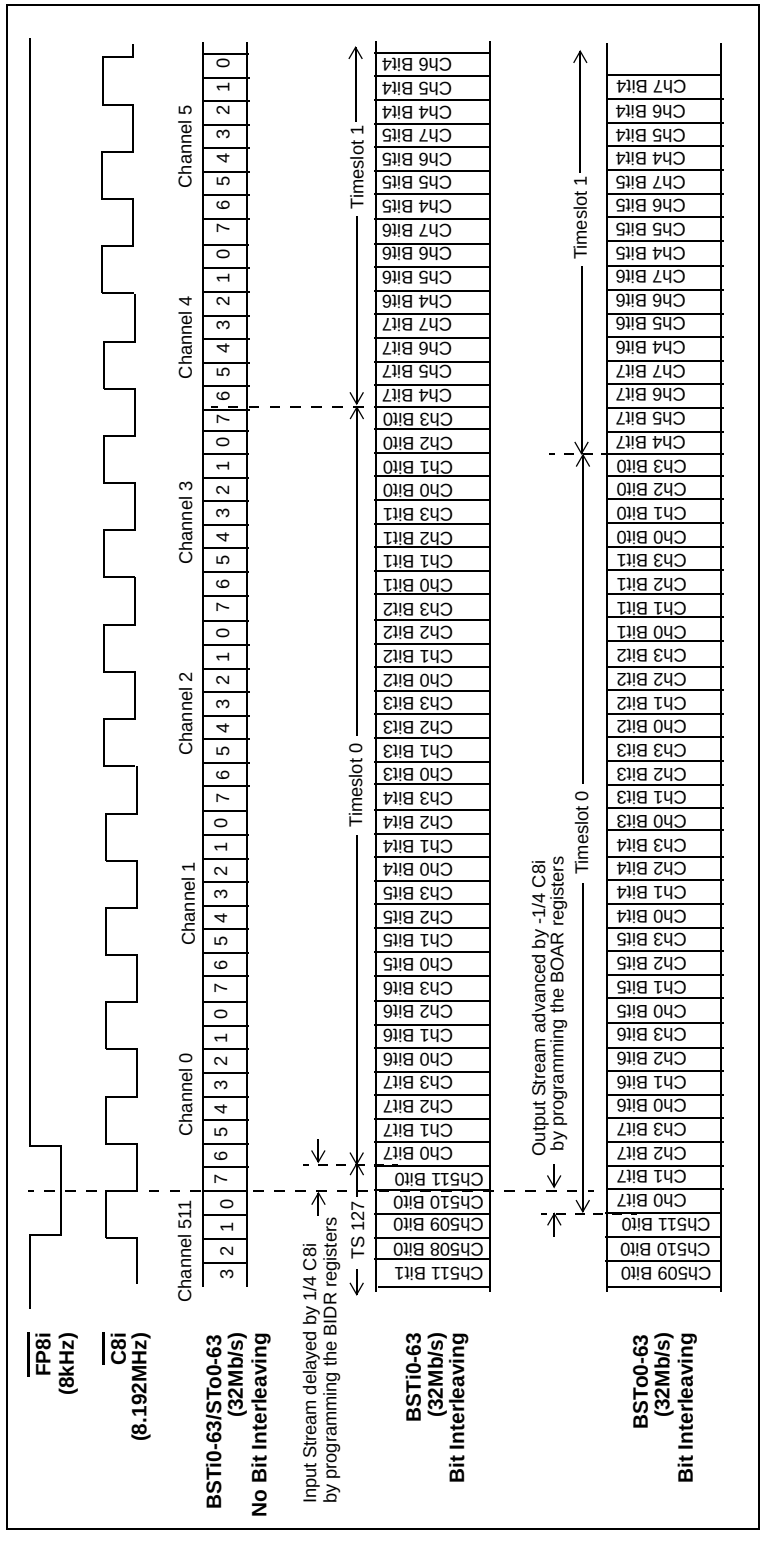


Figure 26 - Bit Interleaving Mode Timing Diagram for Backplane Input and Output Streams

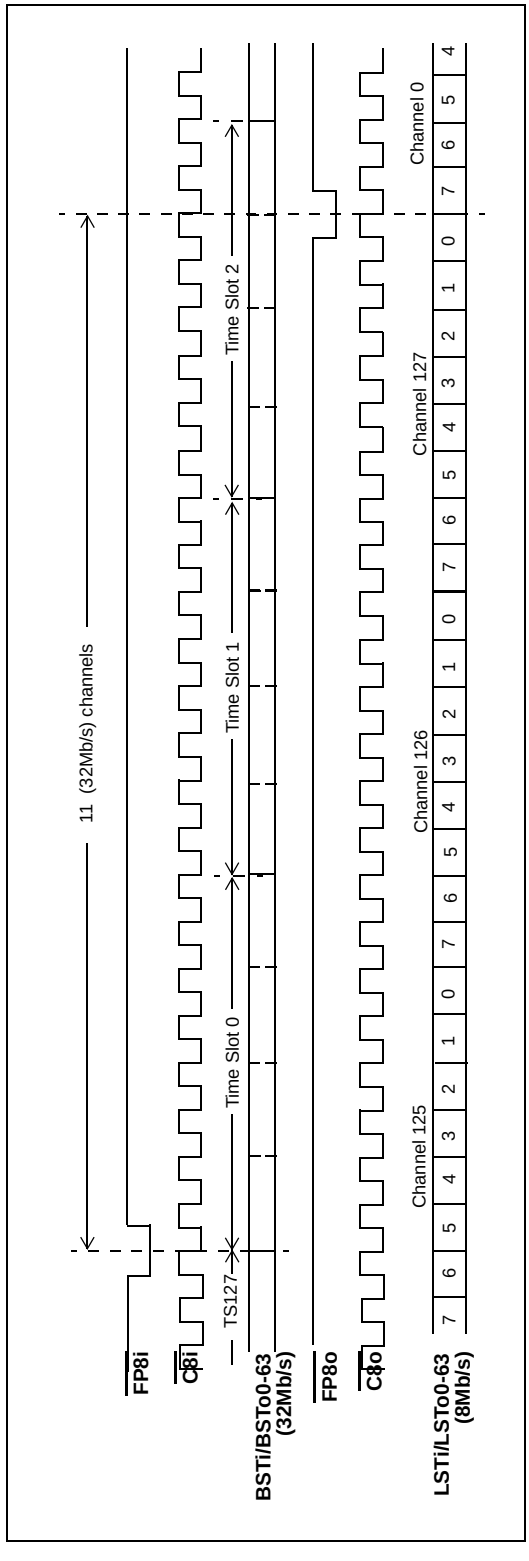
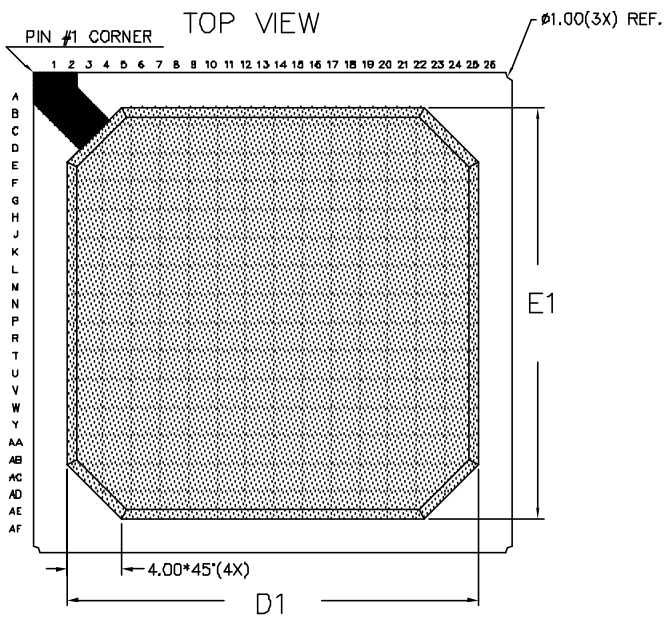
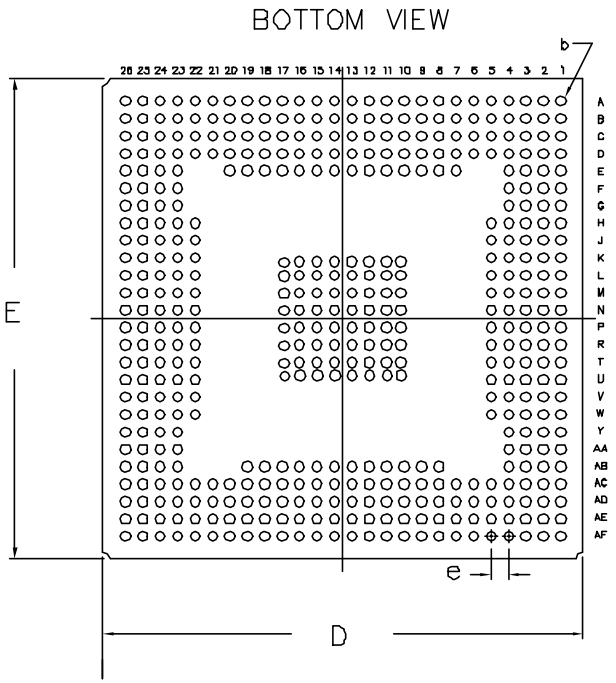
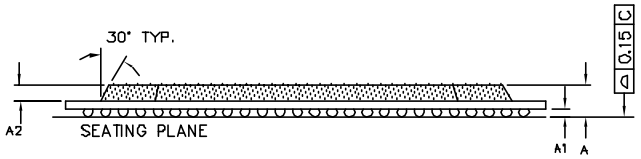


Figure 27 - Backplane and Local Frame Pulse Alignment Diagram for the Bit Interleaving Mode





DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	34.80	35.20
D1	30.00 REF	
E	34.80	35.20
E1	30.00 REF	
b	0.60	0.90
e	1.27	
N	466	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM.

ISSUE	1	2		
ACN	213806	213918		
DATE	25Nov02	13Jan03		
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