ZARLINK
SEMICONDUCTOR

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Features

- 12-channel integrated transimpedance and limiting amplifier operates up to 6.25 Gb/s

- 12 uA$_{PP}$ receiver sensitivity for 10^{-12} BER at 6.25 Gb/s

- Single +3.3V supply dissipating 140 mW per channel

- Selectable analog multiplexer provides junction temperature, supply voltage, and received signal strength for each channel

- Individual channel signal detect compares input signal strength with adjustable threshold

- Squelch automatically disables output when input signal strength falls below programmable threshold

- 2-wire interface provides access to internal registers

- CML output with selectable pre-emphasis and output amplitude control

- 250-micron channel pitch matches optical ribbon fiber and photodiode arrays

- IC dimensions 2245 x 3870 um

- Same form, fit, and function as the ZL62039 with opposite differential data polarity

Applications

- Double data rate (DDR) XAUI

- Double data rate (DDR) Infiniband®

- PCI Express

- SNAP12 optical modules

- Proprietary and CWDM parallel optical modules

- Proprietary 12-lane intra-system parallel optics

Description

The growing use of the Internet has created increasingly higher demand for multi-Gb/s I/O performance. The demand for 40 Gb/s bandwidth and beyond fuels the growth of short-reach 10 Gb/s infrastructures within high-end telco and datacom routers, switches, servers and other proprietary chassis-to-chassis links.

The transimpedance amplifier achieves a nominal 5 GHz bandwidth over a wide range of photodiode input capacitance. Excellent channel-to-channel isolation ensures data integrity at the receiver sensitivity limits. An internal circuit provides the photodiode reverse bias voltage supply and senses average photocurrent supplied to the photodiode array.

The transimpedance amplifier is AC-coupled internally to a high-gain, high-bandwidth, differential, limiting amplifier. The limiting amplifier provides a differential back-terminated CML output that can be used to drive 6.25 Gb/s per channel transceivers or other CML compatible clock and data recovery circuits. The CML output provides selectable pre-emphasis control to improve signal quality. The limiting amplifier features a circuit that senses optical modulation amplitude (OMA) to determine a loss of signal.

A selectable analog multiplexer provides junction temperature, supply voltage, and received signal strength for each channel to enable optical module diagnostic features.

Data controlling the Zarlink ZL62089 is loaded by a simple 2-wire serial serial interface reducing the number of pins required of a microcontroller.
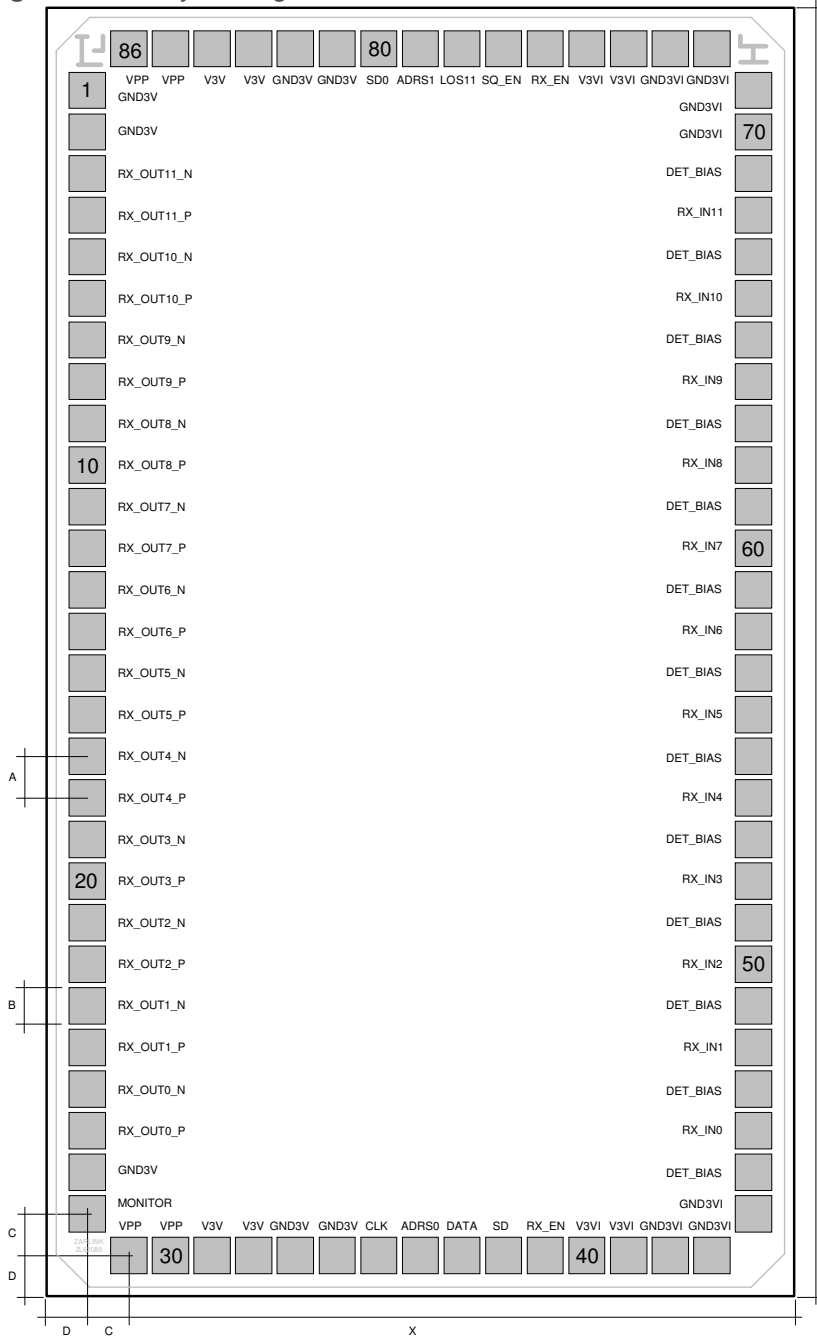
Figure 1: Pad layout diagram

Table 1: Critical dimensions

Symbol	Description	Length	Unit
A	Pad to pad pitch	125	um
B	Bond pad length/width	114	um
C	Corner pad to corner pad pitch	125	um
D	Pad center to edge of die	122.5	um
X	Overall IC dimensions	2245 +/-25	um
Y	Overall IC dimensions	3870 +/-25	um
Z	Standard die thickness	17	mils

Zarlink Semiconductor Inc.

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