ZL70271/72/73/74/88

Medical Surge Protection Device

Data Sheet

September 2008

Features

- Extremely fast turn-on
- Very small size and very low leakage
- 5, 6 and 7 terminals available
- Standard delivery form: solder bumped die
- Variant for wire bonding: ZL70288
- Facilitates compliance with EN-45502 and EN-50061
- Superior Quality
  - QA procedures based on MIL-PRF-38535
  - Traceability for every chip to lot and wafer number
  - 100% burn-in capability
  - **L**ot **A**cceptance **T**esting (**LAT**) Included

Ordering Information

ZL70271UDJ	Bumped Die, Waffle Tray
ZL70272UDJ	Bumped Die, Waffle Tray
ZL70273UDJ	Bumped Die, Waffle Tray
ZL70274UDJ	Bumped Die, Waffle Tray
ZL70288UBJ	Wirebondable Die, Waffle Tray

0°C to +55°C

Applications

- Pacemakers, Implantable Cardioverter Defibrillators (ICDs), Neurostimulators, Bladder Control Devices
- Medical devices with electronics requiring protection against a high voltage surge

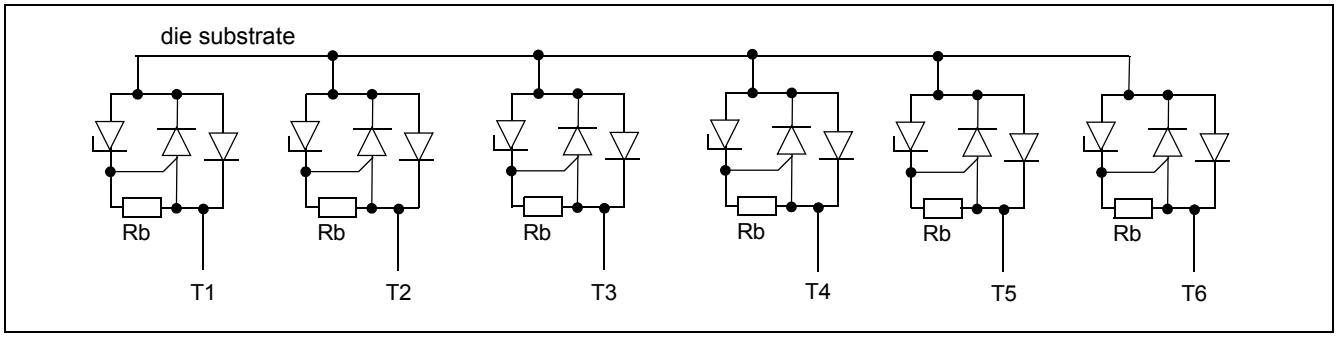

Figure 1 - ZL70273 Block Diagram

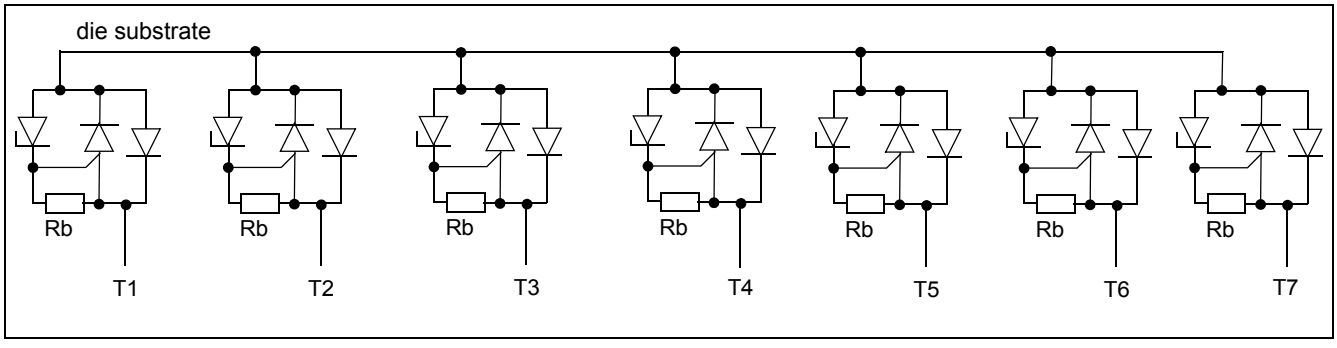

Figure 2 - ZL70274 and ZL70288 Block Diagram

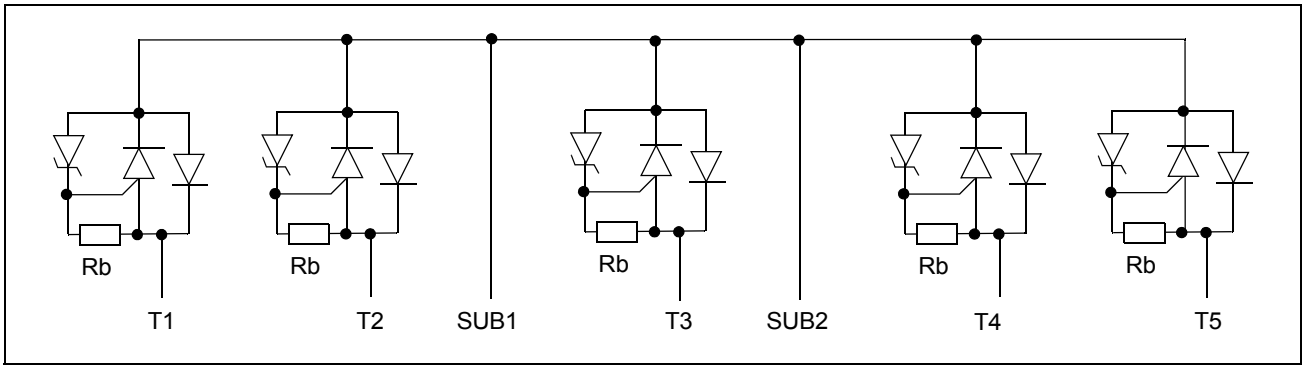

Figure 3 - ZL70271 and ZL70272 Block Diagram

1.0 Change Summary

Changes from May 2008 Issue to July 2008 Issue.

Page	Item	Change
15	Figure 12	Corrected dimensions and tolerances.
17	Figure 16	Corrected dimensions and tolerances.

Changes from July 2008 Issue to September 2008 Issue.

Page	Item	Change
1	Ordering Information	Removed ZL70270UDJ from ordering. Part has been obsoleted.

2.0 Description

The ZL70271/72/73/74/88 is a family of transient surge suppressing devices designed specifically for implanted medical devices. The device terminals exhibit extremely low leakage during normal voltages and can therefore be connected in parallel with the pins of the device they protect. When the voltage rises to dangerous level it then rapidly turns on and limits the voltage by shunting the current thr7ough its thyristors. This makes the ZL70271/72/73/74/88 family an effective means of compliance with international regulations EN-45502, “Active implantable” and EN-50061, “Safety of Implantable Cardiac Pacemakers”.

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3.0 Applications

The EN-45502 standard states that all active medical devices implanted in a human torso should not be permanently affected by an external defibrillation of the patient. Compliance is confirmed if the implanted device continues to meet device specification after being subjected to a sequence of 140 Volt pulses, in series with a 300 Ohm resistor between each conductive part of the device, including the device case (see EN-45502 for details). The ZL70271/72/73/74/88 family meets this test and is an effective means of complying with the EN-45502 standard. Without surge protection, the electronics, in almost all cases would be destroyed. The same compliance tests are also described in EN-50061.

In the application example shown in Figure 4, each of the dual chamber pacemaker's terminals, and the case, are connected to a terminal on the protection device. If a defibrillation pulse causes the ventricular tip to begin to go positive, relative to the case, the ZL70271 thyristor structure rapidly becomes active and forms a low impedance path between T2 and T3 to absorb the current and limit the voltage. This provides an effective means of protecting the pacemaker chip. The voltages and currents the implanted device is subjected to in an actual defibrillation can be higher than described in EN-45502/EN-50061 and has been taken into account in the design of the ZL70271/72/73/74/88 family.

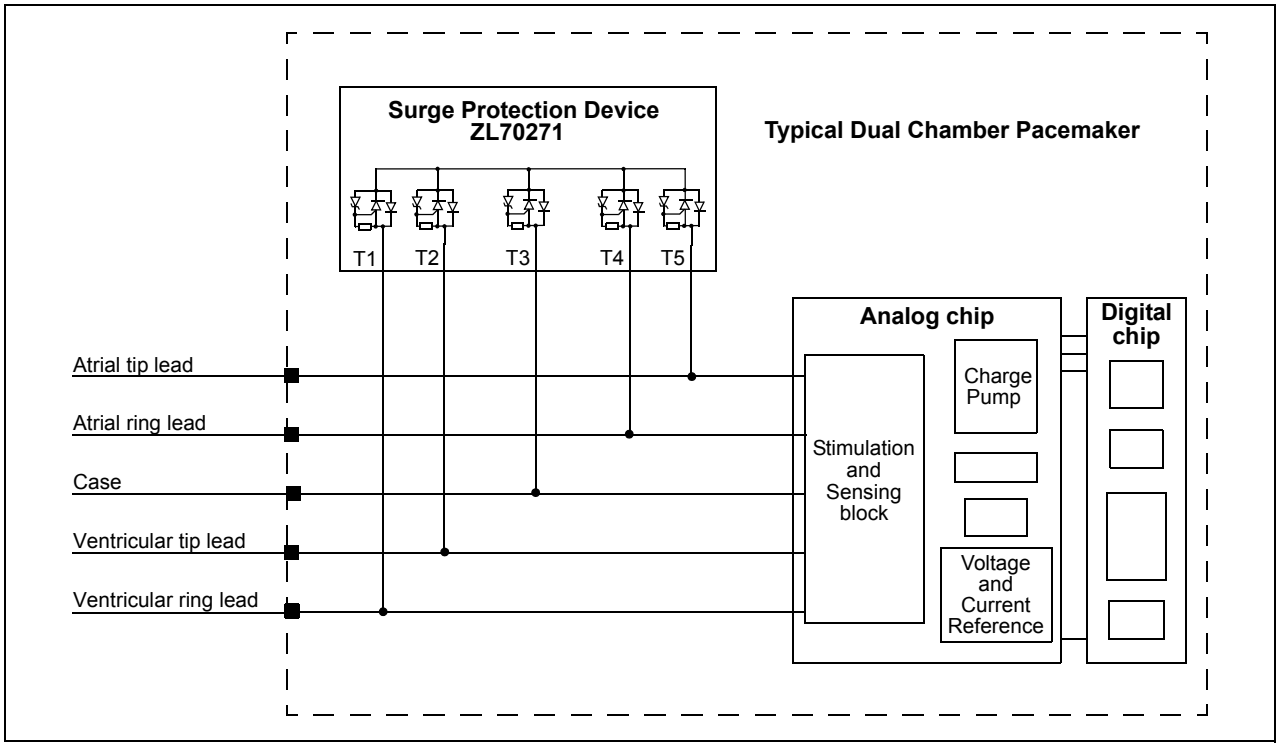


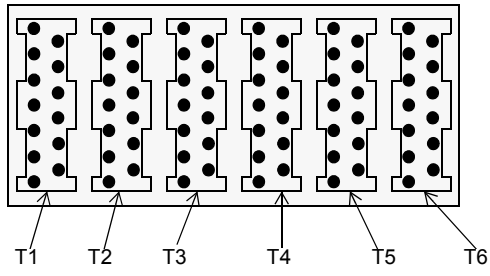
Figure 4 - Pacemaker Application Example

Terminals placed most remotely to others must get special attention since they effectively form a large pick-up coil and could therefore be exposed to a large amount of current. When implanted, the pacemaker case is placed beneath the collarbone and all other terminals are placed together inside the heart. For this reason, the largest current will pass through the surge protection terminal connected to the case of the pacemaker. For ZL70271/72, it is recommended that the case be connected to T3 of the protection device; this terminal is designed to withstand the largest amount of current. If the ZL70273/74/88 device is used in a 5 terminal application, we recommend that 2/3/3 pins of the protection device are connected to the implantable device terminal with the largest current flow (typically the terminal for the device case).

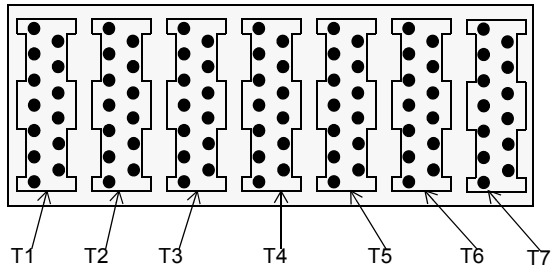
Pin Description Table - ZL70273, ZL70274 and ZL70288

Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I	T3	Transient Surge Protection Terminal 3
4	I	T4	Transient Surge Protection Terminal 4
5	I	T5	Transient Surge Protection Terminal 5
6	I	T6	Transient Surge Protection Terminal 6
7	I	T7	Transient Surge Protection Terminal 7 (ZL70274 and ZL70288 only)

ZL70273



ZL70274



ZL70288

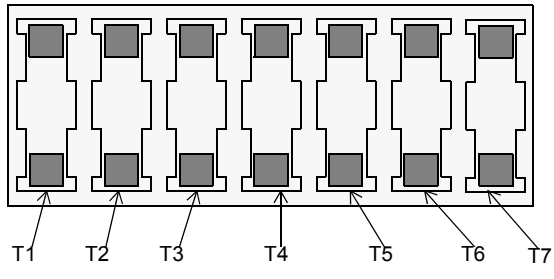


Figure 5 - ZL70273 and ZL70274 Bumped Chip Appearance and ZL70288 Bond Pad Placement

Pin Description Table - ZL70271 and ZL70272

Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I/O	SUB1	Transient Surge Protection Substrate Connection 1
4	I	T3	Transient Surge Protection Terminal 3 Doubled Area
5	I/O	SUB2	Transient Surge Protection Substrate Connection 2
6	I	T4	Transient Surge Protection Terminal 4
7	I	T5	Transient Surge Protection Terminal 5

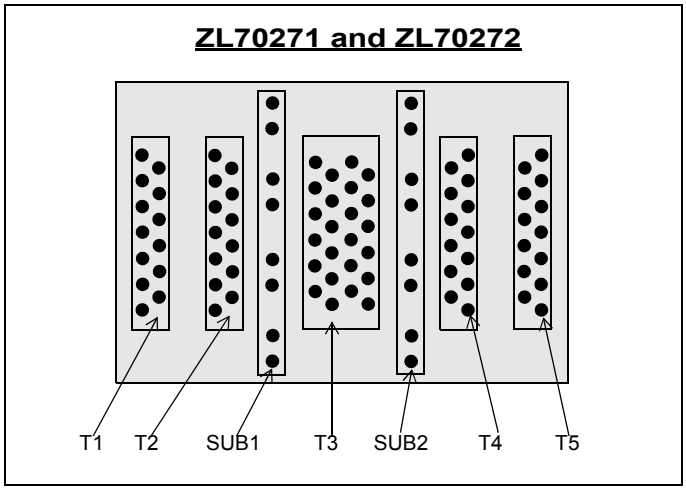


Figure 6 - ZL70270, ZL70271 and ZL70272 Bumped Chip Appearance

4.0 Functional Description

4.1 ZL70273

The ZL70273 is a six-branch device. The suppression is achieved by a self-triggering thyristor-diode device in parallel with a diode between each branch-input and a common node which is also the substrate of the device. The six branches of the device are reached through terminals T1, T2, T3, T4, T5 and T6. The electrical characteristic observed between any two of the terminals (T1, T2, T3, T4, T5 and T6) very much resembles that of a DIAC (see Figure 8).

When a transient current is forced between two branch-input terminals, the positive terminal will be clamped to the common node by the diode of one branch, and the negative terminal to the forward voltage of the thyristor-diode of the other branch. Due to the low on-state voltage of the thyristor that voltage will stay at a safe value during the transient.

4.2 ZL70274 and ZL70288

The ZL70274 and ZL70288 are seven-branch devices with exactly the same electrical characteristics as ZL70273.

4.3 ZL70271 and ZL70272

The ZL70271 and ZL70272 are five-branch transient surge suppressing devices with the same functionality as ZL70273. The only functional difference is that the substrate of the device is accessible through the two terminals SUB1 and SUB2.

5.0 Electrical Data

Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Max.	Units	Test Conditions
1	Storage Temperature range	T_S	-40	125	°C	
2	Maximum junction temperature	T_j		125	°C	
3	Maximum surge current	ITSM		8	A	Test according to Figure 7. tp for flip mounted chips with underfill: 10 ms. tp die wire bonded die: 1ms.
4	Continuous power dissipation	Pmax		300	mW	t>1 s

* Exceeding these values may cause permanent damage. Functional operations under these conditions is not implemented.

Recommended Operating Conditions

	Parameter	Sym.	Min.	Typ.[1]	Max.	Units	Test Conditions
5	Operating temperature range	T_{OP}	0	37	55	°C	

Note 1: Typical figures are at 37°C and are for design only.

DC Electrical Characteristics @ +37°C

	Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
6	Forward breakdown voltage, Zener diode, terminal to terminal						Iz=10 μA
	ZL70273/74/88	Vfz	9.0	10.1	11.0	V	
	ZL70271	Vfz	9.0	9.5	12.2	V	
	ZL70272	Vfz	17.0	18.0	19.5	V	
7	Forward breakdown voltage, Zener diode, terminal to substrate						Iz=10 μA
	ZL70271	Vfz	8.5	9.2	11.5	V	
	ZL70272	Vfz	16.5	17.7	19.0	V	
8	Breakover voltage, terminal to terminal						Figure 8
	ZL70273/74/88	Vbo	9.0	11.2	12.0	V	
	ZL70271	Vbo	9.0	10.5	12.2	V	
	ZL70272	Vbo	17.0	18.7	19.5	V	
9	Breakover voltage, terminal to substrate						Figure 8
	ZL70271	Vbo	8.5	9.8	11.5	V	
	ZL70272	Vbo	16.5	18.4	19.0	V	
10	Forward diode voltage drop, substrate to terminal						Measured @2A
	ZL70271/72	Vfwd			2	V	
11	Breakover current						Figure 8
	ZL70273/74/88	Ibo		15	200	mA	
	ZL70271	Ibo		15	40	mA	

DC Electrical Characteristics @ +37°C (continued)

	Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
	ZL70272	Ibo		15	40	mA	
12	Holding current	Ih	1			mA	Figure 9. Measured after a current pulse of Ip=0.2A for tp=1 ms, RG<200 Ω
13	On-state voltage terminal to terminal	Von		2.2	3.0	V	Measured with a 300 μs pulse, IT=1 A
14	On-state voltage terminal to substrate, ZL70271/72	Von		1.0	3.0	V	Measured with a 300 μs pulse, IT=1 A
15	On-state dynamic resistance						Measured with a 300 μs pulse, dIT=1-2 A
	ZL70271/73/74/88	Ron		0.4	1	Ω	
	ZL70272	Ron		0.3	1	Ω	
16	Off-state current, terminal to terminal						
	ZL70273/74/88	Id		10	100	nA	Measured at 8.0 V
	ZL70271/72	Id		10	150	nA	ZL70271 measured at +8.5 V ZL70272 measured at +16.5 V
	After Surge pulse	ΔId			20	nA	Force 3 current surge pulses, with max 10 s between each (I=3A, t=2 ms), between the Terminal under test and the rest of inputs (they should be tied together). If there are substrate connections, these should be left floating.
17	Off-state current terminal to substrate						
	ZL70271	Id		10	150	nA	ZL70271 measured at +8.0 V
	ZL70272	Id		10	150	nA	Measured at +16.0 V
18	Parasitic capacitance						
	ZL70273/74/88	Cp			50	pF	
19	Parasitic capacitance						
	ZL70271/72	Cp			200	pF	

AC Electrical Characteristics @ +37°C

	Parameter	Sym	Min	Typ	Max	Units	Test Conditions
20	Turn-on delay						Defined according to Figure 10.
	ZL70273/74/88	tond		500	13000	ns	Measured at 8.0 V
	ZL70271	tond		140	4000	ns	Measured at 8.0 V terminal to terminal and at 7.5 V terminal to substrate
	ZL70272	tond			6000	ns	Measured at 16 V terminal to terminal and at 15.5 V terminal to substrate
21	Maximum voltage during surge						Measured at peak and defined according to Figure 10.
	ZL7073/74/88	Vpeak		13	15	V	
	ZL70271	Vpeak		11.5	13	V	
	ZL70272	Vpeak			21.5	V	
22	Immunity to dV/dt triggering						Defined according to Figure 10.
	ZL70073/74/88	dV/dt	1000	>2300		V/us	Measured at 8.0 V
	ZL70271	dV/dt	100	160		V/us	Measured at 9 V terminal to terminal and at 8.5 V terminal to substrate
	ZL70272	dV/dt	100			V/us	Measured at 17 V terminal to terminal and at 16.5 V terminal to substrate

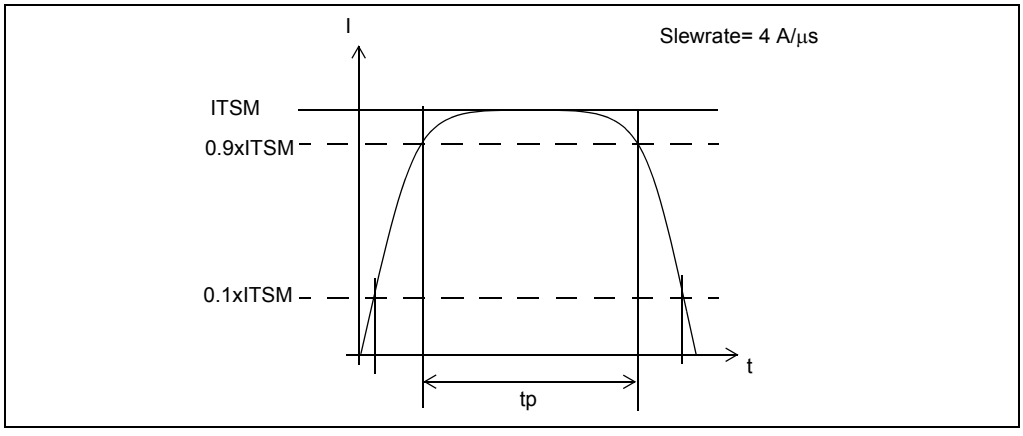


Figure 7 - 10 ms Surge Current Waveform

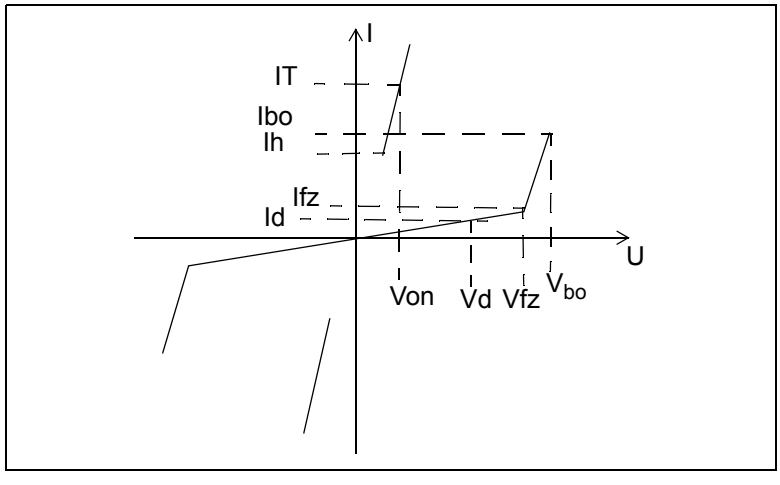


Figure 8 - Terminal to Terminal Characteristic

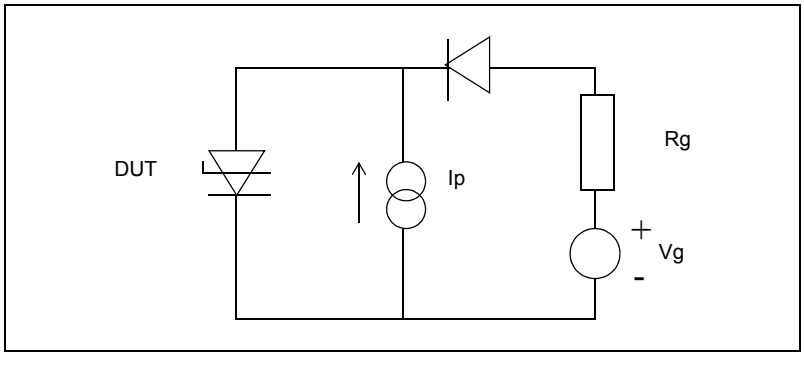


Figure 9 - Holding Current Circuit

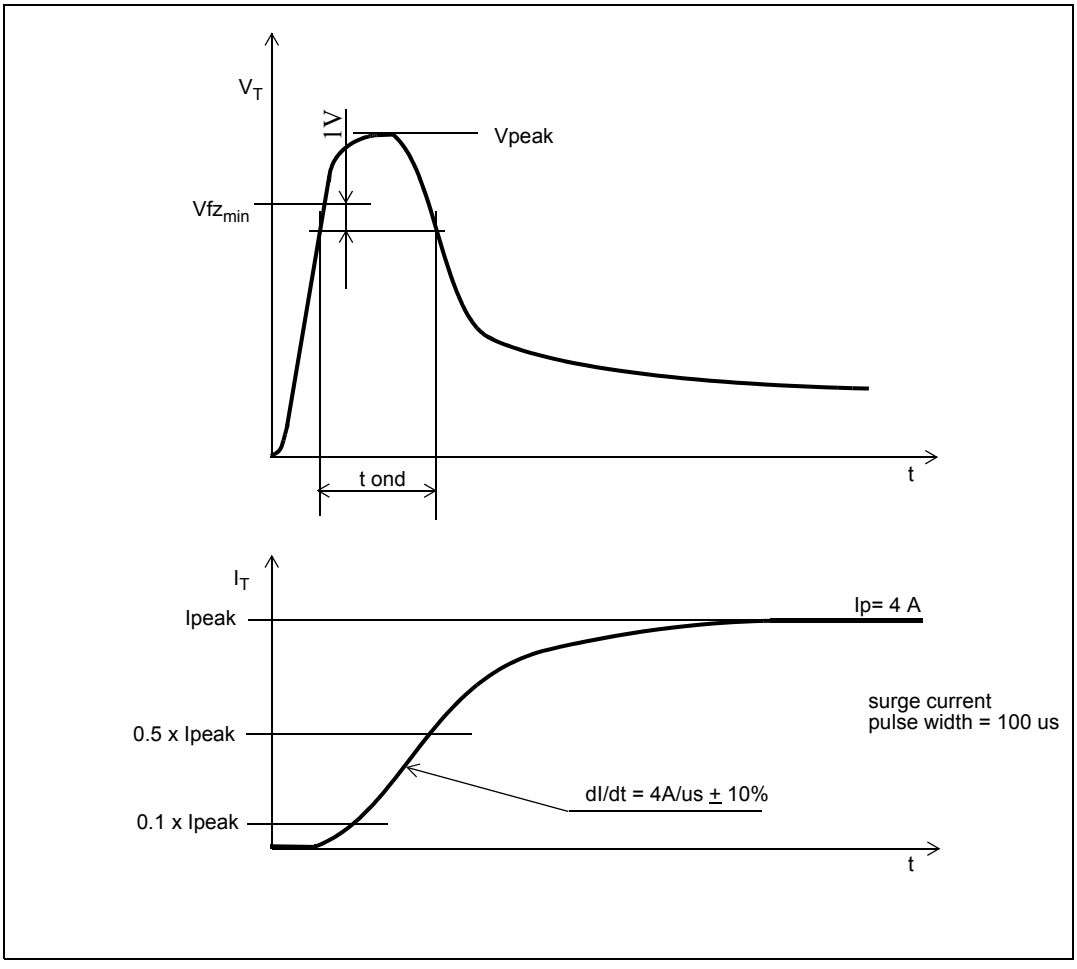


Figure 10 - Turn-on Delay Definition

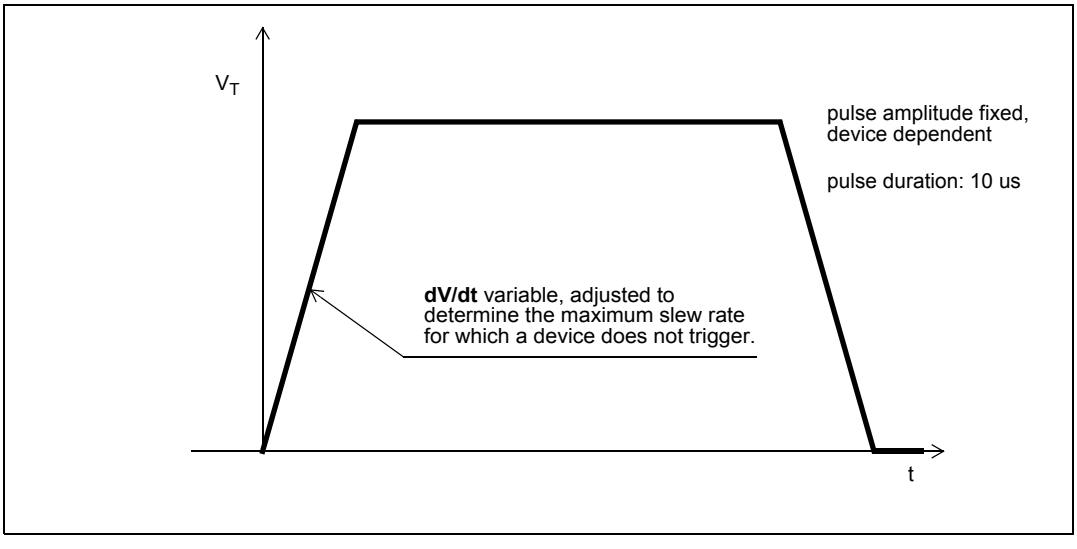


Figure 11 - dV/dt Immunity Test Pulse

6.0 Quality Assurance Procedures

Zarlink's QA procedures are based on MIL-PRF-38535. Zarlink maintains traceability records for every chip to the wafer lot and wafer level. Each wafer lot is subjected to a Lot Acceptance Test (LAT). The devices are assembled to a ceramic test substrate and subjected a 168-hour burn-in test at +125°C, or equivalent. Wafer lots acceptance requires all LAT devices must pass the pre- and post burn-in electrical tests. A certification of compliance (C of C) is included with each shipment.

Additional details/information are available upon request from Zarlink.

7.0 Additional Information

7.1 Evaluation Boards

For bench evaluation purposes, Zarlink offers the surge protection devices mounted on ceramic substrate. Each surge protection device terminal and substrate terminal (if present) is accessible by two through hole solder pins attached to either side of the test substrate. Ordering information is listed in the table below. Evaluation boards are for testing and evaluation purposes only and are not for use in implanted devices.

Evaluation Board, Cross-Reference

Surge Protection Device Part Number	Evaluation Board Part Number	Evaluation Board Description
ZL70271UDJ	ZLE70271MAD	Eval Board, Surge Protection, ZL70271
ZL70272UDJ	ZLE70272MAD	Eval Board, Surge Protection, ZL70272
ZL70273UDJ	ZLE70273MAD	Eval Board, Surge Protection, ZL70273
ZL70274UDJ	ZLE70274MAD	Eval Board, Surge Protection, ZL70274
ZL70288UBJ	ZLE70288MAD	Eval Board, Surge Protection, ZL70288

7.2 Flip Chip Processing Recommendations

The surge protection devices described in this document (with the exception of ZL70288) are designed for Flip Chip assembly. The face or active surface of the chip is covered with small tin/lead solder bumps designed to connect to solder pads on the surface of a circuit board via reflow soldering. For best results, an underfill should be added to fill in the gap between the die and circuit board to reduce thermal stresses imposed on the solder joint. Zarlink does not offer a recommended circuit board pad pattern for these devices. However, there are two approaches to consider when designing the circuit board pad pattern. One method is too layout a pattern of individual pads matched to each solder bump. A second method is to design a pattern of rectangular pads large enough to connect all of the pads for a single terminal. No matter the method used, all of the solder bumps associated with an individual terminal must be connected together via the circuit board (refer to Figure 5 & Figure 6). Likewise, in the case of ZL70271/72, all of the "Sub1" and Sub2" solder bumps must also be connected together (refer to Figure 6). If unfamiliar with flip chip processing, Zarlink recommends that the customer seek advice from a consultant or sub-contractor familiar with the process.

8.0 Mechanical Data

8.1 Mechanical Data - ZL70273

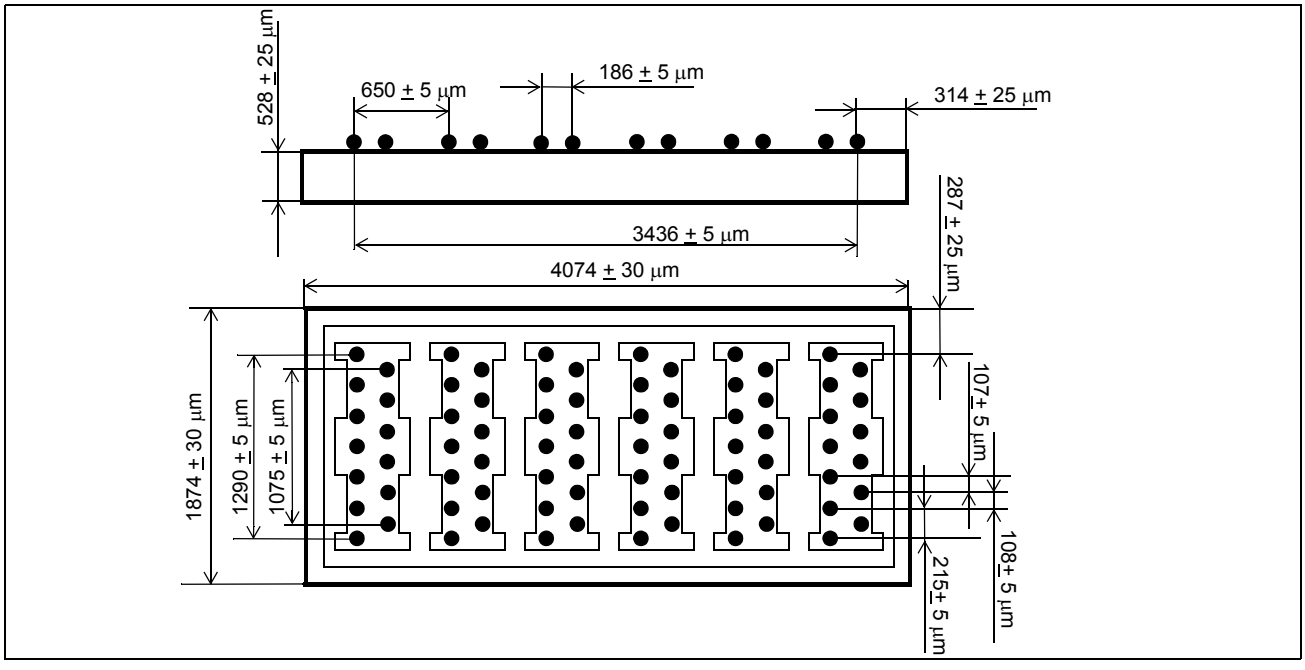


Figure 12 - Die Size and Bump Placement of ZL70273

8.2 Mechanical Data - ZL70274

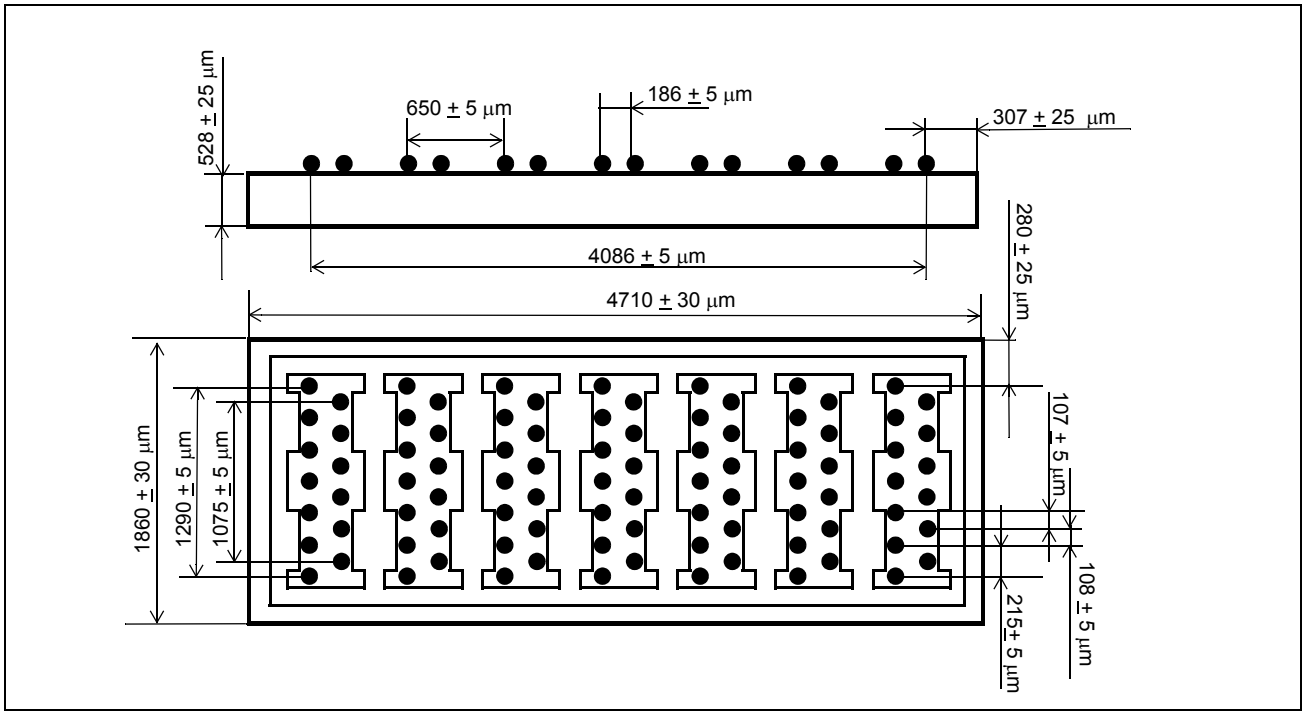


Figure 13 - Die Size and Bump Placement of ZL70274

8.3 Mechanical Data - ZL70271 and ZL70272

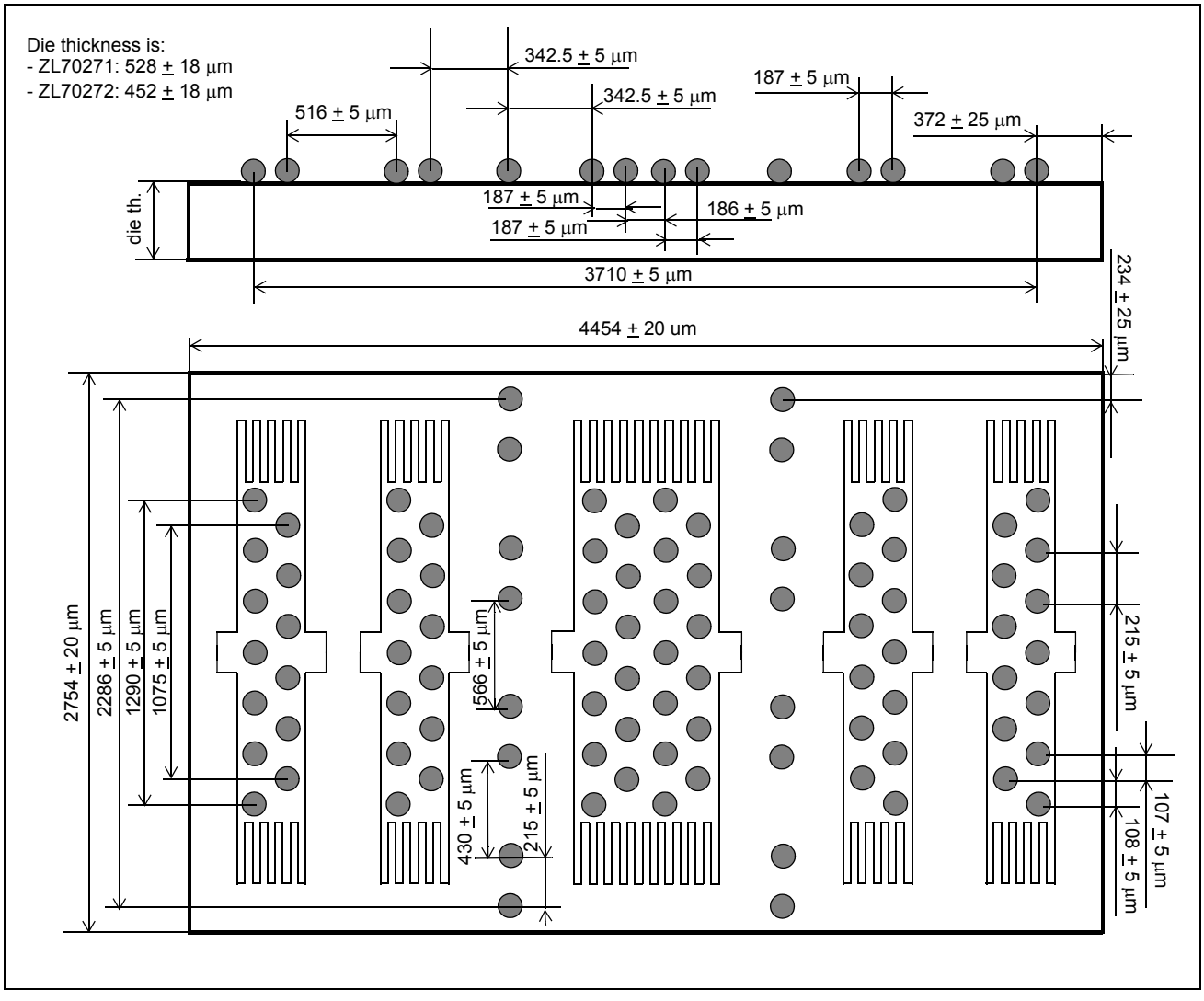


Figure 14 - Die Size and Bump Placement of ZL70271 and ZL70272

8.4 Mechanical Data - Solder bumps ZL70271/72/73/74

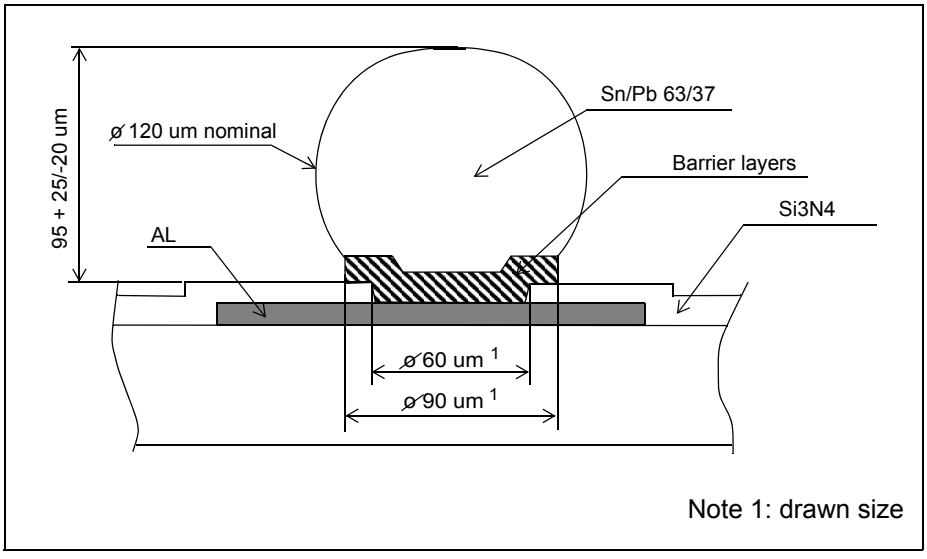


Figure 15 - Solder Bump Appearance of ZL70271/72/73/74

8.5 Mechanical Data - ZL70288

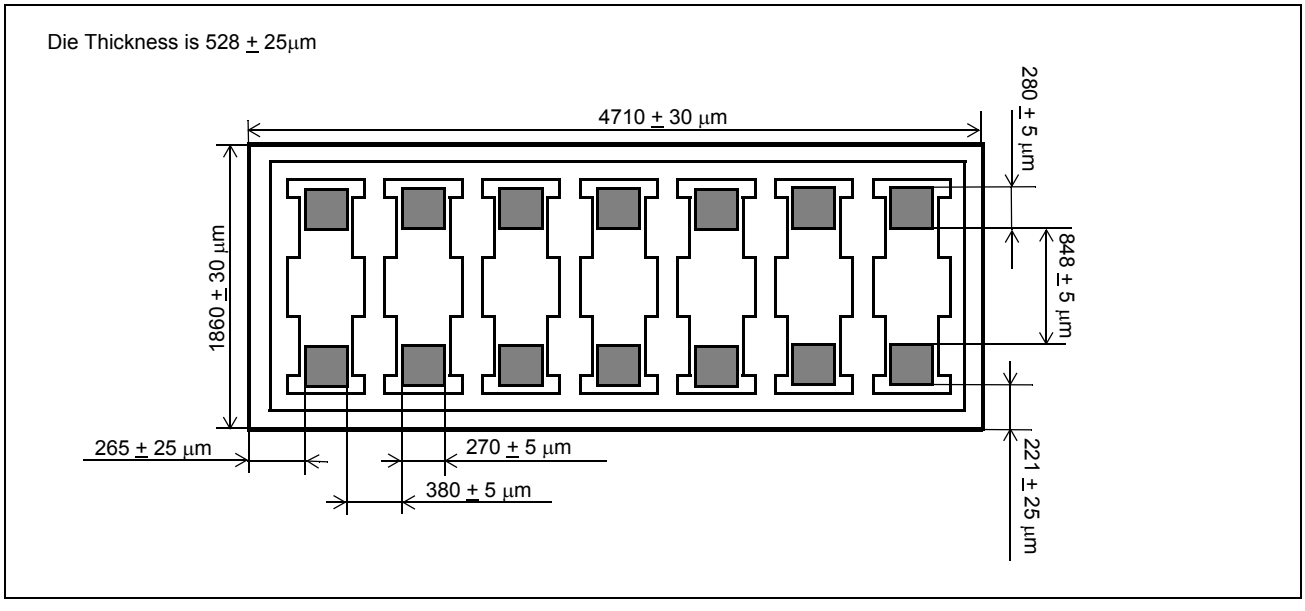


Figure 16 - Size and Bond Pad Placement of ZL70288

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www.zarlink.com