MT90528
28-Port Primary Rate Circuit Emulation AAL1 SAR
Data Sheet

August 2006

Features

- AAL1 Segmentation and Reassembly device compliant with Circuit Emulation Services (CES) standard (af-vtoa-0078.000)
- Supports both Unstructured and Structured Circuit Emulation of 28 independent DS1/E1/ST-BUS interfaces
- Supports AAL1 trunking, with up to 128 TDM channels per VC (af-vtoa-0089.001)
- Supports CAS transmission and reception in all structured modes of operation
- Supports simultaneous processing of up to 896 bidirectional Virtual Circuits
- Supports mixed DS1/E1 operation
- Supports mixed Unstructured and Structured CES operation
- Fully flexible DS0 assignment
- Complete clock recovery solution provided on-chip: Synchronous, Adaptive, or Synchronous Residual Time Stamp (SRTS) via 28 independent PLLs

Ordering Information

MT90528AG	456 PBGA	Trays
MT90528AG2	456 PBGA**	Trays

**Pb Free Tin/Silver/Copper

-40 to +85°C

- Dual-mode (ATM-end or PHY-end) UTOPIA port operates in Level 1 or Level 2 mode for connection to external PHY or ATM devices with UTOPIA clock rate up to 52 MHz
- TDM bus provides 28 bidirectional serial streams at 1.544, 2.048, or 4.096 MHz - compatible with Generic (1.544 Mbps or 2.048 Mbps) and ST-BUS (2.048 Mbps) interfaces
- Supports master and slave TDM backplane bus clock operation
- Supports TDM and UTOPIA loopback functions
- 16-bit microprocessor port, configurable to Motorola or Intel timing
- Master clock rate of 66.0 MHz

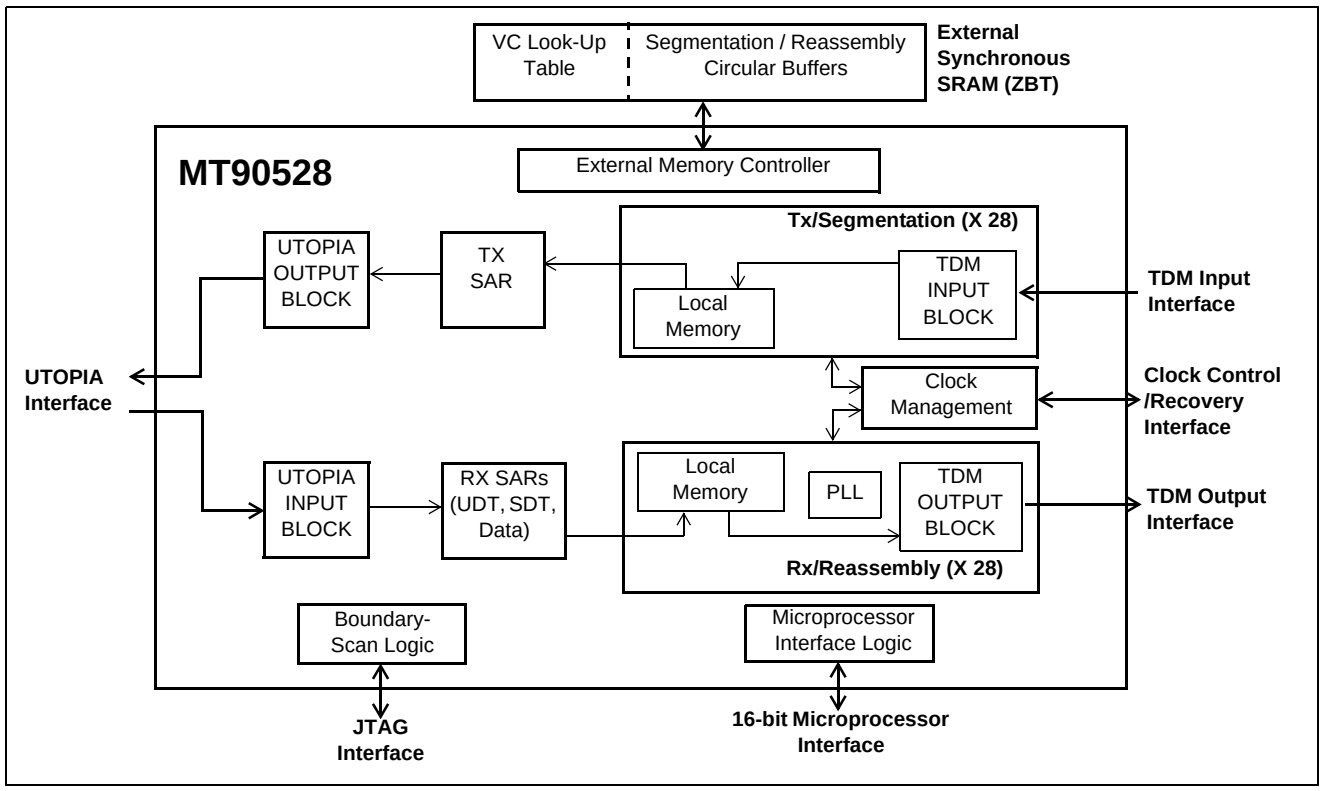


Figure 1 - MT90528 Block Diagram

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Applications

- B-ISDN (Broadband ISDN) systems requiring flexible N x 64 kbps transport
- Systems requiring af-vtoa-0078.000 (ATM Forum CES v2.0) “DS1 or E1 Nx64 Basic Service”, “DS1 or E1 Nx64 Service with CAS”, or “DS1 or E1 Unstructured Service” - flexible CES allows one-board solution to support multiple CES modes
- Systems requiring af-vtoa-0089.001 (ATM Forum - ATM Trunking Using AAL1 for Narrowband Services) - transport of up to 128 channels per VC
- Ideal for carrier-class WAN access products, especially channelized DS3 or E3 interfaces
- ATM Edge Switches
- Carrier Class Voice over ATM systems
- ATM Public Network access for PBX or CO
- TDM traffic transfer over an asynchronous cell bus

Description

The MT90528 28-Port Primary Rate Circuit Emulation AAL1 SAR allows primary rate TDM circuits to be carried over ATM networks using Circuit Emulation Services. Up to 896 bidirectional ATM VC connections can be simultaneously processed by the MT90528 CES AAL1 SAR device.

The MT90528 supports several modes of Circuit Emulation Services for DS1 and E1 rates. These include Unstructured CES and Structured CES with and without Channel Associated Signalling (CAS).

On the TDM bus side, the MT90528 interfaces with 28 primary rate TDM ports operating at 1.544 Mbps or 2.048 Mbps. The configurable TDM ports interface directly with DS1 or E1 framers for Nx64 Structured operation, or with DS1 or E1 LIUs in Unstructured mode.

On the ATM interface side, the MT90528 device meets the ATM Forum standard for UTOPIA Bus Level 2. The MT90528 is capable of operating as a UTOPIA “master” (ATM-end), “slave” (PHY-end), or “multi-PHY slave” (PHY-end). The UTOPIA port can operate in 8-bit or 16-bit mode, with a clock rate up to 52 MHz.

Each of the twenty-eight ports of the device contains a PLL, allowing independent timing of each TDM port. Each PLL supports four modes of clock recovery: SRTS, Adaptive, Synchronous (from the Physical layer), or from the TDM line clock. Although a complete clock recovery solution is provided internally, an optional external PLL or external clock source is also supported.

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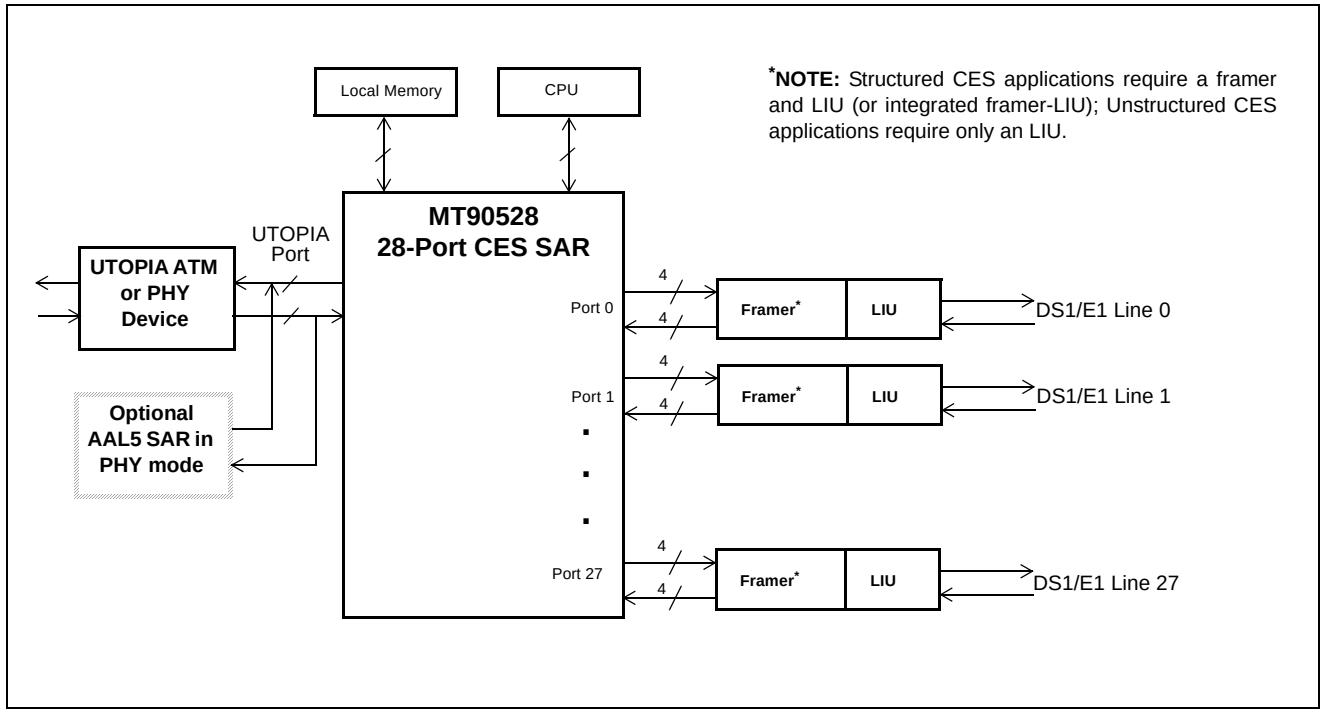


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1.0 Introduction

1.1 Functional Overview

The MT90528 28-Port Primary Rate Circuit Emulation AAL1 SAR (Segmentation and Reassembly) device is intended to carry twenty-eight primary rate TDM (Time Division Multiplexed) circuits (DS1 or E1) over an ATM (Asynchronous Transfer Mode) network using Circuit Emulation Services (CES). The MT90528 is ideally suited for channelized DS3/E3 (i.e., DS3/E3 accessed as multiple DS1/E1) bandwidth. At its interface to the TDM network, the MT90528 can be connected directly to a wide variety of industry-standard framers and LIUs (line interface units), or to a 2.048 Mbps ST-BUS TDM backplane. At its interface to the ATM network, the MT90528 supports a wide selection of UTOPIA-compliant Physical layer devices, and customer-specific ASICs which meet the UTOPIA (Level 1 or Level 2) specification.

The MT90528 provides several modes of Circuit Emulation Services in one device. The MT90528 implements CES for DS1 and E1 rates, as standardized in the ATM Forum CES standard (af-vtoa-0078.000 Version 2). The MT90528 supports both Unstructured and Structured circuit emulation of 28 independent TDM interfaces carrying DS1 or E1 traffic. In Unstructured CES mode, 28 VCCs (Virtual Circuit Connections) are supported. In Structured CES mode, flexible Nx64 kbps VCC assignment is supported, providing options ranging from a maximum of 896 VCCs carrying 64 kbps each (N = 1), to 28 VCCs carrying N = 32, to a smaller number of VCCs carrying up to N = 128. The MT90528 supports Structured CES with, or without, CAS (Channel Associated Signalling). MT90528 Management functions and statistics in accordance with the ATM Forum's CES MIB (Management Information Base) are supported.

On the TDM side, the MT90528 features twenty-eight primary rate TDM ports operating at 1.544 Mbps (Generic) or 2.048 Mbps (Generic or ST-BUS). The configurable TDM ports interface directly with DS1 or E1 framers for Nx64 Structured operation, as well as with DS1 or E1 LIUs (or M13 multiplexers) in Unstructured mode for reduced delay in the segmentation (ATM transmit) direction. The TDM interfaces are capable of operating with the line-rate bit clocks (1.544 MHz or 2.048 MHz), or with framed bus clocks at 1.544 MHz, 2.048 MHz or 4.096 MHz.

Each of the twenty-eight TDM ports contains a PLL (Phase Locked Loop), allowing independent timing of each TDM port. Alternatively in SDT mode, the MT90528 can be operated in backplane mode with a single timing source. Each independent PLL supports four modes of clock recovery: from SRTS time-stamps, from the cell-stream through the Adaptive Clock Method, from the Physical layer (synchronous method), or from the TDM interface line-rate. Although clock recovery is fully supported internally, an optional external PLL or clock source is also supported.

On the ATM interface side, the MT90528 device meets the ATM Forum standard UTOPIA Bus Level 2. The MT90528 is capable of operating as a UTOPIA "master" (ATM-end) or "slave" (PHY-end). ATM-end operation supports connection to a range of standard physical layer transceivers. PHY-end operation allows the MT90528 to be used in systems where pre-existing ASICs are available as "master" and require a "slave" device for interconnection. In PHY-end mode, the MT90528 is capable of Multi-PHY operation and has address inputs for this purpose. The UTOPIA port can operate in 8-bit or 16-bit mode, with a clock rate up to 52 MHz.

The MT90528 features a 16-bit microprocessor interface, capable of operating in Intel or Motorola mode, that is used to configure the device and monitor the management functions.

External memory (synchronous ZBT SRAM) is used in Structured CES operation to provide circular buffers in the segmentation direction and to provide CDV buffering in the reassembly direction. In addition, if the application's non-CBR data throughput (signalling or other) is low, the external memory can be used to provide a Receive Data Cell Buffer and a Transmit Data Cell Buffer for non-CBR data cells to be read or written, for processing by the external CPU. Unstructured CES operation requires no external memory (except where non-CBR data cell buffers are desired).

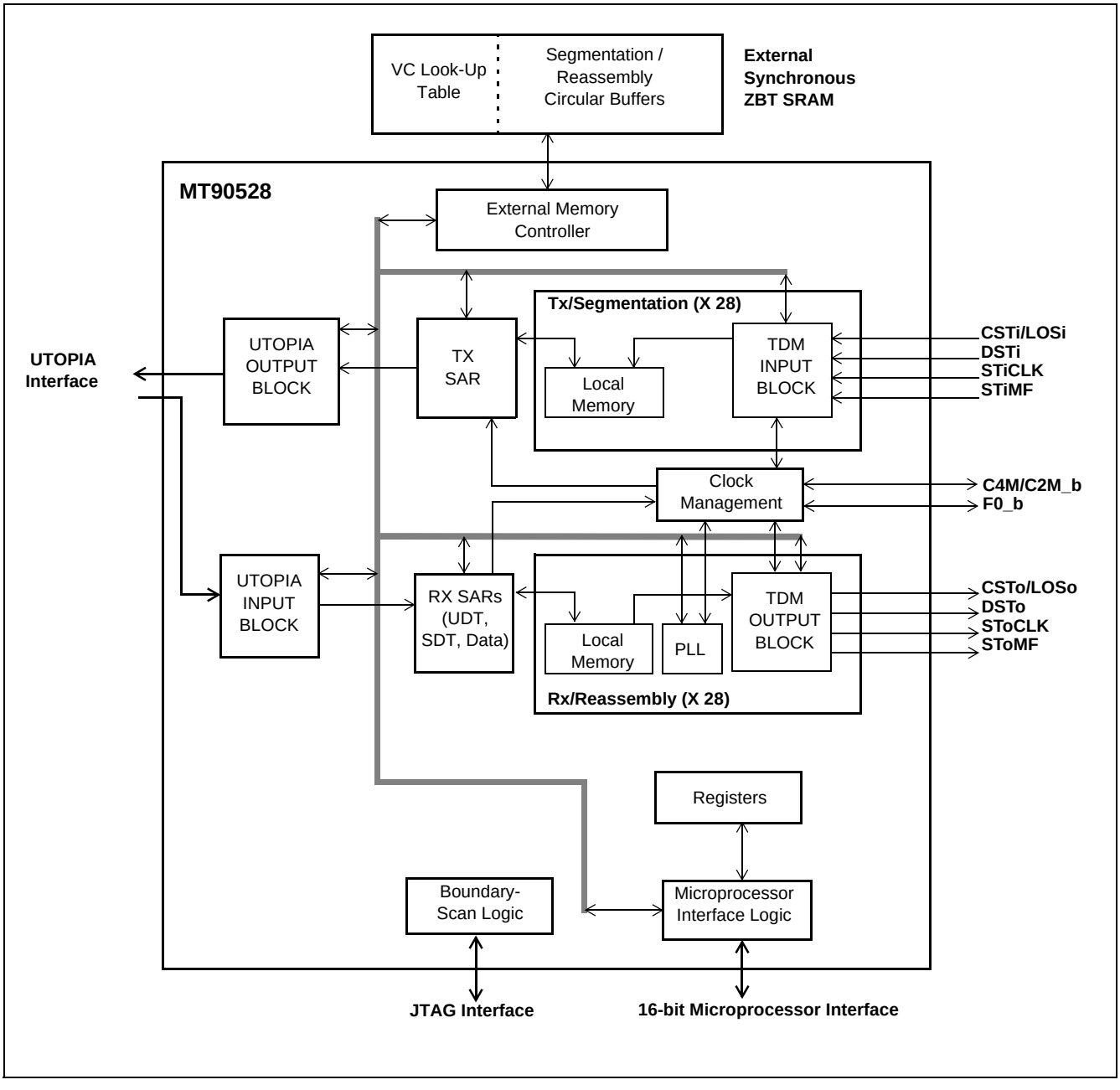


Figure 3 - MT90528 Block Diagram

2.0 Features

2.1 Key Functionality

- High-capacity AAL1 CES SAR device with 28 primary rate TDM ports operating at DS1 or E1 rates.
- Supports major modes of Circuit Emulation Services (CES) for DS1 and E1 as per af-vtoa-0078.000:
  - Logical Nx64 Structured Service, using 2.048 Mbps TDM bus
  - DS1 Nx64 Basic Service
  - DS1 Nx64 Service with CAS
  - E1 Nx64 Basic Service
  - E1 Nx64 Service with CAS
  - DS1 Unstructured Service
  - E1 Unstructured Service
- Supports AAL1 Trunking as per af-vtoa-0089.000:
  - Up to 128 TDM channels can be carried per VCC (up to 896 TDM channels per device)
- Compliant with ITU-T Rec. I.363.1
- Supports mixed DS1/E1 operation
- Supports mixed UDT/SDT operation
- Total clock recovery solution integrated on-chip
- Supports non-CBR data cells and OAM cells destined for microprocessor with Transmit and Receive Data Cell Buffers

2.2 Microprocessor Interface

- 16-bit microprocessor port, configurable to Motorola or Intel timing
- Indirect reads and writes possible to internal and external memory blocks
- Programmable interrupts for control and statistics
- Allows access to internal registers and memory for initialization, control and statistics
- Allows access to external RAM for initialization, control, and observation

2.3 External Memory Interface

- Supports common, commercially-available, no-latency flow-through and pipelined synchronous SRAM (ZBT, NoBL, NtRAM)
- Supports common SSRAM memory sizes - 128 K x 16, 256 K x16, 512 K x 16 and 1 M x 16; 128 K x 18, 256 K x 18, 512 K x 18 and 1 M x 18 (parity is optional)

2.4 TDM Interface

- Flexible TDM port allows operation with a wide selection of framers, LIUs, switches and multiplexers.
- Twenty-eight independently-timed, highly configurable, TDM interfaces can operate using:
  - bit-clock rate (Unstructured CES)
  - framed ST-BUS or Generic TDM bus (Structured CES - independent mode)
  - common TDM backplane clock using ST-BUS or Generic TDM bus (Structured CES - backplane mode)

- Supports up to 896 bidirectional TDM channels.

2.5 UTOPIA Interface

- UTOPIA Level 2 compliant 16-bit or 8-bit bus, capable of running at up to 52 MHz
  - Accepts data rate of up to 622 Mbps
  - Supports both “master” (ATM-end) and “slave” (PHY-end) operation
  - Supports multi-PHY (MPHY) mode when operating as a PHY device
- Capable of operating in UTOPIA Level 1 mode (8-bit bus running at up to 25 MHz), for connection to older devices
- Supports up to 896 bidirectional VCCs (Structured Nx64 mode)
- VPI/VCI Match and Match Enable filter prevents excessive look-up table accesses to external memory
- Cell reception based on look-up table allows flexible VCC assignment for CBR VCCs (allows non-contiguous VCC assignment)
  - Automatically eliminates null cells (i.e., VPI and VCI = 0)
  - Look-up table supports up to 65536 VCC entries

2.6 Segmentation and Reassembly Modules

- Supports AAL1 Segmentation and Reassembly for Structured and Unstructured CES as specified in af-vtoa-0078.000
- Supports non-multiframe or multiframe circuit emulation, using AAL1 structure formats as described in af-vtoa-0078.000: Nx64 Basic Service (single frame structure), or DS1 or E1 Nx64 Service with CAS (multiframe structure)
- Supports transmission and reception of up to 128 TDM channels per VCC in accordance with af-vtoa-0089.001 (ATM Trunking using AAL1 for Narrowband Services)
- Supports Unstructured CES and Structured CES simultaneously on different ports
- Supports 28 bidirectional VCCs, carrying 1.544 Mbps or 2.048 Mbps, in Unstructured CES mode
- Supports up to 896 bidirectional VCCs, carrying from 1 to 128 DS0 (64 kbps) TDM channels, in Structured CES mode (up to 896 DS0 channels total)
- UDT reassembly works with 28 per-port timing engines for fast processing and low delay variation in Unstructured CES mode (1 VCC per port, for 28 UDT VCCs total)
- Low latency in Unstructured CES mode provided by on-chip CDV buffering which does not require any external memory
- Internal CDV buffers of 2048 bytes for each UDT port
- Maximum UDT CDV buffering of $\pm$ 4.9 ms in DS1 mode and $\pm$ 3.7 ms in E1 mode
- External CDV buffers of 1024 bytes for each SDT port
- Maximum SDT CDV buffering of $\pm$ 63.75 ms (dependent on the Reassembly Circular Buffer size and number of channels per VC)
- Non-CBR data cell transmission and reception for software-implemented SAR function (through non-CBR Data Cell Buffers in external memory)
- Gathers statistical information and provides management statistics for network management through microprocessor interface
  - Per VCC monitoring compliant with ATMF CES specification Version 2.0 MIB
- Low latency in segmentation and reassembly directions

2.7 Clock Management

- Individual, per-port, integrated clock-recovery PLL allows for flexible, independent timing on each TDM port.
- Per-port Stratum 4 digital PLL supports several clock recovery modes:
  - Synchronous clocking - generates DS1 or E1 clock from network reference (19.44 MHz or 8 kHz)
  - Adaptive clocking - recovers clock from received-data buffer fill-level
  - SRTS - recovers clock from received RTS (residual time stamp) nibbles
  - Line-rate clocking - PLL locks to incoming DS1 or E1 clock and reduces jitter
  - Free-running clocks - PLL provides free-running high-accuracy clock for start-up or no-signal conditions (accuracy limited by MCLK accuracy)
  - Direct control of PLL output frequency - offset from centre frequency can be configured via CPU
- Support for optional external PLL such as MT9042 or MT9044: primary & secondary network references and primary & secondary LOS references output to external PLL; TDM_CLOCK input from external PLL
- Bus clock I/O for operation in backplane mode: C4M/C2M and F0

2.8 Testing Modes

- Per-port TDM_in to TDM_out low-latency loopback (DSTi input stream to DSTo output stream)
- Per-port TDM_in to TDM_out loopback through the Segmentation and Reassembly Circular Buffers in external memory (SDT mode only)
- Flexible, multi-stream, per-channel TDM circular-buffer loopback possible in SDT Backplane mode
- Loopback provided from incoming UTOPIA FIFO to outgoing UTOPIA FIFO (with or without filtering by Match and Match Enable registers)

2.9 Miscellaneous

- Master clock (MCLK) rate of 66.0 MHz
- 2.5 Volt core supply and 3.3 Volt I/O supply (5 V tolerant I/Os)
- Power consumption: 1.9 W
- IEEE 1149 (JTAG) Boundary-Scan Test Access Port
- 456-pin Plastic BGA
- -40°C to +85°C (industrial temperature range)

2.10 Interrupts

- Wide variety of interrupt source bits, allowing for easy monitoring of MT90528 operation
- Associated enable bits which enable or disable assertion of the service request and, ultimately, the $\overline{\text{IRQ}}$ interrupt pin

2.10.1 Module Level Service Requests

2.10.1.1 External Memory Interface Module

- External Memory Read Parity Error Alarm

2.10.1.2 TDM Module

- Per-port Loss of Signal Alarm (UDT mode only)
- Per-port UDT TDM Output Buffer Error Alarm (UDT mode only)
- Per-port SDT TDM Output Buffer Error Alarm (SDT mode only)
- Per-port Simple Underrun Error Alarm (SDT mode only)
- Per-port Permanent Underrun Error Alarm (SDT mode only)

2.10.1.3 UTOPIA Module

- UTOPIA Incoming Cell Counter Rollover
- Incoming Parity Mismatches Counter Rollover

2.10.1.4 TX_SAR Module

- Data TX_SAR - Transmit Non-CBR Data Cell Buffer Empty Alarm

2.10.1.5 UDT RX_SAR Module

- Reassembled Cell Counter Rollover
- AAL1-byte Header Error (i.e., CRC and/or Parity Error) Counter Rollover
- AAL1-byte Sequence Error Counter Rollover
- Lost Cell Counter Rollover
- Misinserted Cell Counter Rollover
- Write Underrun Counter Rollover
- Write Overrun Counter Rollover
- Late Cell Arrival Counter Rollover
- Overall UDT Cell Counter Rollover

2.10.1.6 SDT RX_SAR Module

- Reassembled Cell Counter Rollover
- AAL1-byte Header Error (i.e., CRC and/or Parity Error) Counter Rollover
- AAL1-byte Sequence Error Counter Rollover
- Lost Cell Counter Rollover
- Misinserted Cell Counter Rollover
- Pointer Reframe Counter Rollover
- Pointer Parity Error Counter Rollover
- Write Underrun Counter Rollover
- Write Overrun Counter Rollover
- Pointer Out-of-Range Indicator
- CAS Changed Status Indicator (only in CAS mode)
- Overall SDT Cell Counter Rollover

2.10.1.7 Data RX_SAR Module

- Data RX_SAR Cell Arrival Indicator
- Data RX_SAR Non-CBR Data Cell Buffer Overrun Alarm
- Data RX_SAR Buffer Half Full Indicator
- Data Cell Counter Rollover

2.10.1.8 UDT Reassembly-Side Timeout Module

- Per-port Cut VC Alarm
- Per-port Late Cell Arrival Alarm

2.11 Statistics

The MT90528 provides a number of statistics to allow monitoring of the MT90528. These statistics generally parallel the operation of some of the service request source bits.

2.11.1 TDM Module

- Per-port Simple Underrun Channel Indicator - status field indicates which channel of the TDM port last experienced a simple underrun (SDT mode only).
- Per-port Permanent Underrun Channel Indicator - status field indicates whether or not a particular channel of the TDM port has experienced a permanent underrun (SDT mode only).

2.11.2 UTOPIA Module

- UTOPIA Incoming Cell Counter
- Incoming Parity Mismatch Counter

2.11.3 TX_SAR Module

- Per-VC Transmitted Cell Counter

2.11.4 UDT RX_SAR Module

- Within each VC's UDT Reassembly Control Structure, there is a bit (V = VC Arrival) which is set each time that a cell arrives on the VC. CPU monitoring of this bit can be used to provide per-VC timeout monitoring.
  - As well, there is a late VC status bit and a cut VC status bit for each port (and therefore VC). These bits are set when user-programmable timeout periods are passed without cells arriving on the VCs in question.
- In addition to the counters themselves, if one of the following per-VC counters rolls over and the corresponding service enable bit for the counter is set, a status field indicates the number of the TDM port associated with the last UDT Reassembly Control Structure to generate a serviceable event.
  - Per-VC Reassembled Cell Counter
  - Per-VC AAL1-byte Header Error Counter
  - Per-VC AAL1-byte Sequence Error Counter
  - Per-VC Lost Cell Counter
  - Per-VC Misinserted Cell Counter
  - Per-VC Write Underrun Counter

  - Per-VC Write Overrun Counter
  - Per-VC Late Cell Arrival Counter
- Overall UDT Cell Counter

2.11.5 SDT RX_SAR Module

- Within each VC's SDT Reassembly Control Structure, there is a bit (V = VC Arrival) which is set each time that a cell arrives on the VC. CPU monitoring of this bit can be used to provide per-VC timeout monitoring.
- In addition to the counters themselves, if one of the following per-VC counters rolls over and the corresponding service enable bit for the counter is set, a status field indicates the address in internal memory of the last SDT Reassembly Control Structure to generate a serviceable event.
  - Per-VC Reassembled Cell Counter
  - Per-VC AAL1-byte Header Error Counter
  - Per-VC AAL1-byte Sequence Error Counter
  - Per-VC Lost Cell Counter
  - Per-VC Misinserted Cell Counter
  - Per-VC Pointer Reframe Counter
  - Per-VC Pointer Parity Error Counter
  - Per-VC Write Underrun Counter
  - Per-VC Write Overrun Counter
- Overall SDT Cell Counter

3.0 Pin Descriptions

3.1 Functional Pin Descriptions

Ball pin numbers are given in the following tables as defined in Figure 4 on page 33. Pins for buses are listed with the MSB appearing first.

I/O definitions are: Output (O), Input (I), Bidirectional (I/O), Power (PWR), or Ground (GND).

Input pad types are: CMOS or Schmitt, 3.3 V. The notations “PU” and “PD” are used, respectively, to indicate that a pad has a weak internal pullup or pulldown resistor. All 3.3 V inputs are 5 V tolerant. The 3.3 V CMOS inputs have a switching threshold of 1.6 V, and tolerate input levels of up to 5 V; therefore they are 5 V TTL compatible.

Output pad types are described by voltage rail and current capability. 3.3 V CMOS outputs will satisfy 5 V TTL input thresholds at the rated current of the output.

Ball Pin #	Pin Name	I/O	Type	Description
E9	Intel/$\overline{\text{Moto}}$	I	3.3 V CMOS PD	This input selects the microprocessor interface mode as Intel (pulled HIGH) or Motorola (pulled LOW). This pin must be configured before power-up.
A7	$\overline{\text{CS}}$	I	3.3 V CMOS PU	Active LOW chip select signal.
D8	$\overline{\text{WR}}$/R_$\overline{\text{W}}$	I	3.3 V CMOS PU	Active LOW Write Strobe (Intel) / Read_$\overline{\text{Write}}$ (Motorola).
C7	$\overline{\text{RD}}$/$\overline{\text{DS}}$	I	3.3 V CMOS PU	Active LOW Read Strobe (Intel) / Active LOW Data Strobe (Motorola).
B7	AEM	I	3.3 V CMOS PD	Access External Memory - CPU accesses external memory when HIGH (internal memory and registers when LOW). This pin is usually connected to a high-order CPU address line.
C15, A16, E15, D15, B16, C16, A17, B17, D16, C17, A18, B18, C18, D17, A19, B19, C19, D18, A20, E17	CPU_ADD[20:1]	I	3.3 V CMOS PD	CPU Address lines A20-A1. All microprocessor accesses to the device are word-wide, but addresses in this document are given as byte addresses. The virtual A[0] bit would select between high and low bytes within a word.
D9, C8, B8, A8, D10, C9, B9, A9, D11, E11, C10, B10, A10, C11, B11, D12	CPU_DATA[15:0]	I/O	3.3 V CMOS PD / 12mA	CPU data bus. All CPU accesses are word accesses.
C12	RDY/$\overline{\text{DTACK}}$	O	3.3 V, 24mA	Ready (Intel) / $\overline{\text{Data Transfer Acknowledge}}$ (Motorola). Acts as normal output in Intel mode, tristated when $\overline{\text{CS}}$ is HIGH; acts as active LOW pseudo-open-drain output in Motorola mode.
A11	$\overline{\text{IRQ}}$	O	3.3 V, 24mA	Active LOW interrupt line (operates as open-drain: high-impedance when inactive).

Table 1 - Microprocessor Interface Pins

Ball Pin #	Pin Name	I/O	Type	Description
H26	$\overline{\text{MEM_CS_1}}$	O	3.3 V, 8mA	Active LOW memory chip select signal for bank 1. This signal is used in all memory configurations to select bank 1 of external memory.
H25	$\overline{\text{MEM_CS_2}}$	O	3.3 V, 8mA	Active LOW memory chip select signal for bank 2. This signal is used to enable memory bank 2 when 2 or more banks of external RAM are connected to the MT90528.
H24	$\overline{\text{MEM_CS_3}}$	O	3.3 V, 8mA	Active LOW memory chip select signal for bank 3. This signal is used to enable memory bank 3 when 4 banks of external RAM are connected to the MT90528.
J23	$\overline{\text{MEM_CS_4}}$	O	3.3 V, 8mA	Active LOW memory chip select signal for bank 4. This signal is used to enable memory bank 4 when 4 banks of external RAM are connected to the MT90528.
G26	$\overline{\text{MEM_WR}}$	O	3.3 V, 8mA	Active LOW write enable.
B21, D20, C21, A22, B22, D21, A23, C22, D22, B23, A24, C23, D23, B24, A25, A26, B26, C24, B25, C25	MEM_ADD[19:0]	O	3.3 V, 8mA	Memory address lines. Connect these lines to external memory as follows: Bank Size of 1 M: MEM_ADD[19:0] are connected to memory. Bank Size of 512 K: MEM_ADD[18:0] are connected to memory. Bank Size of 256 K: MEM_ADD[17:0] are connected to memory. Bank Size of 128 K: MEM_ADD[16:0] are connected to memory.
D24, C26, D25, E23, E24, D26, G22, F23, E25, E26, J22, F24, G23, F25, F26, G24, H23, G25	MEM_DATA[17:0]	I/O	3.3 V CMOS PD / 8mA	Memory data lines. MEM_DATA[15:8] represent the upper byte; MEM_DATA[7:0] represent the lower byte. Optional lines [17] and [16] represent the high and low byte parity values, respectively.

Table 2 - External Memory Interface Pins

Ball Pin #	Pin Name	I/O	Type	Description
P24, M25, K25, K23, AB25, Y24, V24, T24, AD20, AC21, AE24, AD26, AE17, AE15, AE13, AE11, AC10, AC8, AD6, AD4, AC3, AB2, W4, V3, U1, P3, N2, K2	STiCLK[27:0]	I	3.3 V CMOS PD	PCM Input Clocks. These inputs are used to sample the incoming PCM data/ CAS from the E1 or DS1 lines. In Structured CES mode, ST-BUS format STiCLK is 4.096 MHz; Generic format STiCLK is 1.544 MHz or 2.048 MHz for DS1; or 2.048 MHz for E1. In Unstructured CES mode, these pins accept 1.544 MHz for DS1 or 2.048 MHz for E1.
R25, N25, N22, L22, AC26, W22, W26, U25, AF20, AD21, AE23, AF26, AF18, AB14, AF14, AC12, AC11, AE8, AE6, AE4, AD3, AC1, AA1, W2, R4, R3, N4, L2	STiMF[27:0]	I	3.3 V CMOS PD	Input Frame Pulses. In Structured CES mode, these pins are input frame pulses which set the frame boundaries for the incoming data and CAS. These signals can be either multiframe or frame inputs. Not used in Unstructured CES mode.
P25, M26, M23, J24, AA23, Y23, V25, T23, AC19, AE22, AD23, AE26, AD17, AD15, AD13, AB12, AE9, AD8, AF5, AF3, AD2, AA4, V5, U4, U2, R1, N1, K1	DSTi[27:0]	I	3.3 V CMOS PD	Serial PCM Data Inputs. In Unstructured CES mode, each pin carries a 1.544 Mbps or 2.048 Mbps serial stream. In Structured CES mode, each pin carries a 1.544 Mbps or 2.048 Mbps serial stream which contains a 24-channel data stream in DS1 operation or a 32-channel data stream in E1 operation.
R24, N24, K26, J25, AB24, Y25, V23, U26, AE20, AF22, AF24, AD25, AC16, AF16, AF13, AF11, AF9, AF7, AC7, AC5, AC4, Y5, Y3, W1, U3, R2, N3, L3	CSTi/LOSi[27:0]	I	3.3 V CMOS PD	Serial PCM Signalling Inputs or Input Loss of Signal (LOS) Indicators. In Structured CES mode, these pins carry CAS signalling inputs. In Unstructured CES mode, these pins input LOS signals from external LIUs.

Table 3 - TDM Port Pins

Ball Pin #	Pin Name	I/O	Type	Description
R26, R23, L24, N23, AC25, AA26, W24, U24, AC18, AC20, AC22, AE25, AE18, AC15, AE14, AD12, AD10, AB10, AD7, AD5, AE1, AB3, AA2, W3, T4, T1, M5, L1	SToCLK[27:0]	O	3.3 V, 4 mA	PCM Output Clocks. These outputs are used to drive the PCM data/CAS out to the E1 or DS1 lines. In Structured CES mode, ST-BUS format SToCLK is 4.096 MHz; Generic format SToCLK is 1.544 MHz or 2.048 MHz for DS1; or 2.048 MHz for E1. In Unstructured CES mode, these pins provide 1.544 MHz for DS1 or 2.048 MHz for E1.
T25, P23, M24, K24, AC24, AB26, Y26, U22, AF19, AB18, AB20, AF25, AC17, AF17, AF15, AC13, AD11, AF8, AB8, AE5, AF2, AD1, AB1, Y2, T5, T3, P4, M1	SToMF[27:0]	O	3.3 V, 4 mA	Output Frame Pulses. In Structured CES mode, these pins are output frame pulses which set the frame boundaries for the outgoing data and CAS. These signals are programmable as either multiframe pulses or frame pulses. Not used in Unstructured CES mode.
T26, N26, L25, J26, AB23, AA24, W25, U23, AD19, AE21, AD22, AC23, AD18, AE16, AC14, AE12, AE10, AC9, AF6, AC6, AE2, AB4, Y4, V4, V1, T2, P1, M3	DSTo[27:0]	O	3.3 V, 4 mA	Serial PCM Data Outputs. In Unstructured CES mode, each pin carries a 1.544 Mbps or 2.048 Mbps serial stream. In Structured CES mode, each pin carries a 1.544 Mbps or 2.048 Mbps serial stream which contains a 24-channel data stream in DS1 operation or a 32-channel data stream in E1 operation.
R22, P26, L26, L23, AA22, AA25, W23, V26, AE19, AF21, AF23, AD24, AB16, AD16, AD14, AF12, AF10, AD9, AE7, AF4, AF1, AC2, AA3, Y1, V2, P5, P2, M2	CSTo/ LOSo[27:0]	O	3.3 V, 4 mA	Serial PCM Signalling Outputs or Output Loss of Signal (LOS) Indicators. In Structured CES mode, these pins output CAS signalling. In Unstructured CES mode, each of these pins outputs an LOS or general purpose signal based on a user-programmable value in TDM Control Register 3 for the corresponding port.

Table 3 - TDM Port Pins

Ball Pin #	Pin Name	I/O	Type	Description
H2	UTO_IN_CLK	I/O	3.3 V CMOS PD / 24 mA	Synchronization clock for data transfer on UTO_IN_DATA. This clock can be output from an internal divider (equal to MCLK/2) or input from an external source. (RxClk when the MT90528 is in ATM mode; TxClk when the MT90528 is in PHY mode.)
L4, J1, J2, J3, K4	UTO_IN_ADD[4:0]	I	3.3 V CMOS PD	Multi-PHY address signals. These address inputs are used to poll the MT90528 and to select the next MPHY device to receive data on UTO_IN_DATA. These signals are driven from the ATM-end to the PHY-end, and only used when the MT90528 is in PHY mode. (Inactive when the MT90528 is in ATM mode; TxAddr when the MT90528 is in PHY mode.)
H3, J4, G1, G2, H4, G3, F1, F2, H5, G4, F3, E1, E2, F4, D1, E3	UTO_IN_DATA[15:0]	I	3.3 V CMOS PD	16-bit UTOPIA input bus for cell-based data. When in 8-bit mode, only bits [7:0] are active. (RxData[15:0] when the MT90528 is in ATM mode; TxData[15:0] when in PHY mode.)
K5	UTO_IN_PAR	I	3.3 V CMOS PD	Odd parity bit over UTO_IN_DATA[15:0]. When in 8-bit mode, odd parity bit over UTO_IN_DATA[7:0]. (RxPrty when the MT90528 is in ATM mode; TxPrty when in PHY mode.)
K3	UTO_IN_SOC	I	3.3 V CMOS PD	Start of Cell for UTO_IN_DATA. Active HIGH input signal indicating the first word/byte of the cell being received. (RxSOC when the MT90528 is in ATM mode; TxSOC when in PHY mode.)
M4	UTO_IN_CLAVATM_ ENBPHY	I	3.3 V CMOS PD	Handshake input for UTO_IN_DATA. When the MT90528 is in ATM mode, this input is RxClav, indicating that the PHY-end has a complete cell to transfer on UTO_IN_DATA. When the MT90528 is in PHY mode, this input is TxEnb*, indicating that the ATM-end is transferring valid data on UTO_IN_DATA.
H1	UTO_IN_ENBATM_ CLAVPHY	O	3.3 V, 16 mA	Handshake output for UTO_IN_DATA. When the MT90528 is in ATM mode, this output is RxEnb*, indicating that the MT90528 will begin to sample UTO_IN_DATA and UTO_IN_SOC at the end of the next clock cycle. When the MT90528 is in PHY mode, this output is TxClav, indicating that the MT90528 can accept a complete cell on UTO_IN_DATA.

Table 4 - UTOPIA Bus Pins

Ball Pin #	Pin Name	I/O	Type	Description
D5	UTO_OUT_CLK	I/O	3.3 V CMOS PD / 24 mA	Synchronization clock for data transfer on UTO_OUT_DATA. This clock can be output from an internal divider (equal to MCLK/2) or input from an external source. (TxClk when the MT90528 is in ATM mode; RxClk when the MT90528 is in PHY mode.)
E4, D2, C1, D3, D4	UTO_OUT_ADD[4:0]	I	3.3 V CMOS PD	Multi-PHY Address signals. These address inputs are used to poll the MT90528, and to select the next MPHY device to drive data on UTO_OUT_DATA. These signals are driven from the ATM-end to the PHY-end, and only used when the MT90528 is in PHY mode. (Inactive when the MT90528 is in ATM mode; RxAddr when the MT90528 is in PHY mode.)
A2, B3, C3, C4, A3, B4, C5, A4, D6, E7, B5, A5, C6, D7, B6, A6	UTO_OUT_DATA[15:0]	O	3.3 V, 12 mA	16-bit UTOPIA output data bus for cell-based data. When in 8-bit mode, only bits [7:0] are active. In Level 2 operation, this bus is tristated between cell transmissions. (TxData when the MT90528 is in ATM mode; RxData when in PHY mode.)
B1	UTO_OUT_PAR	O	3.3 V, 12 mA	Odd parity bit over UTO_OUT_DATA[15:0]. When in 8-bit mode, odd parity bit over UTO_OUT_DATA[7:0]. In Level 2 operation, this signal is tristated between cell transmissions. (TxPrty when the MT90528 is in ATM mode; RxPrty when in PHY mode.)
C2	UTO_OUT_SOC	O	3.3 V, 12 mA	Start of Cell for UTO_OUT_DATA. Active HIGH output signal indicating the first word/byte of the cell being transmitted. In Level 2 operation, this signal is tristated between cell transmissions. (TxSOC when the MT90528 is in ATM mode; RxSOC when in PHY mode.)
B2	UTO_OUT_CLAV ATM_ ENBPHY	I	3.3 V CMOS PD	Handshake input for UTO_OUT_DATA. When the MT90528 is in ATM mode, this input is TxClav, indicating that the PHY-end can accept a complete cell on UTO_OUT_DATA. When the MT90528 is in PHY mode, this input is RxEnb*, indicating that the ATM-end will begin to sample UTO_OUT_DATA and UTO_OUT_SOC at the end of the next clock cycle.
A1	UTO_OUT_ENBA TM_ CLAVPHY	O	3.3 V, 16 mA	Handshake output for UTO_OUT_DATA. When the MT90528 is in ATM mode, this output is TxEnb*, indicating that the data on UTO_OUT_DATA is valid. When the MT90528 is in PHY mode, this output is RxClav, indicating that the MT90528 has a complete cell ready to output on UTO_OUT_DATA.

Table 4 - UTOPIA Bus Pins

Ball Pin #	Pin Name	I/O	Type	Description
A15	TDM_CLK	I	3.3 V CMOS PD	Clock input from external PLL, operating at DS1/E1/ST-BUS line rate.
B15	PHY_CLK	I	3.3 V CMOS PD	PRS-traceable clock input (8 kHz reference clock or 19.44 MHz clock from PHY network layer).
C14	C4M/C2M_b	I/O	3.3 V CMOS PD / 24 mA	- Backplane clock to be used when all 28 TDM ports are to have the same input and output clock. - TDM clock running at either 4.096 MHz or 2.048 MHz. - Input in TDM backplane slave mode; output in TDM backplane master mode.
D14	F0_b	I/O	3.3 V CMOS PD / 24 mA	- Frame pulse which delineates the 8 kHz frame boundary on PCM input and output streams. - In 2.048 Mbps ST-BUS applications, this is a negative-going pulse straddling the frame boundary and lasting for one cycle of the 4.096 MHz clock. - In Generic bus applications, this signal may be a positive-going or negative-going pulse following the frame boundary and lasting for one bit cycle (i.e., one cycle of the 2.048 MHz clock). - Input in TDM backplane slave mode; output in TDM backplane master mode.
B14	PRI_REF	O	3.3 V, 2 mA	Output clock running at DS1/E1/ST-BUS line rate, used to provide a primary reference clock for an external PLL. **Note:** This pin will still present a clock (derived from an internal PLL) even if its source clock is experiencing an LOS condition. Therefore, the PRI_LOS signal should be used to qualify the quality of this clock.
A14	PRI_LOS	O	3.3 V, 2 mA	If high, indicates to an external PLL that the primary reference clock has experienced an LOS condition.
B13	SEC_REF	O	3.3 V, 2 mA	Output clock running at DS1/E1/ST-BUS line rate, used to provide a secondary reference clock for an external PLL.
A13	SEC_LOS	O	3.3 V, 2 mA	If high, indicates to an external PLL that the secondary reference clock has experienced an LOS condition.

Table 5 - Clock Management Pins

Ball Pin #	Pin Name	I/O	Type	Description
C13	MCLK	I	3.3 V CMOS	Master Clock. This signal drives the internal logic. The same clock should be driven to the external memory
A12	$\overline{\text{RESET}}$	I	3.3 V Schmitt PU	Chip reset signal (active LOW). Note that internal reset activity is synchronous to MCLK; this signal is latched internally and held, and MCLK must be applied to bring the MT90528 out of reset. The $\overline{\text{TRST}}$ pin (JTAG reset) should also be asserted LOW during chip reset. Also see RESET bit in Chip Wide Reset Register at address 0000h.
C20	TMS	I	3.3 V CMOS PU	JTAG Test Mode Select.
B20	TCK	I	3.3 V CMOS	JTAG Test Clock.
A21	TDI	I	3.3 V CMOS PU	JTAG Test Data In. Should be pulled HIGH if boundary-scan not in use.
D19	$\overline{\text{TRST}}$	I	3.3 V CMOS PU	JTAG Test Reset input (active LOW). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. **Note:** This pin has an internal pull-up and must be pulled down externally for normal operation.
E19	TDO	O	3.3 V, 4 mA	JTAG Test Data Out.
AB22, AE3	TEST_IN	I		Test input pins. These pins must be grounded.
AA5, AB6, AB9, AB13, AB17, AB21, E6, E10, E14, E18, E21, F5, F22, J5, K22, N5, P22, U5, V22	VDD_3.3V	PWR		Power for I/O logic (3.3 V).
AB5, AB7, AB11, AB15, AB19, E8, E12, E13, E16, E20, E22, G5, H22, L5, M22, R5, T22, W5, Y22	VDD_2.5V	PWR		Power for core logic.
B12, D13, E5, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16	VSS	GND		Ground for device.

Table 6 - Master Clock, Test, and Power Pins

Type	Input	Output	I/O	Power	Ground	Unused	Total
Microprocessor Interface	25	2	16	-	-	-	43
External Memory Interface	-	25	18	-	-	-	43
TDM Interface	112	112		-	-	-	224
UTOPIA	30	20	2	-	-	-	52
Clock Management	2	4	2	-	-	-	8
Miscellaneous	8	1	-	-	-	-	9
Power & Ground	-	-	-	38	39	-	77
Total	**177**	**164**	**38**	**38**	**39**	**0**	**456**

Table 7 - Pinout Summary

3.2 Physical Pin Description

3.2.1 Pin Description by Ball Pin Number

The following table lists each ball of the PBGA package and the corresponding functional pin name.

Ball Pin #	Pin Name
A1	UTO_OUT_ENBATM_ CLAVPHY
A2	UTO_OUT_DATA[15]
A3	UTO_OUT_DATA[11]
A4	UTO_OUT_DATA[8]
A5	UTO_OUT_DATA[4]
A6	UTO_OUT_DATA[0]
A7	$\overline{CS}$
A8	CPU_DATA[12]
A9	CPU_DATA[8]
A10	CPU_DATA[3]
A11	$\overline{IRQ}$
A12	$\overline{RESET}$
A13	SEC_LOS
A14	PRI_LOS
A15	TDM_CLK
A16	CPU_ADD[19]
A17	CPU_ADD[14]
A18	CPU_ADD[10]
A19	CPU_ADD[6]
A20	CPU_ADD[2]
A21	TDI
A22	MEM_ADD[16]
A23	MEM_ADD[13]
A24	MEM_ADD[9]
A25	MEM_ADD[5]
A26	MEM_ADD[4]
B1	UTO_OUT_PAR
B2	UTO_OUT_CLAVATM _ ENBPHY
B3	UTO_OUT_DATA[14]
B4	UTO_OUT_DATA[10]
B5	UTO_OUT_DATA[5]
B6	UTO_OUT_DATA[1]
B7	AEM
B8	CPU_DATA[13]
B9	CPU_DATA[9]
B10	CPU_DATA[4]
B11	CPU_DATA[1]
B12	VSS
B13	SEC_REF
B14	PRI_REF
B15	PHY_CLK

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
B16	CPU_ADD[16]
B17	CPU_ADD[13]
B18	CPU_ADD[9]
B19	CPU_ADD[5]
B20	TCK
B21	MEM_ADD[19]
B22	MEM_ADD[15]
B23	MEM_ADD[10]
B24	MEM_ADD[6]
B25	MEM_ADD[1]
B26	MEM_ADD[3]
C1	UTO_OUT_ADD[2]
C2	UTO_OUT_SOC
C3	UTO_OUT_DATA[13]
C4	UTO_OUT_DATA[12]
C5	UTO_OUT_DATA[9]
C6	UTO_OUT_DATA[3]
C7	$\overline{RD}/\overline{DS}$
C8	CPU_DATA[14]
C9	CPU_DATA[10]
C10	CPU_DATA[5]
C11	CPU_DATA[2]
C12	RDY/$\overline{DTACK}$
C13	MCLK
C14	C4M/C2M_b
C15	CPU_ADD[20]
C16	CPU_ADD[15]
C17	CPU_ADD[11]
C18	CPU_ADD[8]
C19	CPU_ADD[4]
C20	TMS
C21	MEM_ADD[17]
C22	MEM_ADD[12]
C23	MEM_ADD[8]
C24	MEM_ADD[2]
C25	MEM_ADD[0]
C26	MEM_DATA[16]
D1	UTO_IN_DATA[1]
D2	UTO_OUT_ADD[3]
D3	UTO_OUT_ADD[1]
D4	UTO_OUT_ADD[0]
D5	UTO_OUT_CLK
D6	UTO_OUT_DATA[7]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
D7	UTO_OUT_DATA[2]
D8	$\overline{WR}$/R_$\overline{W}$
D9	CPU_DATA[15]
D10	CPU_DATA[11]
D11	CPU_DATA[7]
D12	CPU_DATA[0]
D13	GND
D14	F0_b
D15	CPU_ADD[17]
D16	CPU_ADD[12]
D17	CPU_ADD[7]
D18	CPU_ADD[3]
D19	$\overline{TRST}$
D20	MEM_ADD[18]
D21	MEM_ADD[14]
D22	MEM_ADD[11]
D23	MEM_ADD[7]
D24	MEM_DATA[17]
D25	MEM_DATA[15]
D26	MEM_DATA[12]
E1	UTO_IN_DATA[4]
E2	UTO_IN_DATA[3]
E3	UTO_IN_DATA[0]
E4	UTO_OUT_ADD[4]
E5	VSS
E6	VDD_3.3V
E7	UTO_OUT_DATA[6]
E8	VDD_2.5V
E9	Intel/$\overline{Moto}$
E10	VDD_3.3V
E11	CPU_DATA[6]
E12	VDD_2.5V
E13	VDD
E14	VDD_3.3V
E15	CPU_ADD[18]
E16	VDD_2.5V
E17	CPU_ADD[1]
E18	VDD_3.3V
E19	TDO
E20	VDD_2.5V
E21	VDD_3.3V
E22	VDD_2.5V
E23	MEM_DATA[14]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
E24	MEM_DATA[13]
E25	MEM_DATA[9]
E26	MEM_DATA[8]
F1	UTO_IN_DATA[9]
F2	UTO_IN_DATA[8]
F3	UTO_IN_DATA[5]
F4	UTO_IN_DATA[2]
F5	VDD_3.3V
F22	VDD_3.3V
F23	MEM_DATA[10]
F24	MEM_DATA[6]
F25	MEM_DATA[4]
F26	MEM_DATA[3]
G1	UTO_IN_DATA[13]
G2	UTO_IN_DATA[12]
G3	UTO_IN_DATA[10]
G4	UTO_IN_DATA[6]
G5	VDD_2.5V
G22	MEM_DATA[11]
G23	MEM_DATA[5]
G24	MEM_DATA[2]
G25	MEM_DATA[0]
G26	$\overline{\text{MEM_WR}}$
H1	UTO_IN_ENBATM_ CLAVPHY
H2	UTO_IN_CLK
H3	UTO_IN_DATA[15]
H4	UTO_IN_DATA[11]
H5	UTO_IN_DATA[7]
H22	VDD_2.5V
H23	MEM_DATA[1]
H24	$\overline{\text{MEM_CS_3}}$
H25	$\overline{\text{MEM_CS_2}}$
H26	$\overline{\text{MEM_CS_1}}$
J1	UTO_IN_ADD[3]
J2	UTO_IN_ADD[2]
J3	UTO_IN_ADD[1]
J4	UTO_IN_DATA[14]
J5	VDD_3.3V
J22	MEM_DATA[7]
J23	$\overline{\text{MEM_CS_4}}$
J24	DSTi[24]
J25	CSTi/LOSi[24]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
J26	DSTo[24]
K1	DSTi[0]
K2	STiCLK[0]
K3	UTO_IN_SOC
K4	UTO_IN_ADD[0]
K5	UTO_IN_PAR
K22	VDD_3.3V
K23	STiCLK[24]
K24	SToMF[24]
K25	STiCLK[25]
K26	CSTi/LOSi[25]
L1	SToCLK[0]
L2	STiMF[0]
L3	CSTi/LOSi[0]
L4	UTO_IN_ADD[4]
L5	VDD_2.5V
L11	VSS
L12	VSS
L13	VSS
L14	VSS
L15	VSS
L16	VSS
L22	STiMF[24]
L23	CSTo/LOSo[24]
L24	SToCLK[25]
L25	DSTo[25]
L26	CSTo/LOSo[25]
M1	SToMF[0]
M2	CSTo/LOSo[0]
M3	DSTo[0]
M4	UTO_IN_CLAVATM_ ENBPHY
M5	SToCLK[1]
M11	VSS
M12	VSS
M13	VSS
M14	VSS
M15	VSS
M16	VSS
M22	VDD_2.5V
M23	DSTi[25]
M24	SToMF[25]
M25	STiCLK[26]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
M26	DSTi[26]
N1	DSTi[1]
N2	STiCLK[1]
N3	CSTi/LOSi[1]
N4	STiMF[1]
N5	VDD_3.3V
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
N22	STiMF[25]
N23	SToCLK[24]
N24	CSTi/LOSi[26]
N25	STiMF[26]
N26	DSTo[26]
P1	DSTo[1]
P2	CSTo/LOSo[1]
P3	STiCLK[2]
P4	SToMF[1]
P5	CSTo/LOSo[2]
P11	VSS
P12	VSS
P13	VSS
P14	VSS
P15	VSS
P16	VSS
P22	VDD_3.3V
P23	SToMF[26]
P24	STiCLK[27]
P25	DSTi[27]
P26	CSTo/LOSo[26]
R1	DSTi[2]
R2	CSTi/LOSi[2]
R3	STiMF[2]
R4	STiMF[3]
R5	VDD_2.5V
R11	VSS
R12	VSS
R13	VSS
R14	VSS
R15	VSS

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
R16	VSS
R22	CSTo/LOSo[27]
R23	SToCLK[26]
R24	CSTi/LOSi[27]
R25	STiMF[27]
R26	SToCLK[27]
T1	SToCLK[2]
T2	DSTo[2]
T3	SToMF[2]
T4	SToCLK[3]
T5	SToMF[3]
T11	VSS
T12	VSS
T13	VSS
T14	VSS
T15	VSS
T16	VSS
T22	VDD_2.5V
T23	DSTi[20]
T24	STiCLK[20]
T25	SToMF[27]
T26	DSTo[27]
U1	STiCLK[3]
U2	DSTi[3]
U3	CSTi/LOSi[3]
U4	DSTi[4]
U5	VDD_3.3V
U22	SToMF[20]
U23	DSTo[20]
U24	SToCLK[20]
U25	STiMF[20]
U26	CSTi/LOSi[20]
V1	DSTo[3]
V2	CSTo/LOSo[3]
V3	STiCLK[4]
V4	DSTo[4]
V5	DSTi[5]
V22	VDD_3.3V
V23	CSTi/LOSi[21]
V24	STiCLK[21]
V25	DSTi[21]
V26	CSTo/LOSo[20]
W1	CSTi/LOSi[4]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
W2	STiMF[4]
W3	SToCLK[4]
W4	STiCLK[5]
W5	VDD_2.5V
W22	STiMF[22]
W23	CSTo/LOSo[21]
W24	SToCLK[21]
W25	DSTo[21]
W26	STiMF[21]
Y1	CSTo/LOSo[4]
Y2	SToMF[4]
Y3	CSTi/LOSi[5]
Y4	DSTo[5]
Y5	CSTi/LOSi[6]
Y22	VDD_2.5V
Y23	DSTi[22]
Y24	STiCLK[22]
Y25	CSTi/LOSi[22]
Y26	SToMF[21]
AA1	STiMF[5]
AA2	SToCLK[5]
AA3	CSTo/LOSo[5]
AA4	DSTi[6]
AA5	VDD_3.3V
AA22	CSTo/LOSo[23]
AA23	DSTi[23]
AA24	DSTo[22]
AA25	CSTo/LOSo[22]
AA26	SToCLK[22]
AB1	SToMF[5]
AB2	STiCLK[6]
AB3	SToCLK[6]
AB4	DSTo[6]
AB5	VDD_2.5V
AB6	VDD_3.3V
AB7	VDD_2.5V
AB8	SToMF[9]
AB9	VDD_3.3V
AB10	SToCLK[10]
AB11	VDD_2.5V
AB12	DSTi[12]
AB13	VDD_3.3V
AB14	STiMF[14]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
AB15	VDD_2.5V
AB16	CSTo/LOSo[15]
AB17	VDD_3.3V
AB18	SToMF[18]
AB19	VDD_2.5V
AB20	SToMF[17]
AB21	VDD_3.3V
AB22	TEST_IN
AB23	DSTo[23]
AB24	CSTi/LOSi[23]
AB25	STiCLK[23]
AB26	SToMF[22]
AC1	STiMF[6]
AC2	CSTo/LOSo[6]
AC3	STiCLK[7]
AC4	CSTi/LOSi[7]
AC5	CSTi/LOSi[8]
AC6	DSTo[8]
AC7	CSTi/LOSi[9]
AC8	STiCLK[10]
AC9	DSTo[10]
AC10	STiCLK[11]
AC11	STiMF[11]
AC12	STiMF[12]
AC13	SToMF[12]
AC14	DSTo[13]
AC15	SToCLK[14]
AC16	CSTi/LOSi[15]
AC17	SToMF[15]
AC18	SToCLK[19]
AC19	DSTi[19]
AC20	SToCLK[18]
AC21	STiCLK[18]
AC22	SToCLK[17]
AC23	DSTo[16]
AC24	SToMF[23]
AC25	SToCLK[23]
AC26	STiMF[23]
AD1	SToMF[6]
AD2	DSTi[7]
AD3	STiMF[7]
AD4	STiCLK[8]
AD5	SToCLK[8]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
AD6	STiCLK[9]
AD7	SToCLK[9]
AD8	DSTi[10]
AD9	CSTo/LOSo[10]
AD10	SToCLK[11]
AD11	SToMF[11]
AD12	SToCLK[12]
AD13	DSTi[13]
AD14	CSTo/LOSo[13]
AD15	DSTi[14]
AD16	CSTo/LOSo[14]
AD17	DSTi[15]
AD18	DSTo[15]
AD19	DSTo[19]
AD20	STiCLK[19]
AD21	STiMF[18]
AD22	DSTo[17]
AD23	DSTi[17]
AD24	CSTo/LOSo[16]
AD25	CSTi/LOSi[16]
AD26	STiCLK[16]
AE1	SToCLK[7]
AE2	DSTo[7]
AE3	TEST_IN
AE4	STiMF[8]
AE5	SToMF[8]
AE6	STiMF[9]
AE7	CSTo/LOSo[9]
AE8	STiMF[10]
AE9	DSTi[11]
AE10	DSTo[11]
AE11	STiCLK[12]
AE12	DSTo[12]
AE13	STiCLK[13]
AE14	SToCLK[13]
AE15	STiCLK[14]
AE16	DSTo[14]
AE17	STiCLK[15]
AE18	SToCLK[15]
AE19	CSTo/LOSo[19]
AE20	CSTi/LOSi[19]
AE21	DSTo[18]
AE22	DSTi[18]

Table 8 - Pinout by Ball Pin Number

Ball Pin #	Pin Name
AE23	STiMF[17]
AE24	STiCLK[17]
AE25	SToCLK[16]
AE26	DSTi[16]
AF1	CSTo/LOSo[7]
AF2	SToMF[7]
AF3	DSTi[8]
AF4	CSTo/LOSo[8]
AF5	DSTi[9]
AF6	DSTo[9]
AF7	CSTi/LOSi[10]
AF8	SToMF[10]
AF9	CSTi/LOSi[11]
AF10	CSTo/LOSo[11]
AF11	CSTi/LOSi[12]
AF12	CSTo/LOSo[12]
AF13	CSTi/LOSi[13]
AF14	STiMF[13]
AF15	SToMF[13]
AF16	CSTi/LOSi[14]
AF17	SToMF[14]
AF18	STiMF[15]
AF19	SToMF[19]
AF20	STiMF[19]
AF21	CSTo/LOSo[18]
AF22	CSTi/LOSi[18]
AF23	CSTo/LOSo[17]
AF24	CSTi/LOSi[17]
AF25	SToMF[16]
AF26	STiMF[16]

Table 8 - Pinout by Ball Pin Number

3.2.2 Pin Diagram

The package is a 456 ball Plastic Ball Grid Array (PBGA). It has 420 signal balls and 36 balls for ground (VSS) and thermal conduction at the center. The outside dimensions are 35 mm x 35 mm. The pin pitch is 1.27 mm.

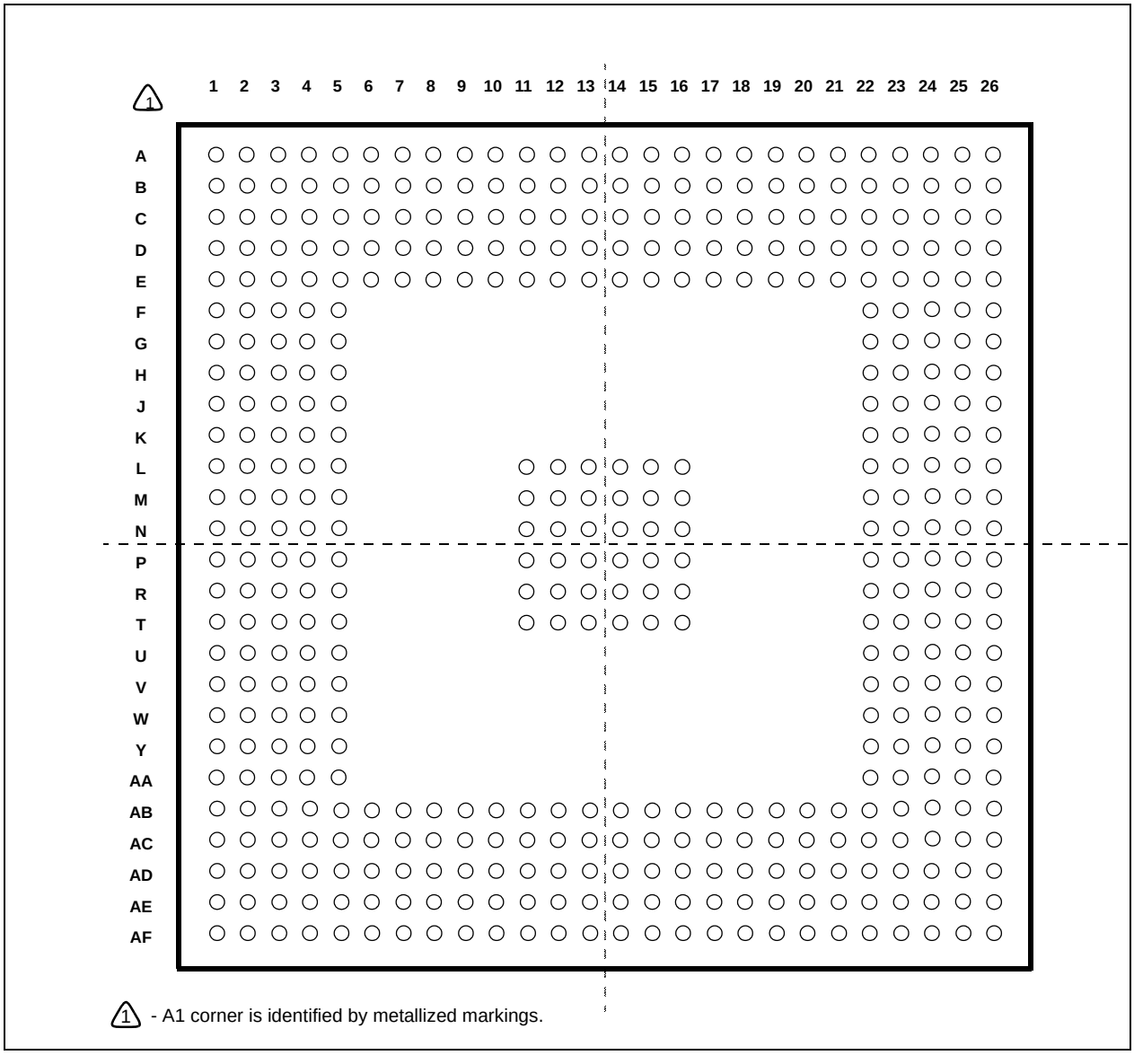


Figure 4 - PCB Pad Diagram for 35 mm x 35 mm PBGA (JEDEC MO-151)

3.2.3 Package Specifications

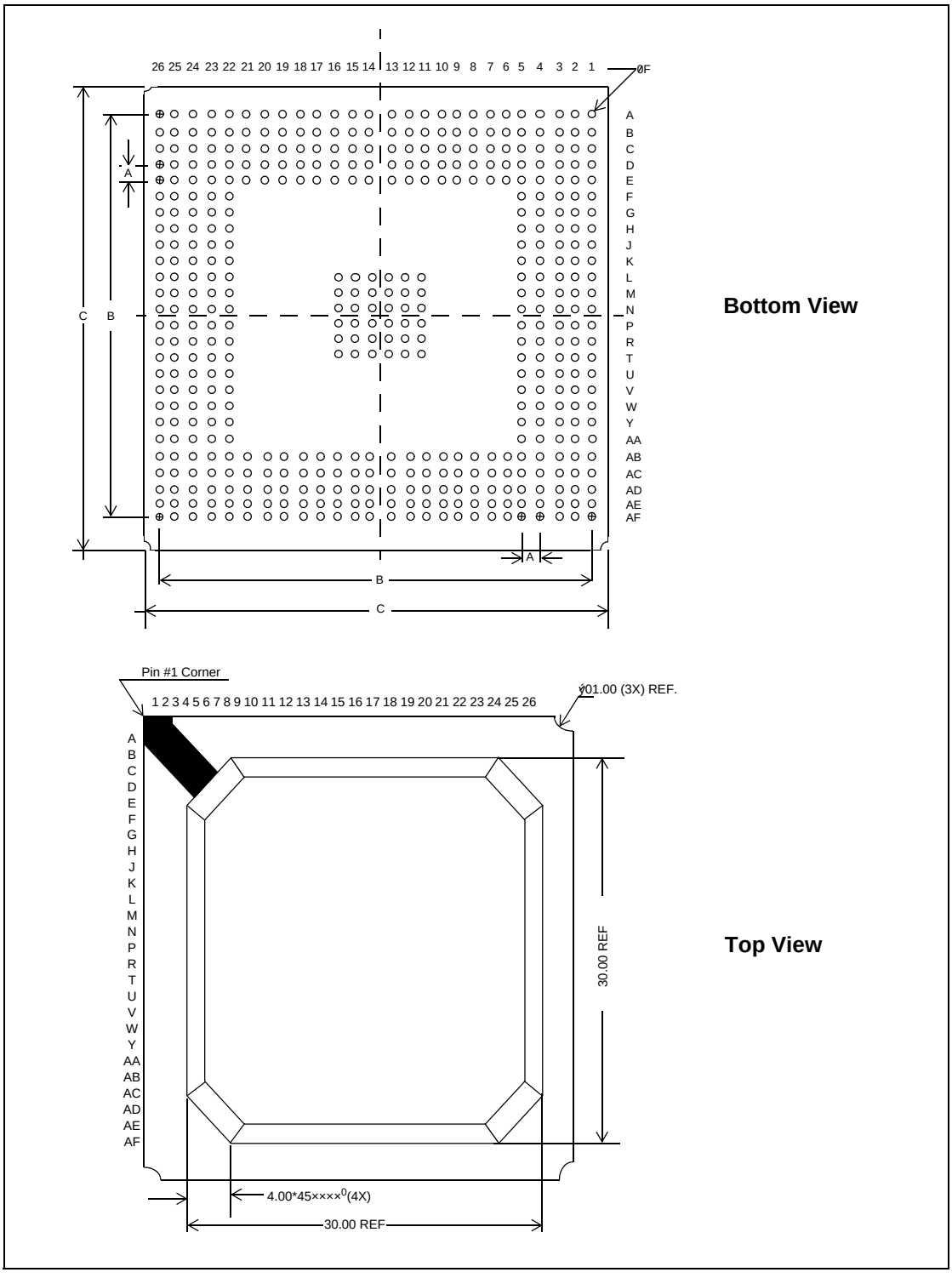


Figure 5 - Aerial View of Package Specifications

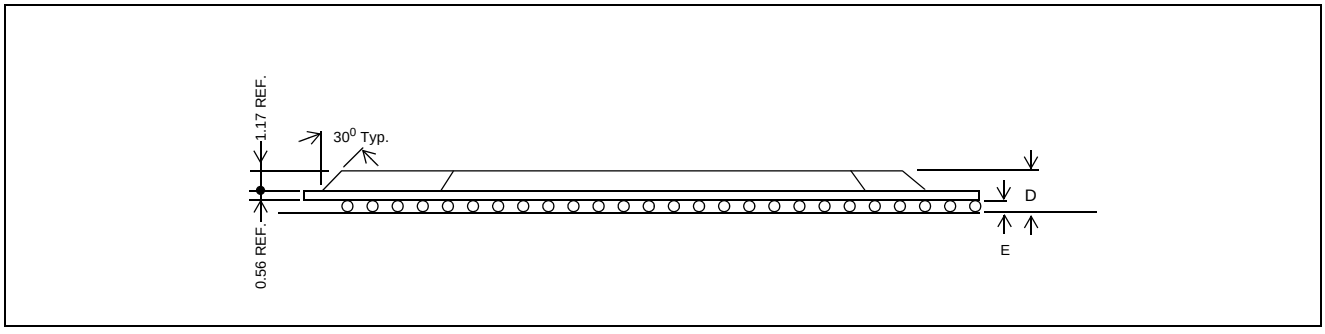


Figure 6 - Side View of Package Specification

Dim.	Min.	Max.	Notes
A	1.27 (REF)		solder ball grid pitch
B	31.75 (REF)		
C	34.80	35.20	
D	2.20	2.46	
E	0.50	0.70	stand-off height
F	0.60	0.90	solder ball diameter

Table 9 - Package Dimensions

Notes:

1) Dimensions are given in millimeters.

2) 456-pin BGA package complies to JEDEC Standard MO-151.

4.0 Module Functional Descriptions

As shown in Figure 3 on page 13, the MT90528 consists of the following major components: Microprocessor Interface Module, External Memory Interface Module, TDM Interface Module, UTOPIA Interface Module, TX_SAR Module, RX_SAR Modules (consisting of the UDT RX_SAR, SDT RX_SAR, and Data RX_SAR), the Clock Management Module, and the Test Interface (JTAG) Module. This section describes each module in detail.

4.1 Microprocessor Interface

The microprocessor interface permits an external microcontroller to access registers and internal memories within the MT90528 device. In addition, this interface provides the microcontroller with access to the external memory (synchronous ZBT SRAM) connected to the MT90528 device.

The MT90528 microprocessor interface is compatible with both Intel and Motorola processors. The user selects the mode of operation of the internal CPU block via the Intel/Motorola pin.

The synchronous microprocessor interface supports word (i.e., 16-bit) data accesses only. Although all microprocessor accesses to the device are word-wide, CPU addressing of the MT90528 is on a byte-wide basis. There is a 20-bit address bus between the microcontroller and the MT90528 interface, featuring address lines CPU_ADD[20] to CPU_ADD[1]. The virtual CPU_ADD[0] bit would select between high and low bytes in a word. The AEM (Access External Memory) pin is effectively address line CPU_ADD[21] (or any higher address line selected by the user) and determines if the CPU is accessing the internal registers and memories of the MT90528 (AEM = ‘0’) or the external memory (AEM = ‘1’).

All registers within the MT90528 device are accessed (for reads or writes) with fixed low latency. However, there is a variable delay between a CPU access and the successful completion of an access to a memory, whether internal to the device, or within external memory. In order to reduce this latency, the MT90528 supports indirect accesses to internal and external memory via indirection registers. The user can designate a memory address which is to be written or read, along with the data to be written to that memory location, and then initiate an indirect memory access. The CPU must then wait for the access to be completed by either polling a register bit (waiting for the ACC bit within the High Address Indirection Command Register at byte address 0006h to be cleared) or, if the service request was enabled, by waiting for an interrupt. Then, if the access was a read, the user can read the accessed data from the Indirection Data Register located at byte address 0008h. More information about the timing of CPU accesses can be found in Section 7.2.1 on page 164.

Interrupt signals from the various modules of the MT90528 are gated together within the microprocessor interface module to produce a single interrupt request signal, IRQ, which is presented to the CPU. There is a status register within the microprocessor interface module indicating which module of the MT90528 generated the interrupt request. As well, the microprocessor interface module contains an interrupt enable register which may be programmed by the user to enable or disable interrupt sources. Details regarding interrupt handling within the MT90528 are given in Section 4.1.2.

4.1.1 Global Reset

During a hardware reset (when the $\overline{\text{RESET}}$ pin is driven low), the CPU-accessible registers of the MT90528 go to their respective reset states, as indicated in the register descriptions of Section 6.2. At that time, the RESET bit in the Chip Wide Reset Register (CWRR) at 0000h is set high, “latching” the reset state. No registers other than the CWRR can be accessed until the RESET bit is cleared. The steps to reset and restart the MT90528 are therefore:

1. Assert hardware reset by driving the $\overline{\text{RESET}}$ pin low, or initiate a software reset by writing 0001h to the CWRR at byte address 0000h.
2. After at least 100 ns, remove hardware reset.
3. After at least 2 μs, clear the CWRR (de-assert software reset).
4. Write other MT90528 registers. (Note that configuration bits must generally be programmed before setting process enable bits.)

4.1.2 CPU Interrupts

The CPU interrupt mechanism works in a common way for all modules. Each module of the MT90528 has a status register and a service request enable register. One or more additional status-related registers may also be located within a module's address space.

When a status bit is asserted, the corresponding service enable bit is checked. If the bit is set, the module's service request will be raised. The service request of the module will be asserted and stay high as long as any one of the status/service enable pairs remains asserted.

This module's service request is sent to the device's Main Status Register (0002h). Within the microprocessor block, there is an Interrupt Enable Register, located at byte address 000Ah. If any of the individual module service requests is high, the corresponding interrupt enable bit is checked. If the appropriate interrupt enable bit is set, the CPU module generates a global interrupt by driving the $\overline{IRQ}$ pin low. Note that the $\overline{IRQ}$ pin is tristated when there is no active interrupt source. Refer to Figure 7 for an example of how an interrupt is generated within the MT90528.

Note that some of the modules within the MT90528 feature an additional level of interrupt masking. The memory- and register-based interrupt mechanisms for these modules (UDT RX_SAR, SDT RX_SAR, and TDM) are explained in the module descriptions for the blocks later in this document.

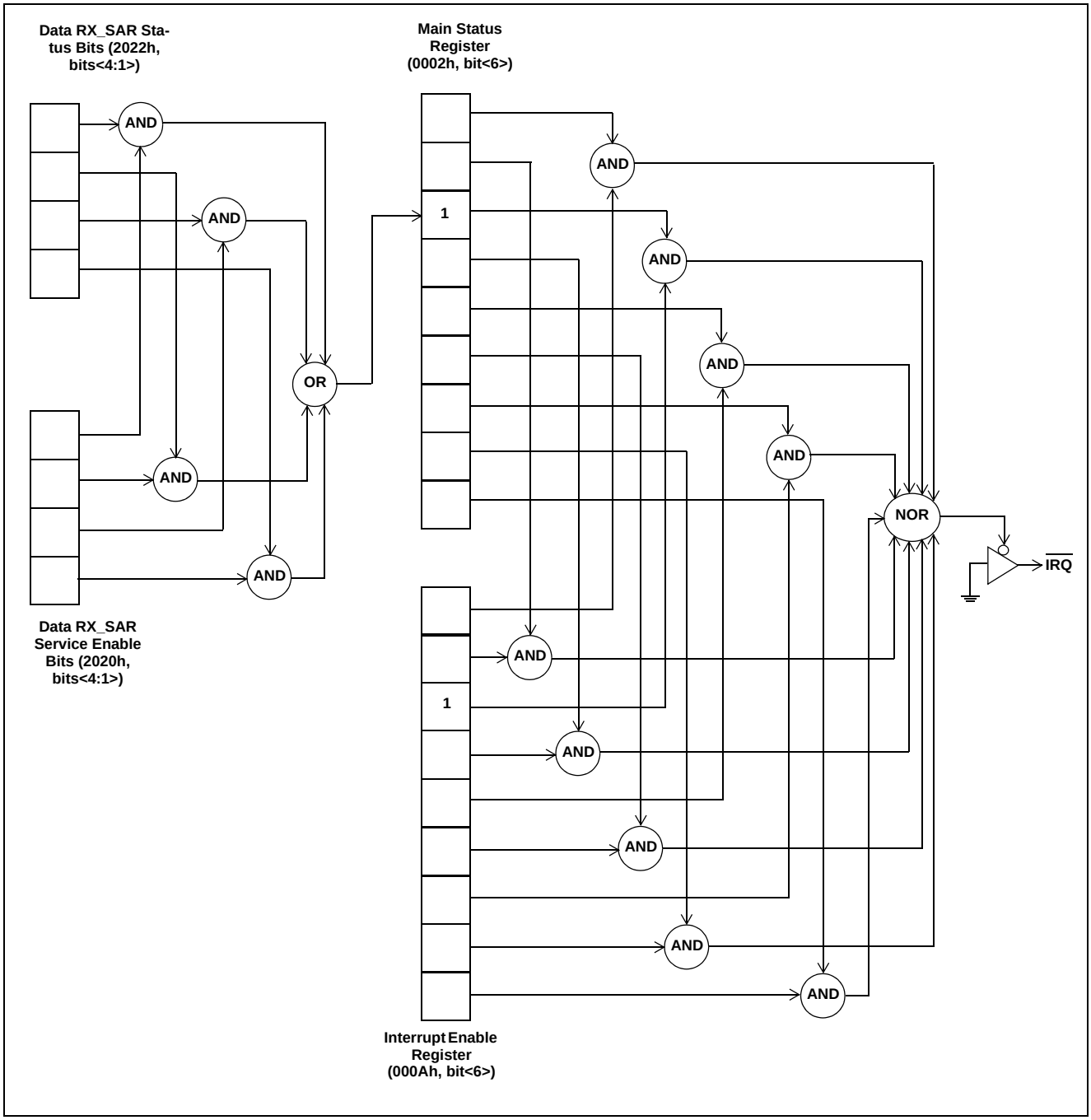


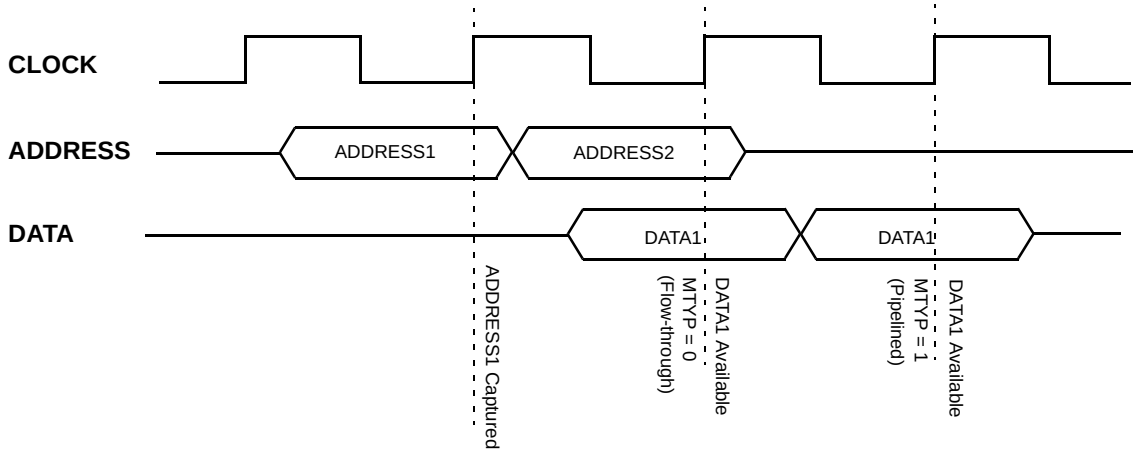
Figure 7 - Sample Interrupt Generation (for Data RX_SAR Module)

4.2 External Memory Interface

The external memory interface module of the MT90528 provides access to external memory devices by various MT90528 modules (i.e., TDM, TX_SAR, UTOPIA, SDT RX_SAR, Data RX_SAR) and by the CPU.

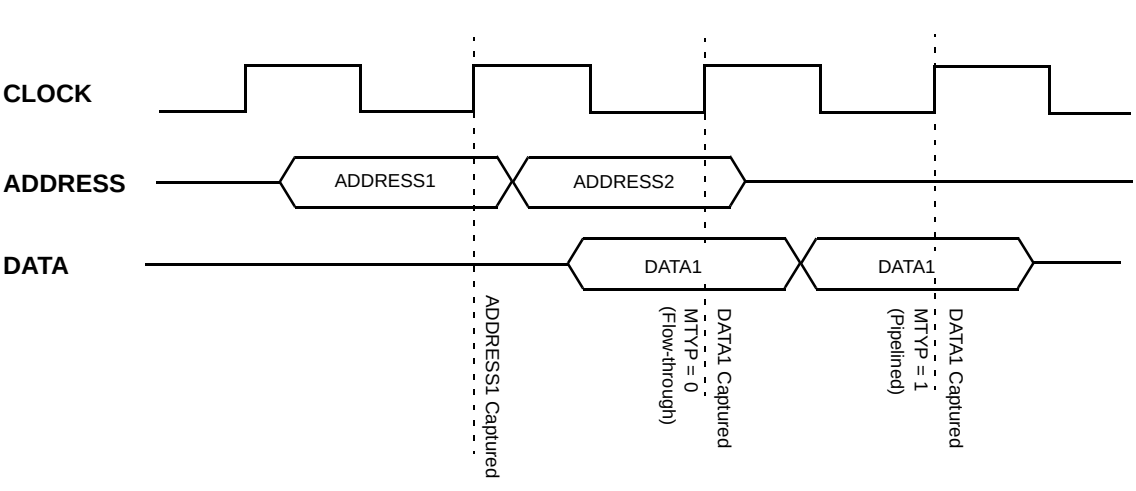
The MT90528 can interface with both the pipelined and flow-through types of synchronous zero bus turnaround (ZBT) RAM. The difference between flow-through and pipelined memories is illustrated in Figure 8 and Figure 9. In the case of flow-through memory, read cycle data is available on the next rising clock edge after the address is sampled by the memory. Contrarily, the data from pipelined memory is available two rising clock edges after the

address is sampled by the memory. A flow-through write cycle requires that valid data be placed on the data bus before the next rising clock edge after the address is sampled. On the other hand, data must be valid before the second rising edge of the clock after the address is presented to memory in the case of pipelined RAM.



Note: The number of clock cycles between an address (ADDRESS1) and its read data (DATA1) is set according to the MTYP field in the Memory Arbiter Configuration Register at byte address 7000h.

Figure 8 - Memory Read Pipeline Length



Note: The number of clock cycles between an address (ADDRESS1) and its written data (DATA1) is set according to the MTYP field in the Memory Arbiter Configuration Register at byte address 7000h.

Figure 9 - Memory Write Pipeline Length

Accesses to/from the external memory are made on a word-wide (i.e., 16-bit) basis. 2 optional bits, MEM_DATA[17:16], can provide parity data regarding the external memory data. The external memory interface module of the MT90528 generates MEM_DATA[17] to represent the even parity bit over MEM_DATA[15:8]. Similarly, MEM_DATA[16] represents the even parity bit over MEM_DATA[7:0]. When data is read from external

memory, the external memory interface module checks the parity bits of the data which is read. If there are parity errors, they are reported in the Parity Error Status Register at byte address 7004h. A service enable bit may be set to cause a CPU interrupt to be generated due to the occurrence of a parity error on reads of external memory data.

The external memory interface of the MT90528 supports up to 1 Mword of external memory. The configuration is programmable via the Memory Arbiter Configuration Register at byte address 7000h, and some of the possible configurations are listed in Table 10 below:

Number of Memory Banks	Maximum Size of Each Memory Bank (words)	Maximum Total Memory Size (words)
1	1 M	1 M
2	512 K	1 M
4	256 K	1 M

Table 10 - Possible Memory Configurations

4.3 TDM Interface Module

The TDM Interface module of the MT90528 device is designed to interface to a time division multiplexed backplane bus, to external framers, and to external line interface units (LIUs). Thus, the TDM module can interface with buses which carry Nx64 kbps data or bit stream data. The TDM module is responsible for performing Structured Data Transfer with and without CAS, and Unstructured Data Transfer, as required to meet the CES specification, af-vtoa-0078.000.

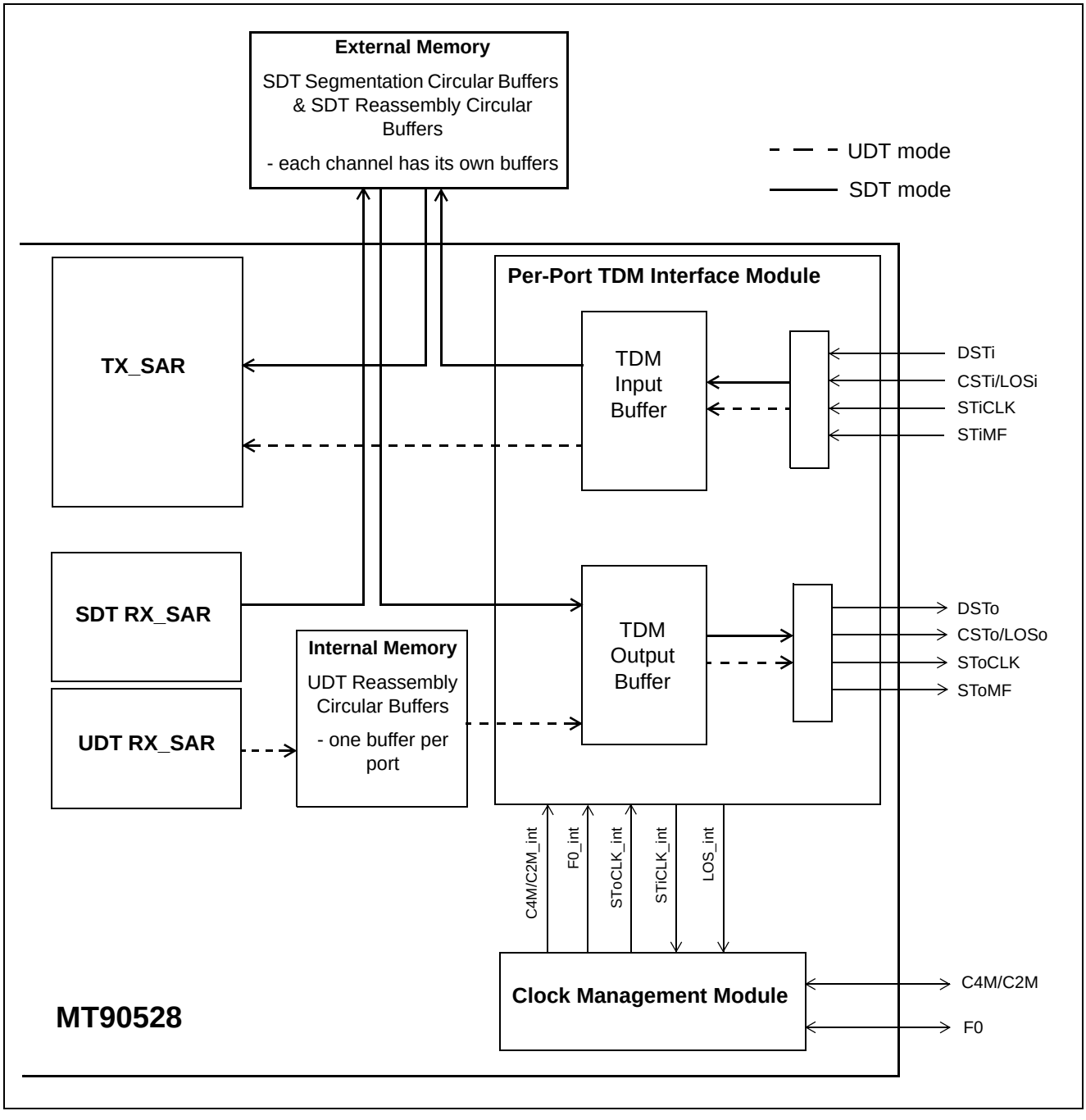


Figure 10 - Data Flow Through the TDM Module (1 port)

4.3.1 Overview

4.3.1.1 Segmentation Direction

In the UDT mode of operation, the segmentation process samples serial data received on DSTi and converts it to an 8-bit parallel stream. Data is then written to the TDM Input Buffer on a byte-by-byte basis and is read by the TX_SAR module in 47-byte blocks. Upon assertion of the LOSi (CSTi/LOSi pin) input signal, “all ones” data is written to the TDM Input Buffer.

In the SDT mode of operation, serial data and CAS are sampled from the DSTi and CSTi inputs respectively, and converted to separate 8-bit parallel streams. Data and CAS are then written to the Segmentation Circular Buffers (one for each TDM channel), located in external memory. The data written to external memory is then read by the TX_SAR module.

4.3.1.2 Reassembly Direction

In the UDT mode of operation, data is written to internal UDT Reassembly Circular Buffers (one per port) by the UDT RX_SAR module. This data is read by the TDM module and written to the TDM Output Buffer. The data is then read out of this buffer, converted to a serial stream and sent to the TDM output, DSTo.

In the SDT mode of operation, data and CAS are written by the SDT RX_SAR module to SDT Reassembly Circular Buffers (one for each TDM channel) located in external memory. Data and CAS are then read from external memory, converted to separate serial streams, and sent to the TDM outputs, DSTo and CSTo.

4.3.2 Functional Description

4.3.2.1 Segmentation Process

The incoming data on DSTi[p] can be sampled using the corresponding external pin STiCLK[p], C4M/C2M (for SDT backplane mode), or, in special circumstances (e.g., UDT LOS condition), an internal clock generated by the Clock Management Module.

STiMF[p] is defined as an input pin and is supplied by a framer. This pin is not used in UDT mode; in SDT mode, the user may choose to use either frame pulses or multiframe pulses on STiMF.

In ST-BUS mode, data and CAS are sampled on the falling edge of the selected TDM input clock. In Generic mode, data and CAS can be sampled either on the rising edge or the falling edge of the TDM input clock, depending upon the user’s selected configuration.

UDT Mode

Since there is no CAS in the UDT mode of operation, the CSTi/LOSi pin is used as an input for the Loss of Signal (LOS) line from an LIU. Loss of Signal polarity is specified by the user’s programming the TDM_LOS_POL bit in the per-port TDM Control Register 1.

Serial data which is received on the DSTi pin need not be aligned to any framing. If a framing signal is provided (on STiMF[p]), it will be ignored. Data is sampled using the TDM input clock STiCLK[p]. However, if a Loss of Signal is detected, an internally generated clock can (depending on the user-configuration) be used to sample the data: upon a Loss of Signal condition, if the TDM_LOS_CLK bit is set (in the per-port TDM Control Register 1), the internal clock will be used to sample the data. If a Loss of Signal is detected and the TDM_LOS_CLK bit is not set, the STiCLK input will continue to be used as the sampling clock.

If no Loss of Signal is detected, the sampled data is written to the TDM Input Buffer, where it is read by the TX_SAR. On the other hand, upon detecting a Loss of Signal, the TDM module ignores the data input on DSTi and writes all ones data to the TDM Input Buffer, for transfer to the TX_SAR.

SDT Mode

Data and CAS, received on the DSTi and CSTi/LOSi pins, respectively, are sampled on edges of either STiCLK[p] or C4M/C2M. If the TDM port is configured to be in backplane mode, the common clock C4M/C2M is used; if not, STiCLK[p] is used. Similarly, if the TDM port is in backplane mode, the frame pulse F0 is used to indicate the beginning of a frame, whereas STiMF[p] is used if the port is configured to be in independent mode.

In ST-BUS applications, a falling edge on STiMF[p]/F0 indicates the beginning of a frame/multiframe pulse. In Generic applications (and depending on the configuration specified by the user via register bits), either a rising or falling edge on STiMF[p]/F0 indicates the beginning of a frame/multiframe pulse.

The sampled data and CAS bytes are written to the TDM Input Buffer. In Generic DS1-1.544MHz mode, the framing bit (aligned with the frame pulse) is discarded by the TDM block, and therefore not transmitted in the ATM cells. The TDM segmentation process then transfers data and CAS to the SDT Segmentation Circular Buffers, located in external memory.

SDT Segmentation Circular Buffers

The main function of the SDT Segmentation Circular Buffers is to store data and CAS, coming from the TDM Input Buffer, for transfer to the TX_SAR. The buffers are composed of 16-bit wide entries, each of which is composed of the following fields, as shown in Figure 11:

- **Res (Reserved)** - bits<15:12> are unused.
- **CAS** - bits<11:8> are used to store the CAS nibbles.
- **TDM Data** - bits<7:0> store bytes of data received on DSTi.

The location of the SDT Segmentation Circular Buffers in external memory is determined by the Segmentation Circular Buffer Base Address (configured via TDM_SEGMEN_BASE_ADD in the per-port TDM Control Register 2). The SDT Segmentation Circular Buffer for the first channel of the DS1/E1 stream is located at the word address specified by TDM_SEGMEN_BASE_ADD. The second is located at TDM_SEGMEN_BASE_ADD + 64 words (128 bytes), etc., as seen in Figure 11. There is one circular buffer for each TDM channel and each buffer is 64 entries long.

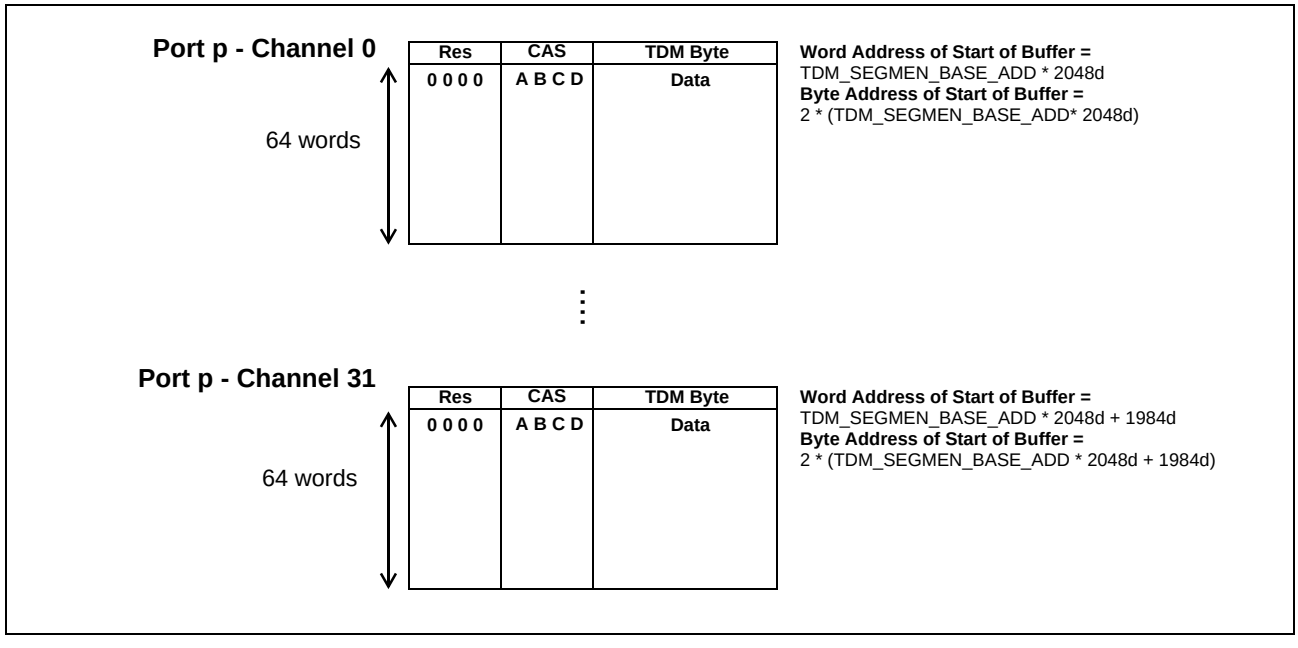


Figure 11 - Per-Port SDT Segmentation Circular Buffers

4.3.2.2 Reassembly Process

In the reassembly direction, the outgoing data on DSTo[p] is driven with its clock reference on the external pin SToCLK[p] or the backplane clock, C4M/C2M.

In SDT mode, the frame/multiframe pulse signal is either SToMF[p] in independent mode or F0 in backplane mode. The frame pulses are not used in UDT mode.

In ST-BUS mode, data and CAS are driven out on DSTo and CSTo/LOSo, respectively, on the falling edge of SToCLK[p] or C4M/C2M. In Generic mode, data and CAS can be driven out on either the rising or falling edge of the outgoing clock, depending on the configuration selected by the user.

4.3.2.3 UDT format

In this format, the data is written by the UDT RX_SAR to a UDT Reassembly Circular Buffer (one per port) in internal memory. The TDM module retrieves this data and writes it to the port's TDM Output Buffer. The data is then converted to a serial stream and sent out on DSTo, driven on the selected edge of SToCLK[p]. SToMF[p] is kept low by the TDM module. The CSTo/LOSo pin drives out the value specified by the user in the TDM_REASS_LOS bit (programmed in the per-port TDM Control Register 3).

In the case of an underrun, the TDM reassembly process continues to read from the port's internal circular buffer, but ignores the actual data read and instead writes "all ones" data to the TDM Output Buffer. The underrun detection is performed by the UDT RX_SAR. See Section and Section 4.6.2.3 for more details.

SDT format

In SDT mode, data and CAS are written to the SDT Reassembly Circular Buffers in external memory by the SDT RX_SAR (one buffer per channel). The data is then extracted from the SDT Reassembly Circular Buffers by the SDT TDM reassembly process and transferred to the per-port TDM Output Buffers.

Data and CAS are read out of the TDM Output Buffer, converted to separate bit streams and driven out on DSTo and CSTo/LOSo, on the selected edge of the TDM clock (SToCLK[p] if the device is in independent mode, or the common clock C4M/C2M if the device is in backplane mode). In DS1-1.544MHz mode, no framing bit is received in the ATM cells. Therefore, when the time comes to send out a framing bit (aligned with the frame pulse), the DSTo line is tristated for the duration of that bit.

The user can select either a multiframe or a frame pulse to be sent out on SToMF[p] by setting the TDM_PULSE_SEL bit (in the per-port TDM Control Register 1). However, if the device is in backplane mode, only frame pulses can be sent out on the common frame pulse pin, F0. The user can also select the format of the frame/multiframe pulse by setting the polarity control bit (TDM_PULSE_POL in TDM Control Register 1). The multiframe or the frame pulse is driven out on the selected edge of the appropriate TDM clock.

SDT Reassembly Circular Buffers

The main function of the SDT Reassembly Circular Buffers is to store reassembled TDM data and CAS for output onto the TDM bus. These circular buffers, which are located in external memory, are composed of 16-bit wide entries, each of which is composed of the following fields, as shown in Figure 12:

- **MF -** multiframe indicator; this bit is used only when a VC is carrying CAS data (if a VC isn't carrying CAS, the MF bits are always zero).
- **Res -** reserved field; this field always contains a zero.
- **Turn -** this field contains a copy of the two most-significant bits of the SDT RX_SAR write pointer for the VC. These bits are used by the TDM module for underrun detection.
- **CAS -** If CAS data is being processed, this field contains the nibble of data which was last received by this channel (i.e., in the previous multiframe). CAS data is repeated for an entire multiframe (i.e., 24 consecutive entries in DS1 case, 16 consecutive entries in E1 case).

- **TDM Byte -** This field contains the TDM data bytes which are extracted from received cells. If dummy cells have been inserted, this field contains the value of the dummy data programmed by the user.

The size of the SDT Reassembly Circular Buffers is variable, and there is one buffer for each TDM channel. For more details regarding fields of the SDT Reassembly Circular Buffers, refer to page 82.

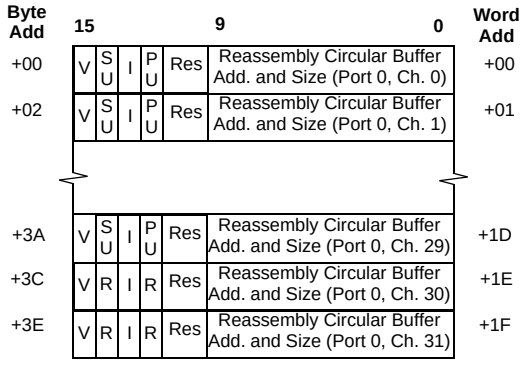
MF	Res	Turn	CAS	TDM Byte
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
1	0	01	ABCD	00101010
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX

Figure 12 - Per-Channel SDT Reassembly Circular Buffer

TDM SDT Reassembly Control Structure

Each TDM SDT Reassembly Control Structure is used to determine which TDM output channels of a particular port are valid, which ones are idle and whether to report underruns on particular channels. There is one entry per channel and one Control Structure per port. The TDM SDT Reassembly Control Structures are located in internal memory at byte addresses A0000h + p*800h. The format of the 16-bit entries is shown in Figure 13.

The Reassembly Circular Buffer Address field in each entry tells the hardware where the reassembly data and CAS are located (points to the location of the per-channel SDT Reassembly Circular Buffers in external memory). These addresses in external memory are formed using the TDM_REASS_BASE_ADD field (located in TDM Control Register 3) and the addresses programmed in the TDM SDT Reassembly Control Structure. Refer to Table 11 for more information on how the addresses are formed.



V (Valid): If this bit is set, the channel's output on DSTo and CSTo is valid. If this bit is '0', the channel's output on DSTo and CSTo is tristated. Should be used for mapping DS1 channels in 2.048 Mbps mode.
SU (Simple Underrun Service Enable): If this bit is set and a simple underrun is detected, a status bit is set and the underrunning channel is reported in the port's TDM Control Register 4.
I (Idle Enable): If this bit is set, idle data (user-programmable via Main TDM Control Register 2) will be output on DSTo for the channel's duration.
PU (Permanent Underrun Enable): If this bit is set and a permanent underrun is detected, a status bit is set in the port's TDM Control Register 4 and the underrunning channel is reported in the port's TDM Control Registers 5 & 6.
Res, R (Reserved): Unused. Must be set to 0.
Reassembly Circular Buffer Address & Size. The size field of this entry indicates if the Circular Buffer is 64, 128, 256, 512 or 1024 entries long. The leading bits in the field, when appended with a number of least-significant zeroes, indicate the Reassembly Circular Buffer word address, as shown in the drawing below.

Structure of the Reassembly Circular Buffer Address and Size Fields

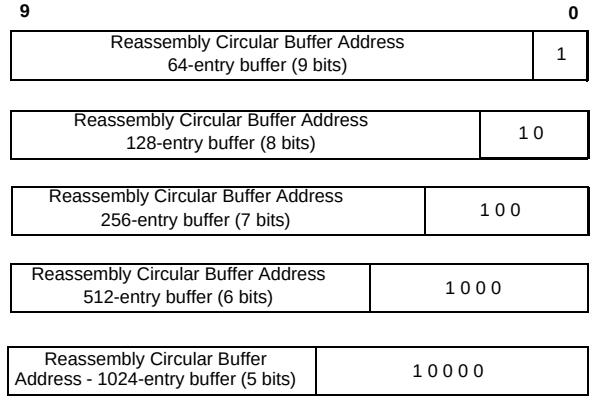


Figure 13 - TDM SDT Reassembly Control Structure

Buffer Size	Address to External Memory
64 entries	{TDM_REASS_BASE_ADD, Reassembly Circ. Buffer Add. and Size<9:1>, 6'b0}
128 entries	{TDM_REASS_BASE_ADD, Reassembly Circ. Buffer Add. and Size<9:2>, 7'b0}
256 entries	{TDM_REASS_BASE_ADD, Reassembly Circ. Buffer Add. and Size<9:3>, 8'b0}
512 entries	{TDM_REASS_BASE_ADD, Reassembly Circ. Buffer Add. and Size<9:4>, 9'b0}
1024 entries	{TDM_REASS_BASE_ADD, Reassembly Circ. Buffer Add. and Size<9:5>, 10'b0}

Table 11 - Formation of the Reassembly Circular Buffer Base Address

Underrun Detection in SDT Mode

The SDT TDM reassembly process reads data which was written to the SDT Reassembly Circular Buffers by the SDT RX_SAR block. Because the SDT RX_SAR and the TDM module don't operate at the same rate (i.e., data is written to the buffers based on the cell arrival rate while data is read from the buffers at a constant rate determined by the TDM output clock rate), there is a possibility of underruns. The SDT TDM reassembly process therefore performs underrun detection. The SDT TDM reassembly process compares the two most significant bits of the TDM channel's read pointer with the two bits called "turn" which are stored in the SDT Reassembly Circular Buffer entries:

1- If the comparison is true **(i.e., 2 MSB of the read pointer = turn)**, there is no underrun.

2- If the previous comparison is false, a second comparison **(2 MSB of the read pointer = turn + 1 or 2 MSB of the read pointer = turn + 2)** is performed. If this comparison is true, a simple underrun has occurred. The REPLAY_NSILENCE bit is checked: if it is set, the reassembly process keeps reading (old data) from the circular buffer. If it is not set, a silence byte (as configured in Main TDM Control Register 1) is written to the port's TDM Output Buffer for the underrunning channel. If the SU bit is set in the TDM SDT Reassembly Control Structure, a simple underrun is reported in the port's TDM Control Register 4.

3- If the two previous comparisons are false, a third comparison **(2 MSB of the read pointer = turn + 3)** is performed. If this comparison is true, a permanent underrun has occurred. The REPLAY_NSILENCE bit is checked: if it is set, the reassembly process keeps reading (old data) from the circular buffer. If it is not set, a silence byte (as configured in Main TDM Control Register 1) is written to the port's TDM Output Buffer for the underrunning channel. If the PU bit is set in the TDM SDT Reassembly Control Structure, a permanent underrun is reported in the port's TDM Control Registers 4, and 5 or 6.

Once a permanent underrun is detected on a TDM channel, underrun data (silence or old buffer data) will be sent out on DSTo[p] until the channel's permanent underrun bit is cleared in TDM5_Pp or TDM6_Pp.

Underrun Considerations

The SDT TDM reassembly process internal to the MT90528 performs underrun detection. Underruns are declared when the receive circular buffer does not have valid data to play out onto the TDM bus. The underrun detection is performed on a per channel basis for each of the up to 32 channels on a TDM port. The underrunning channels are reported TDM Control Register 4, TDM Control Register 5 and TDM Control Register 6.

Each active channel in a VC may be used independently to perform underrun detection. For example, in a 10 channel VC, each of the 10 channels may have their underrun detection activated. Thus all 10 channels are programmed to report underrun to the host processor. However the same functionality may be achieved by reporting underrun on a single channel in the VC, thereby reducing the amount of work required of the host processor and the number of interrupts generated. Given that all the channels are part of the same VC and will experience the same cell loss and CDV, when one channel underruns, they all underrun. So, for the example given, one channel would have its underrun detection activated and the 9 other channels would have their underrun detection disabled.

Internal to the MT90528 the underrun detection mechanism is dependent on the active channel order of the output TDM bus DSTo. Underrun is mis-reported on any channel (x) for which an upper channel (x+4) is not active on the same TDM port. As an example, channel 5 underrun status would be mis-reported if channel 9 of the same output TDM port was inactive. Given this operation it is suggested that underrun detection be enabled only on receive channels in a VC that are not mis-reporting underrun. Those channels which are mis-reporting underrun would have their underrun detection disabled. Note again that only a single channel per receive VC is required to have its underrun detection enabled to provide the equivalent functionality as all receive channels in a VC detecting underrun.

Silence Insertion

During an underrun condition bit 10 of TDM Control Register 3, REPLAY_N_SILENCE, is used to indicate whether old data or a silence byte will be played out onto the TDM bus signal DSTo. This bit is programmable on a per port basis. When the bit is set to 1 or REPLAY, old data from the reassembly circular buffer will be played out. When the bit is set to 0 or SILENCE, a programmable silence byte is played out onto the DSTo channel. The silence byte to be played out is programmed into the Main TDM Control Register 1, bits <15:8>.

When an active channel is mis-reporting an underrun condition the REPLAY_N_SILENCE bit still controls what data is played out onto the TDM bus. If this bit is set to 1 for REPLAY the correct data will be played out. If the bit is set to 0 for SILENCE then the silence byte will be played out rather than the correct data. As such, for bit error free operation, the REPLAY option must be selected for any TDM port where an active channel is mis-reporting an underrun condition.

Inactive Channels

A recommended solution would be to open a dummy receive VC(s) containing up to 128 inactive channels. This will increase the prospect that active channels (x) will not mis-report underrun as more (x+4) channels will be active. The procedure would be as follows

- To open a valid receive VC - mask TDM interrupts, close the dummy receive VC(s), open the valid receive VC, re-open the dummy receive VC(s) (with less channels), unmask the TDM interrupts
- To close a valid receive VC - mask TDM interrupts, close the valid receive VC, close the dummy receive VC(s), re-open the dummy receive VC(s) (with more channels), unmask the TDM interrupts

4.3.2.4 TDM Loopback

There are two loopback modes implemented in the TDM module.

4.3.2.5 TDM Low-Latency Loopback

The first loopback mode is TDM low-latency loopback, and is enabled by setting the TDM_LOW_LATENCY_LPBK bit in a port's TDM Control Register 1. When this bit is set, the TDM data coming in on DSTi is directly output on the DSTo output line of the same TDM port, with a delay through the device of about two TDM clock cycles.

TDM Circular Buffer Loopback (SDT Mode)

The second loopback is performed at the Circular Buffer level. It can only be used in SDT mode and it is selected by setting the TDM_CIR_BUF_LPBK bit in a port's TDM Control Register 1. In this loopback mode, the TDM SDT reassembly process uses the TDM_SEGMEN_BASE_ADD (in the per-port TDM Control Register 2) as the base address for the SDT Reassembly Circular Buffers in external memory. This loopback mode can be used to:

- loop back an entire stream
- loop back certain channels while tristating others
- switch the data between various channels (within the same port)

To determine which channels to loop back and their order, the TDM reassembly process reads the TDM SDT Reassembly Control Structure (refer to Figure 13 on page 46), which should be programmed in the following manner:

- **V -** The valid bits should be set for those channels which should be output on DSTo/CSTo. If the valid bit for a channel is not set, the output channel is tristated.
- **SU, I, and PU bits -** These bits should be cleared.
- **Reassembly Circular Buffer Address bits -**
  - bits<9:6> - These bits should be cleared as they are not used in loopback mode.
  - **bits<5:1> -** These five bits identify the input channel whose data is being output on the timeslot associated with this entry.
- **bit<0> -** This bit must be set to '1' (the SDT Segmentation Circular Buffers onto which the SDT Reassembly Circular Buffers are mapped always contain 64 entries).

4.4 UTOPIA Interface Module

The MT90528's UTOPIA interface is compliant with the ATM Forum Level 2 specification for the UTOPIA interface (af-phy-0039.000). The Level 2 specification is backwards-compatible with the Level 1 specification (af-phy-0017.000); therefore, the MT90528 interface also supports Level 1 applications. The UTOPIA interface is capable of emulating either a PHY device or an ATM device.

The MT90528's UTOPIA interface addresses reference configuration A of Figure 14 when it is operating in ATM mode. This means that the interface communicates with one, and only one, PHY. When the UTOPIA module is operating in PHY mode, it addresses reference configuration B of Figure 14.

The UTOPIA module does not address multi-PHY (MPHY) operation in ATM mode, nor does it address the use of multiple CLAV signals.

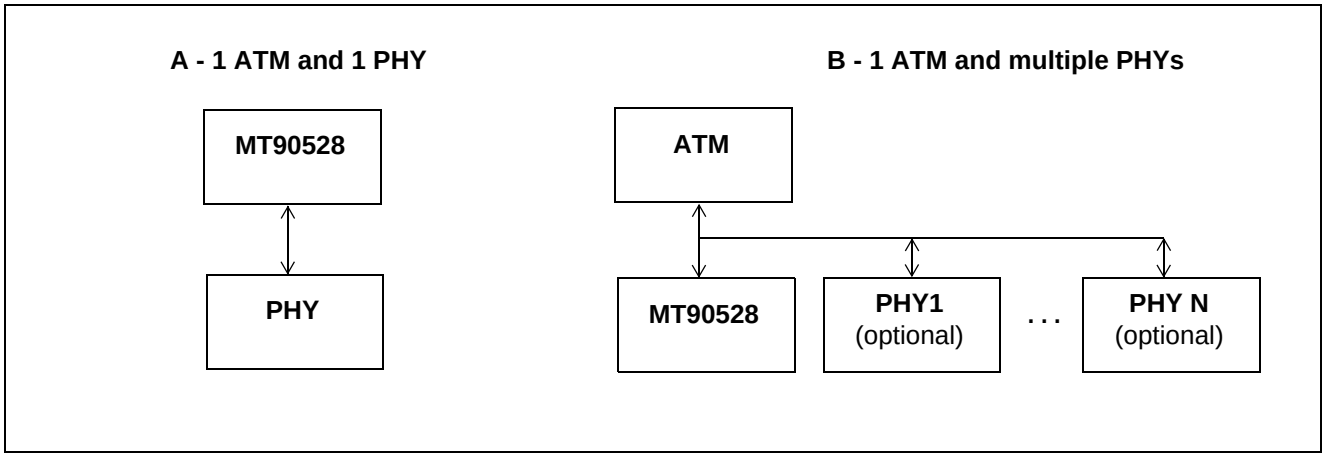


Figure 14 - UTOPIA Reference Configurations

The UTOPIA interface allows the user to choose between an 8-bit or 16-bit interface. The 8-bit interface is only specified to a maximum UTOPIA clock-rate of 33 MHz (in the UTOPIA Level 2 specification); however, the MT90528 interface is capable of operating up to 52 MHz.

The user can choose to have the UTOPIA interface emulate a PHY device or an ATM device. When the MT90528 is operating in PHY mode, it is capable of being polled; this allows the ATM device accessing the MT90528 to operate in multi-PHY mode.

The UTOPIA interface contains a loopback configuration, where data received on the incoming port can be looped back to the outgoing port. This is implemented to assist developers with debug and diagnostics.

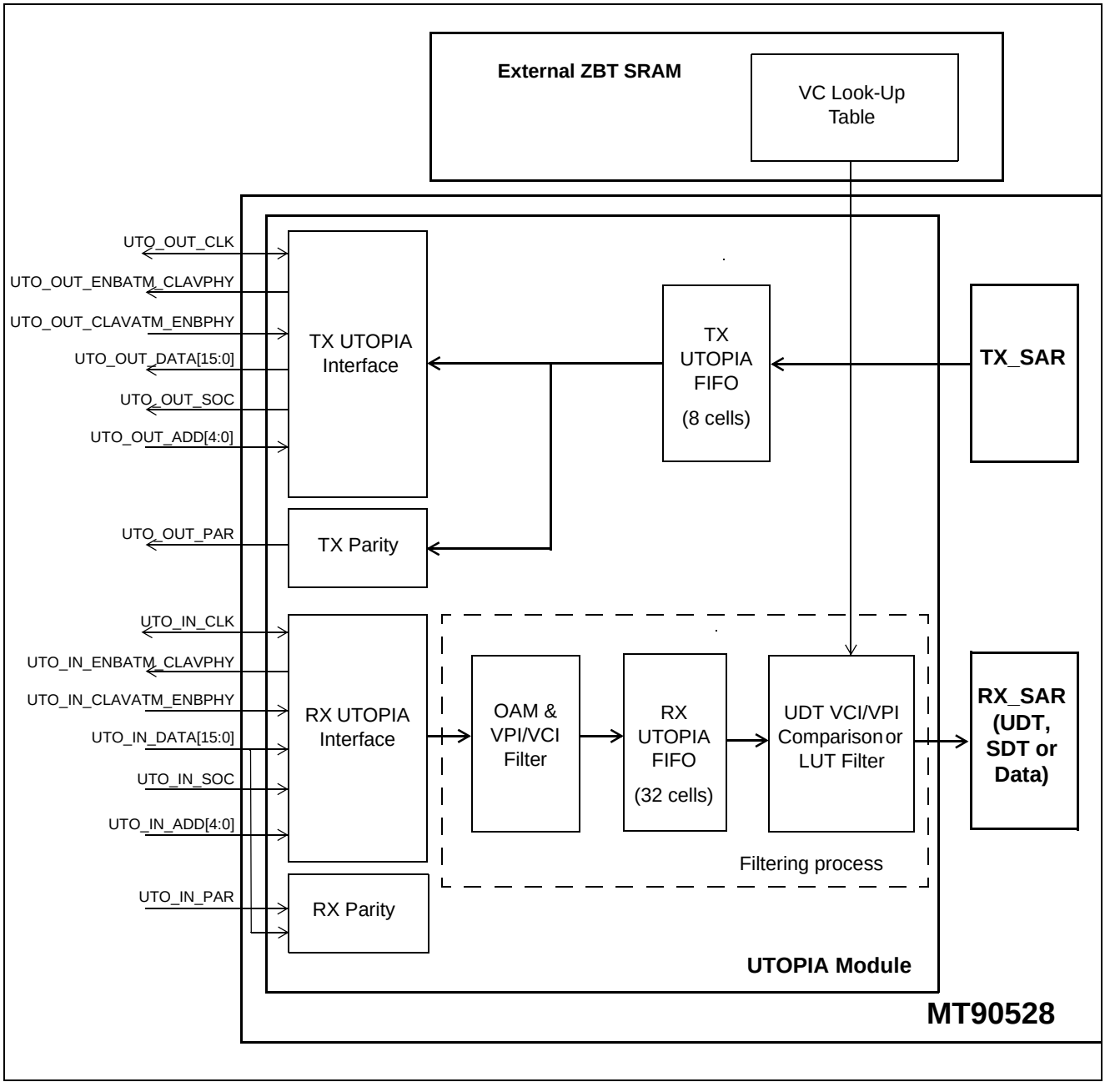


Figure 15 - UTOPIA Block Diagram

4.4.1 Functional Description

4.4.1.1 Segmentation Direction

TX UTOPIA Interface

The TX UTOPIA Interface's primary function is to transmit ATM cells to devices outside the MT90528 chip, according to the ATM Forum's Level 2 UTOPIA specification. The port can operate in either ATM or PHY mode. When the port is operating in ATM mode, it complies with the transmit portion of the ATM Forum specification; when operating in PHY mode, it complies with the receive portion of the specification. Additionally, when operating in PHY mode, the TX UTOPIA Interface complies with the receive sub-section of the multi-PHY section of the ATM Forum specification.

The TX UTOPIA Interface can be configured to operate in a variety of modes. The TX UTOPIA can operate in PHY or ATM mode, using Level 1 or Level 2 mode, with a 16-bit or 8-bit interface. The user selects between these different modes by programming the UTOPIA Configuration Register at byte address 4000h.

When operating in 16-bit mode, the cells transmitted by the interface are 54 bytes long, whereas when operating in 8-bit mode, the cells transmitted by the interface are 53 bytes long. When operating in 8-bit mode, the upper 8 bits of the outgoing data bus (UTO_OUT_DATA[15:8]) are not used.

When operating in Level 1 mode, the ATM Forum only specifies UTO_OUT_CLK to a maximum clock speed of 25 MHz. The user, however, is able to use the interface at speeds of up to 52 MHz, if desired.

TX UTOPIA FIFO

The main role of the TX UTOPIA FIFO is to act as a buffer between the TX_SAR and the TX UTOPIA Interface. This buffer is necessary because it is possible for the UTOPIA bus to be halted (i.e., not able to transmit) while the TX_SAR continues to assemble cells. This is an 8-cell deep FIFO.

TX Parity

The TX Parity sub-module generates an odd parity bit over the outgoing UTOPIA data (UTO_OUT_DATA[7:0] in 8-bit mode, and UTO_OUT_DATA[15:0] in 16-bit mode). The resulting parity bit (UTO_OUT_PAR) is transmitted to the external device to which the TX UTOPIA Interface is connected.

4.4.1.2 Reassembly Direction

RX UTOPIA Interface

The primary function of the RX UTOPIA Interface is to receive ATM cells (in accordance with the ATM Forum's Level 2 UTOPIA specification), from devices which are external to the MT90528 chip. The interface can operate in either ATM or PHY mode. When the interface is operating in ATM mode, it complies with the receive portion of the ATM Forum specification. When the interface operates in PHY mode, it complies with the transmit portion of the ATM Forum specification. In addition, when operating in PHY mode, the RX UTOPIA Interface complies with the transmit sub-section of the multi-PHY section of the ATM Forum specification.

In the same manner as the TX UTOPIA Interface, the RX UTOPIA Interface can be configured to operate in a variety of modes. It can operate in PHY or ATM mode, in Level 1 or Level 2 mode, with a 16-bit or an 8-bit interface. The user selects between these different modes by programming the UTOPIA Configuration Register (at byte address 4000h).

When operating in 16-bit mode, the cells received by the interface are 54 bytes long; when operating in 8-bit mode, the cells being received are 53 bytes long. When operating in 8-bit mode, the upper 8 bits of the incoming data bus (UTO_IN_DATA[15:8]) are not used.

When operating in Level 1 mode, the ATM Forum only specifies UTO_IN_CLK to a maximum clock speed of 25 MHz. However, the user is able to use the interface at speeds of up to 52 MHz, if desired.

OAM & VPI/VCI Filter

The role of the OAM & VPI/VCI filter sub-module is to limit unnecessary VPI/VCI comparison and look-up table accesses. The filter allows only certain cells to be written into the Receive UTOPIA FIFO of the MT90528 and discards unwanted cells. Unwanted cells fall into three categories:

- null cells (i.e., cells with VPI = 0 and VCI = 0); these cells are automatically discarded.
- cells whose VPI and/or VCI fall outside the Match and Match Enable filters which are configured via the registers at byte addresses 4008h - 400Ch.
- OAM cells (i.e., cells where the most significant bit of the PTI field in the cell header is set). OAM cells are discarded if the user clears the GLOBAL_OAM_SEL bit in the UTOPIA Configuration Register at 4000h

The filter considers the headers of cells received at the RX UTOPIA Interface; if cells pass through the Match and Match Enable filters successfully, the “accepted” cells are written to the RX UTOPIA FIFO.

The operation of OAM & VPI/VCI filter sub-module can be summarized by the flow chart in Figure 16.

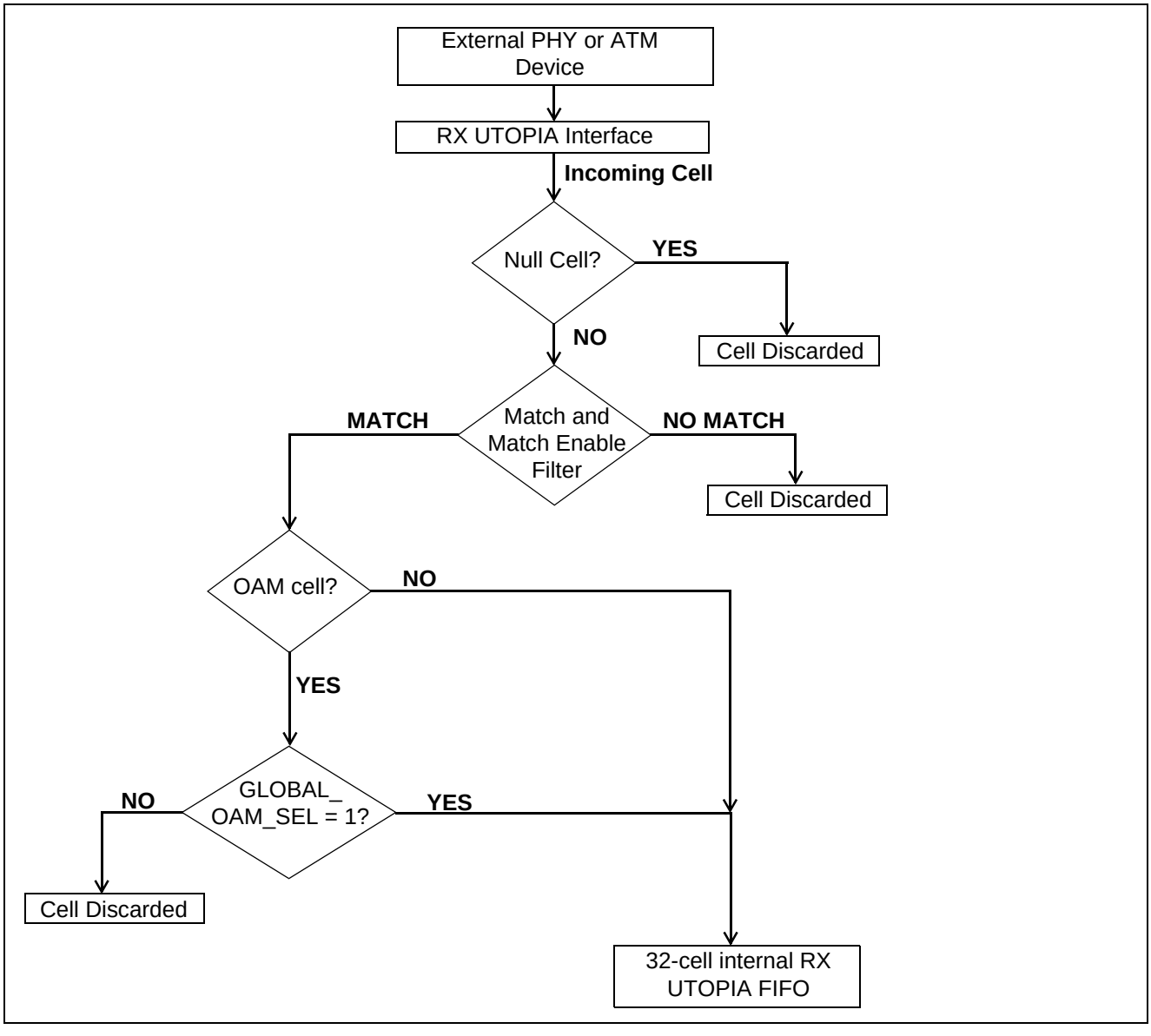


Figure 16 - OAM & VPI/VCI Filter Flowchart

The header of the incoming cell is transferred from the RX UTOPIA Interface to the OAM & VPI/VCI filter. Once the header has been received, the VPI and VCI fields are examined. If all the bits of the VPI field and all the bits of the VCI field are equal to zero, the cell is a filler cell (i.e., a null cell), and it is discarded. Otherwise, the processing of the cell continues in the Match and Match Enable filter.

In the Match and Match Enable filter, the cell's VPI field is examined first (all 12 bits, including the GFC). A bit-by-bit comparison of the VPI is performed using the contents of both the VPI Match Register (400Ah) and the VPI Match Enable Register (400Ch). If a bit value in the VPI Match Enable Register is '0', no comparison is performed on the corresponding bit in the VPI Match Register (and the bit is automatically accepted). If a bit value in the VPI Match Enable Register is '1', the comparison result is only true if the received VPI bit and the corresponding VPI Match Register bit are identical. The cell is only processed further if each of the 12 bit-comparisons produces a true result. Otherwise the cell is discarded.

If the VPI comparison is true, the same process is applied to the cell's VCI field, using the VCI Match Register (4006h) and the VCI Match Enable Register (4008h). The cell is only processed further if each of the 16 bit-comparisons produces a true result. Otherwise the cell is discarded.

If the VCI comparison is true, the most significant bit of the PTI field in the cell header is examined to determine if the cell is identified as carrying OAM information. If the received cell is not an OAM cell, it is automatically sent to the internal RX UTOPIA FIFO. If the received cell is an OAM cell and the GLOBAL_OAM_SEL bit in the UTOPIA Control Register is set, the cell is sent to the internal RX UTOPIA FIFO; OAM cells that are sent to this internal FIFO are treated as non-CBR data cells and are eventually sent to the Receive Data Cell Buffer in external memory. If the received cell is an OAM cell, but the GLOBAL_OAM_SEL bit is cleared, the cell is discarded.

Note: The VPI/VCI Match and Match Enable filter serves two important purposes. It can eliminate non-unique look-up table entries (this is important, because the look-up-table space is smaller than the entire VPI/VCI space of 16 M addresses), and it eliminates null cells. The Match and Match Enable filter can reduce the number of unnecessary look-up table accesses (and therefore unnecessary memory-access bandwidth) by eliminating cells with VPI/VCI combinations known not to be destined for the MT90528 device. The user is advised to set the VPI/VCI Match and Match Enable filter as narrowly as practical for the application.

RX UTOPIA FIFO

The primary role of the RX UTOPIA FIFO is to act as a buffer between the OAM & VPI/VCI Filter and the UDT VPI/VCI comparison and look-up table search sub-modules. This buffer is necessary because the RX UTOPIA Interface may be receiving cells while the next filtering modules are not yet ready to process them. The 32-cell deep FIFO therefore allows these cells to be stored until they can be processed.

UDT VCI/VPI Comparison and Look-up Table

This sub-module's primary function is to determine the destination of the cells; the module is responsible for determining to which of the RX_SARs (UDT, SDT or Data) cells should be directed. The RX_SARs are responsible for processing the received cells and transferring their contents to either a buffer in external memory or the TDM data bus.

UDT Operation

In the UDT case, the routing task is performed using a number of pre-defined match registers (one per port) which identify which cells are associated with a particular TDM port.

Up to twenty-eight (28) bits of the cell header may be used to perform this search: the GFC<3:0> field, the VPI<7:0> field, and the VCI<15:0> field. The 4-bit GFC field is only used when NNI-type cells are received. A global register bit (UNI_N_NNI in the UTOPIA Configuration Register) determines whether the GFC field is used in the search. Because the comparison sub-module operates as a pseudo-CAM, the incoming cell header is compared with all of the UDT search registers (4200h to 426Eh) simultaneously.

If the incoming cell is matched with a particular port, an additional comparison is performed to see whether the cell contains OAM data:

- If the cell contains OAM data (determined by the most significant bit of the PTI header field being set to '1') and the 'OAM_SEL' bit is set in the corresponding UDT VPI Register (located at 4202h + p*4h), the UTOPIA module sends the cell to the Data RX_SAR. The Data RX_SAR (if enabled) is responsible for copying the cell into the Receive Data Cell Buffer in external memory.
- If the cell is carrying OAM data but the user has selected not to process OAM cells for that port (i.e., 'OAM_SEL' bit for port = 0), the UTOPIA module discards the cell.
- If the cell is not carrying OAM data, the UTOPIA module sends the cell to the UDT RX_SAR for processing.

If external memory is present in the system configuration containing the MT90528, any received cells whose headers do not match those in the UDT search registers are passed to the look-up table sub-module and are processed as detailed in the SDT Operation section that follows. This additional processing is provided primarily to

permit the reception of non-CBR data cells, and for additional OAM-cells (cells with VCI = 3h or VCI = 4h). This extra processing also allows the user to process both SDT and UDT cells simultaneously. If no external memory is present, the cells with unmatched headers (after passing through the VPI/VCI comparison registers) are simply discarded.

SDT Operation

In the SDT case, the destination of the received cell is determined using a user-programmed look-up table. Unlike the UDT case, all 28 bits of the header are not used to perform the look-up. Rather, a VPI/VCI concatenation register (4002h) is provided for the user to choose how many bits of the cell header are to be used to form the look-up table addresses. The user selects up to 16 of the bits of the combined GFC/VPI and VCI fields to be used for the look-up table search. The look-up table itself is located in external memory, with each entry occupying one 16-bit word. As such, the external memory requirement for this structure is $\mathbf{2^{(VPI_bits + VCI_bits)}}$ words.

- **minimum:** 2^4 words (must use at least 4 bits from VCI field) = 16 words
- **maximum:** 2^{16} words (can use at most 16 bits from combined header fields) = 64 Kwords

Each successful look-up search provides two pieces of information:

- the destination of the received cell (e.g., TDM bus, Receive Data Cell Buffer)
- the address of the SDT Reassembly Control Structure associated with this VC (this field is ignored when the received cell is not a CBR-type cell).

Refer to Figure 17 for the structure of a look-up table entry.

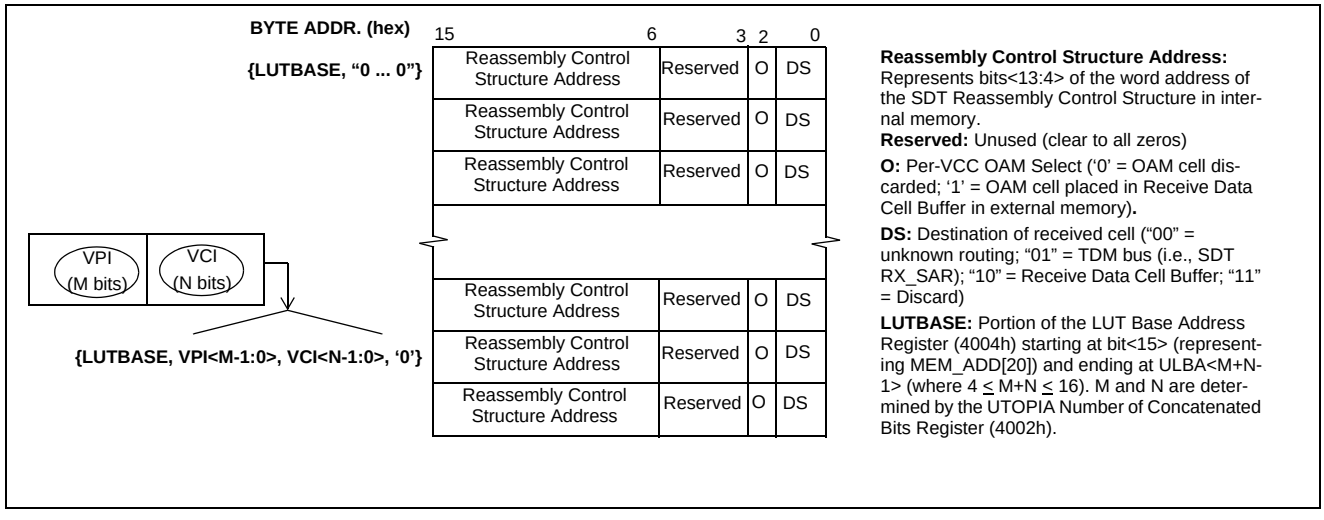


Figure 17 - Look-up Table Format

Depending on the value of the DS field of a look-up table entry, the UTOPIA module can process the cell in one of the following ways:

- if DS = “00”, and the global UKSEL bit is set (in the UTOPIA Configuration Register), the cell is sent to the Data RX_SAR for eventual storage in the Receive Data Cell Buffer in external memory
- if DS = “00”, and the global UKSEL bit is cleared, the cell is discarded and the UTOPIA module simply starts processing the next cell
- if DS = “01”, the cell as well as the SDT Reassembly Control Structure Address from the look-up table entry are sent to the SDT RX_SAR
- if DS = “10”, the complete cell is sent to the Data RX_SAR. F4 level OAM cells (cells with VCI = 3 or VCI = 4) should be set to DS = “10”
- if DS = “11”, the cell is discarded and the UTOPIA module simply starts processing the next cell.

Refer to Figure 18 on page 57 for an overview of the complete UDT VCI/VPI comparison and look-up table searches.

RX Parity

The RX Parity sub-module’s role is to calculate the odd parity bit over UTO_IN_DATA[15:0] (over UTO_IN_DATA[7:0] when operating in 8-bit mode). The module then compares the internally calculated value with the one supplied by the external system on UTO_IN_PAR. If the parity bits do not match, a counter is incremented in the UTOPIA Parity Mismatches Register (400Eh).

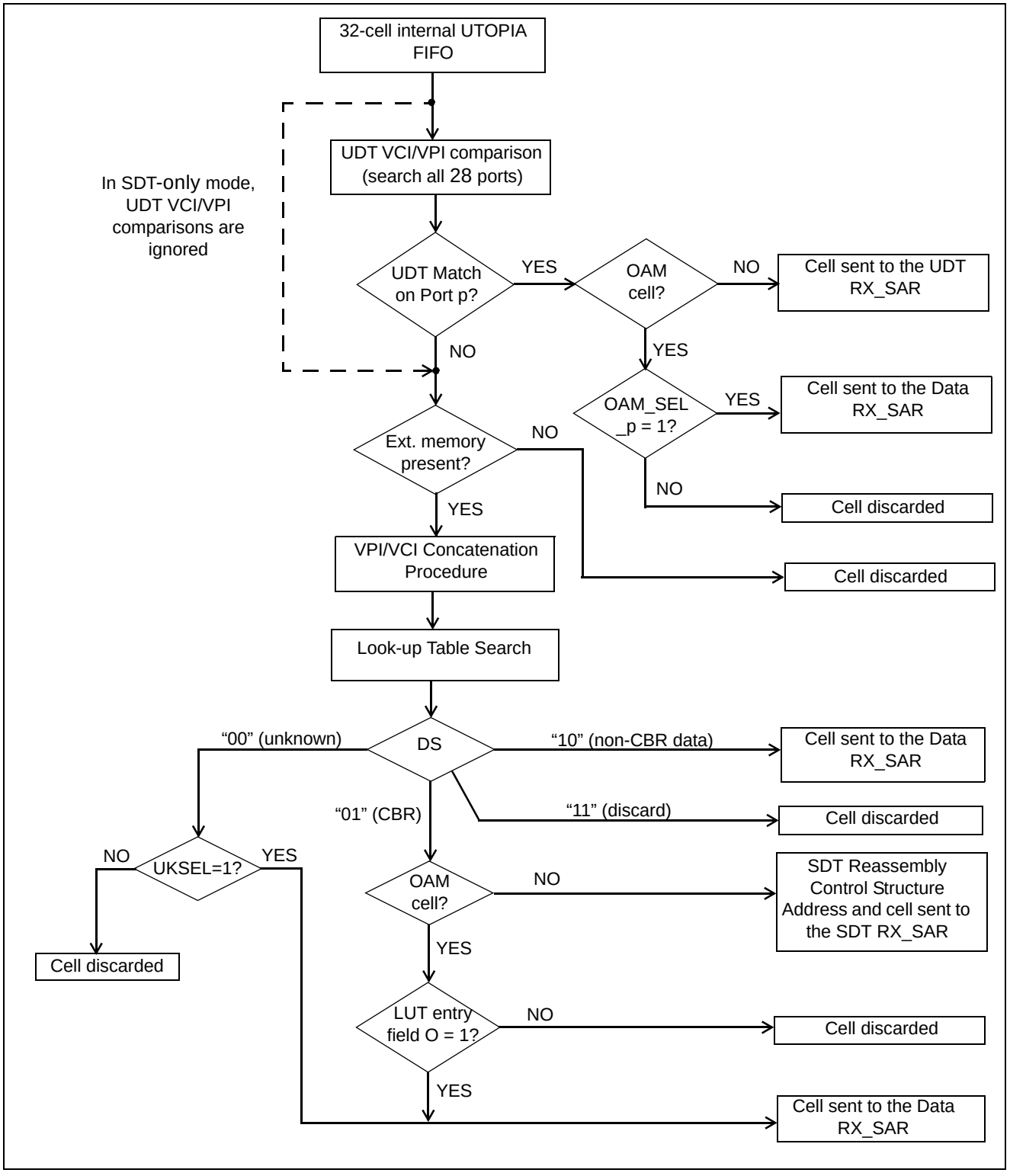


Figure 18 - Overview of the UDT VCI/VPI Comparison and Look-up Table Filtering Process

4.5 TX_SAR Module

The TX_SAR modules of the MT90528 device (consisting of the CBR-handling TX_SAR and the non-CBR Data TX_SAR) are primarily responsible for organizing TDM data into ATM cells. Since the cells contain constant-bit-rate traffic, they must be assembled at a rate which is synchronized to the 28 plesiochronous TDM ports.

The TX_SAR generates AAL1 cells which may contain TDM data and CAS signalling information. In both the UDT and SDT modes of operation, the TX_SAR is capable of inserting SRTS clock recovery information into outgoing cells.

A secondary Data TX_SAR transfers non-CBR cells from a CPU-accessible cell buffer in external memory to the UTOPIA interface for transfer onto the ATM network.

4.5.1 ATM Overview

As mentioned above, the TX_SAR is responsible for the generation of AAL1 cells, in accordance with the formats set out in ITU-T I.363.1. There are two basic cell formats which are used in AAL1 systems: cells with pointers (used only in the Structured Data Transfer mode of operation) and cells without pointers (used in both the UDT and SDT modes of operation). When operating in the 8-bit UTOPIA mode of operation, AAL1 cells are 53 bytes long; when using the 16-bit UTOPIA mode of operation, AAL1 cells are 54 bytes long and feature an extra field, UDF2. The formats of the cell types are shown below in Figure 19. Note that the 46-byte or 47-byte payload in the cells may contain TDM data or CAS signalling information.

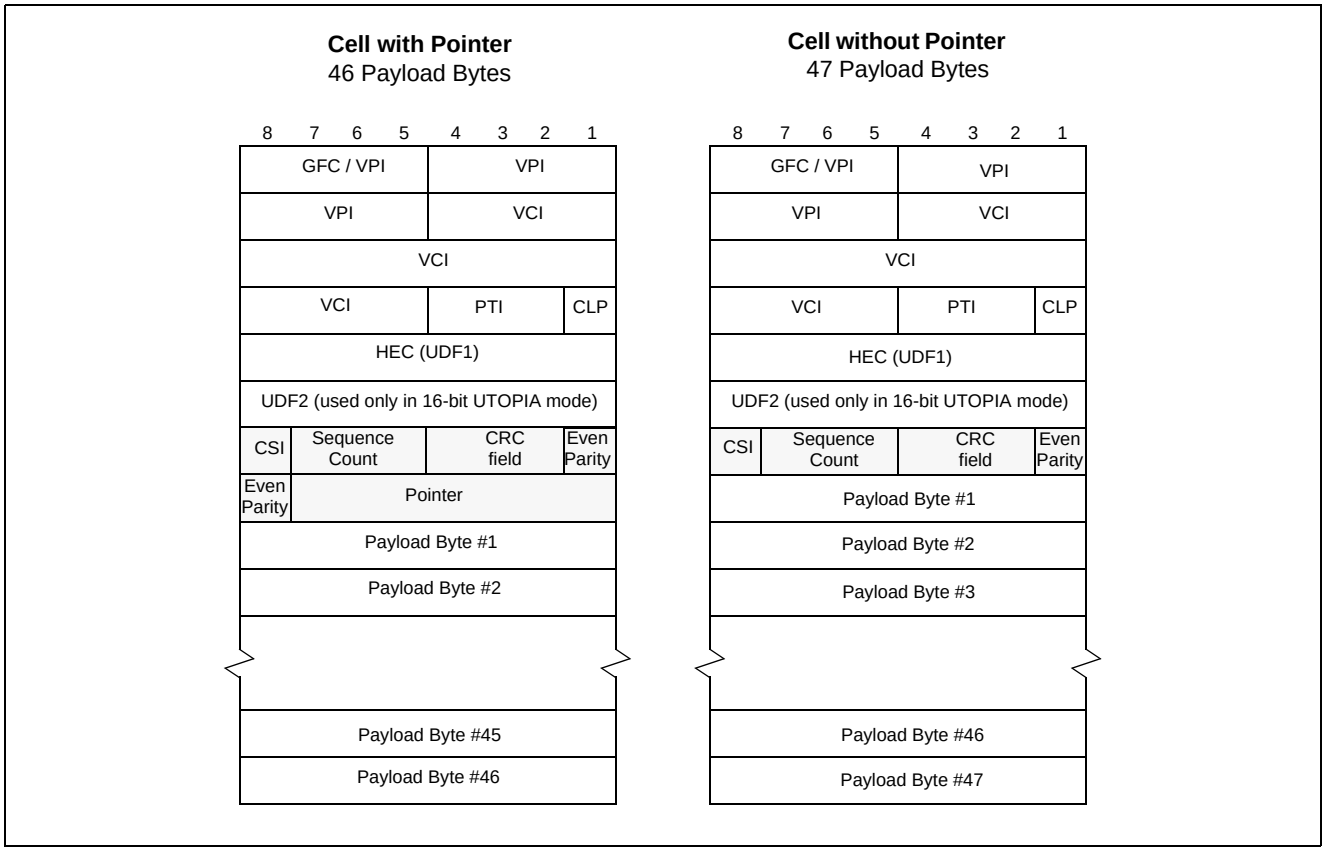


Figure 19 - AAL1 ATM Cell Formats

4.5.2 UDT Mode of Operation

In the UDT mode of operation, the TX_SAR is capable of generating and transmitting cells for 28 independent VCs, representing each of the 28 TDM ports of the MT90528 device.

4.5.2.1 Control Structure Configuration

The first step in setting up the TX_SAR for UDT operation is the configuration of a UDT Segmentation Control Structure, as shown in Figure 20.

There must be one control structure for each UDT VC that the TX_SAR is to transmit. A control structure may be located at any address within the internal memory space which is reserved for Segmentation Control Structures (starting at byte address 80000h). The TX_SAR hardware identifies the location of a particular control structure by reading the TX_SAR Pointer Table Base Register for the corresponding TDM port. These registers are located at byte addresses 1000h + p*2h, where p represents the particular port number. Within these registers, the user must configure the least-significant 14 bits to point to the word address of the start of a UDT Segmentation Control Structure in internal memory. As well, the TXCFG bits in the register must be set to “01” to indicate that the control structure being pointed to is formatted for UDT transmission.

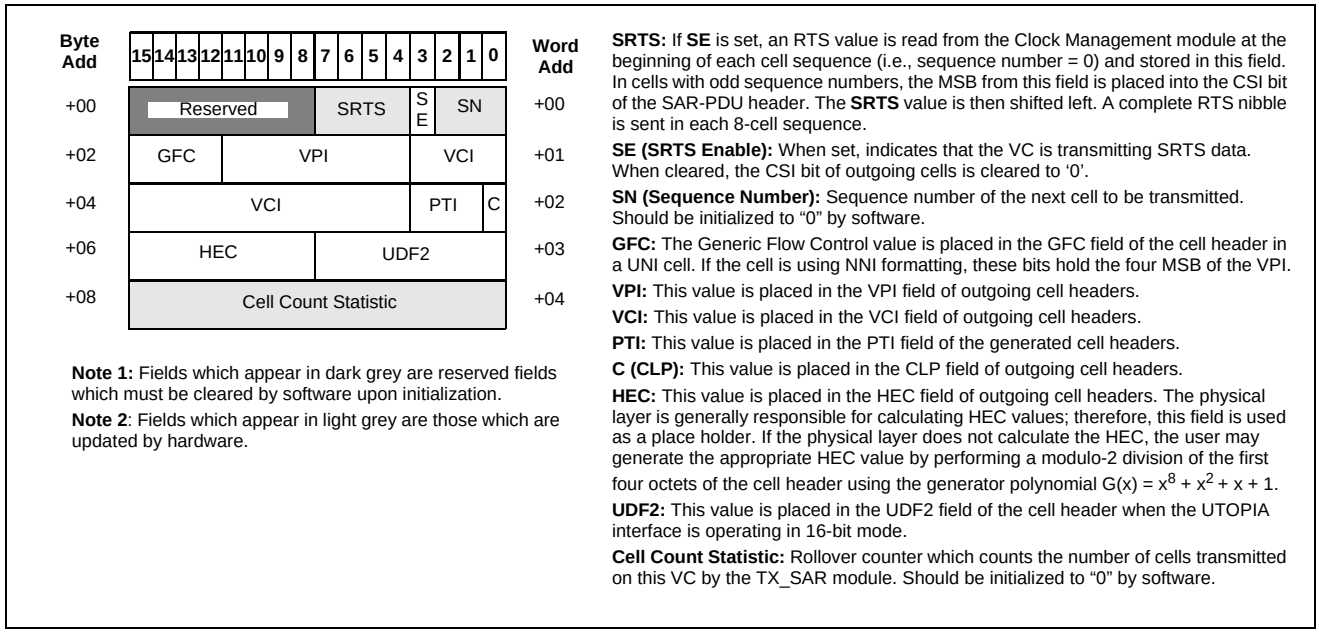


Figure 20 - Segmentation Control Structure - UDT Format

All of the fields within the control structure are explained in the text accompanying Figure 20. Upon initialization, several of the fields within the UDT Segmentation Control Structure need to be explicitly configured by the user. The **GFC**, **VPI**, and **VCI** fields must be programmed to configure the header of the outgoing cells to contain the correct routing information. The user may also program the **PTI** and **CLP** fields to configure the networking properties for the cells on the VC. Additionally, the user can configure the **HEC** and **UDF2** fields of outgoing cells. The **HEC** field is used primarily as a place-holder since PHY devices are usually responsible for the generation of header error checking values. The value contained in the **UDF2** field is only transmitted in outgoing cells if the MT90528 is using a 16-bit UTOPIA interface. If the VC is going to be carrying RTS nibbles, the **SE** bit must be set, as detailed in the figure above. The remaining fields in the control structure should be cleared upon initialization.

Once the control structure has been configured, the transmission of CBR cells can begin as soon as the TX_SAR is enabled, by setting the TXENB bit in the TX_SAR Master Enable Register at byte address 1044h.

4.5.2.2 Operation

Generally speaking, the generation of CBR cells in UDT mode is performed automatically by the TX_SAR, without any CPU intervention being required. The TDM module reads data from the TDM bus and stores it in 47-byte blocks in internal memory. When a block of memory is full, the TDM module sends an internal flag to the TX_SAR module, indicating that it is time to generate a cell. The TX_SAR prepends the 47-byte block of data with an AAL1 header byte consisting of an in-order sequence number and related protection fields. The resulting 48-byte block is then prepended with the 6-byte ATM cell header as configured via the fields in the UDT Segmentation Control Structure for the VC. The complete cells are then transferred to the UTOPIA module for transmission onto the ATM network.

Figure 21 below shows the complete segmentation data path in UDT mode, from the incoming TDM data bus to the outgoing UTOPIA data bus.

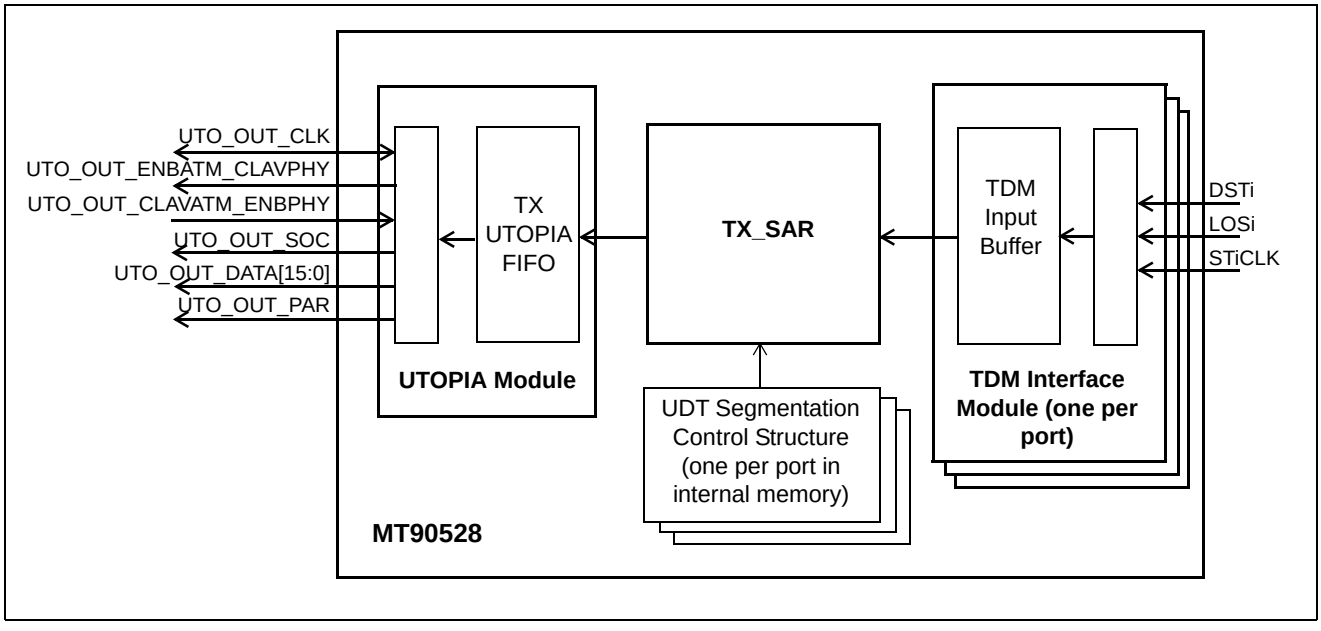


Figure 21 - Overview of CBR Data Segmentation Process (UDT Mode)

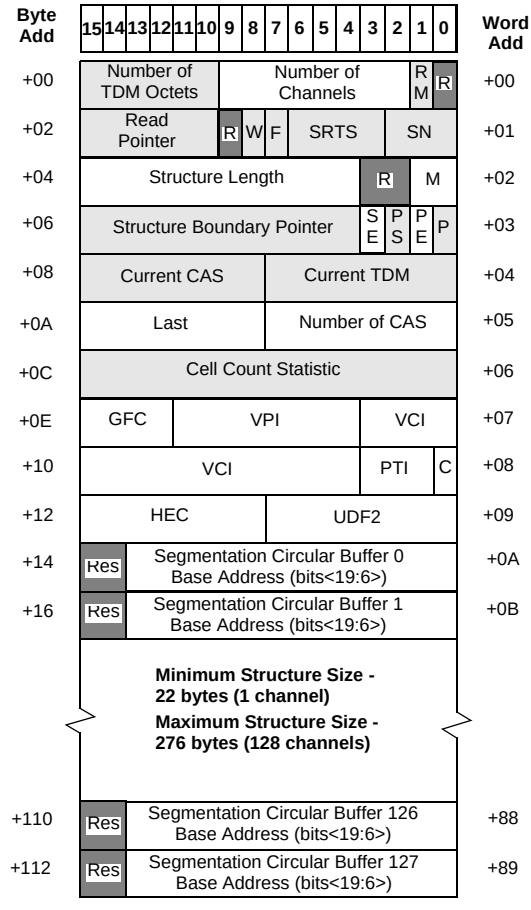
4.5.3 SDT Mode of Operation

In the SDT mode of operation, the TX_SAR is capable of generating cells on multiple VCs, independent of the originating port on which the TDM data to be transmitted was received. Specifically, the TX_SAR is capable of generating cells for a maximum of 896 different VCs (the equivalent of 32 VCs originating from each of the TDM ports) in SDT mode. Unlike UDT mode, a single SDT VC does not need to transmit all of the data from a particular port. Instead, VCs can contain various combinations of channels, ranging from N=1 VCs to VCs carrying up to 128 channels, in accordance with the af-vtoa-0089.000 standard for AAL1 narrowband trunking.

4.5.3.1 Control Structure Configuration

SDT Segmentation Control Structures

There must be one control structure for each SDT VC that the TX_SAR is to transmit. The format for the SDT Segmentation Control Structures is shown in Figure 22. SDT control structures may be located at any address within the internal memory space (starting at byte address 80000h) which is reserved for Segmentation Control Structures.



Note 1: Fields which appear in dark grey are reserved fields which must be cleared by software upon initialization.

Note 2: Fields which appear in light grey are those which are updated by hardware.

Number of TDM Octets: Indicates the number of TDM octets required to fill the next cell of the corresponding VC. Initialize to 47d.

Number of Channels: Indicates the number of TDM channels in the VC associated with this control structure (possible values = 1d to 128d).

RM (Remainder): When set, this bit indicates that there is enough TDM data to create more than one cell in the current frame. Initialize to '0'.

Read Pointer: This value represents the location in the circular buffers from which the next TDM value will be read. Should generally be initialized to "0", but if the chip is supporting a large number of VCs, this field may be used to distribute cell generation over more than 1 frame. See "Read Pointer Field" on page 62 for more details.

W (Wait for Multiframe): When set, the TX_SAR module waits for the multiframe boundary to produce the first cell (seq. num = 0; pointer = 0).

F (First Cell): If set, indicates that the next cell is the first one to be sent for the current VC. Should be initialized to '1', except if the **Read Pointer** is used to scatter the cell generation over multiple frames (this bit should then be cleared).

SRTS: If **SE** is set, an SRTS value is read from the Clock Management module at the beginning of each cell sequence (SN = 0) and stored in this field. In cells with odd sequence numbers, the MSB from this field is placed into the CSI bit of the SAR-PDU header. The **SRTS** value is then shifted left.

SN (Sequence Number): Holds the sequence number of the next cell to be generated. Must be initialized to "0".

Structure Length: This field contains the length of the multiframe structure (payload substructure + signalling substructure). For non-CAS VCs, this field should be initialized to **Number of Channels**. For CAS VCs, this field = (**Number of Channels**)*m + roundup(**Number of Channels**/2) where m=24 for DS1 and 16 for E1.

M (Mode): "01" = (DS1 with CAS and **Number of Channels** = 1); "10" = (E1 with CAS and **Number of Channels** = 1); "11" = (E1 with CAS and **Number of Channels** = 2); "00" = all other cases.

Structure Boundary Pointer: Indicates the distance, in octets, between the last payload byte written and the next structure boundary. Initialize to "0".

SE (SRTS Enable): When set, indicates that the VC is transmitting SRTS data. When cleared, the CSI bit of outgoing odd-numbered cells is set to '0'. Only one VC per port may carry SRTS information.

PS (Pointer Sent): Used to ensure that only a single pointer cell is sent within an eight-cell sequence. Initialize to '0'.

PE (Pointer Enable): When set, a pointer cell will be generated once per 8-cell sequence. This bit must be cleared to '0' for single-channel VCs not transporting CAS, but set in all other cases.

P (Pointer Cell): Indicates that the next cell to be produced will be a pointer cell. Should be initialized to the same value as the **PE** bit.

Current CAS: When transporting CAS, this field is used to keep track of which circular buffer pointer to read next. Must be initialized to 0Ah.

Current TDM: Used to keep track of which circular buffer pointer to read next. Must be initialized to 0Ah.

Last: Contains the address (relative to word 0) of the last valid **Segmentation Circular Buffer Base Address** in the control structure. The formula for this field is: 09h + **Number of Channels**.

Number of CAS: Contains the size, in octets, of the signalling substructure. If CAS is not being transmitted, this field should be initialized to "0". Otherwise, the formula is: roundup(**Number of Channels**/2).

Cell Count Statistic: Rollover counter which counts the number of cells transmitted on this VC by the TX_SAR module. Initialize to "0".

GFC: The Generic Flow Control value is placed in the GFC field of cell headers in a UNI cell. If the cell is using NNI formatting, these bits hold the four MSBs of the VPI.

VPI: This value is placed in the VPI field of outgoing cell headers.

VCI: This value is placed in the VCI field of the generated cell headers.

PTI: This value is placed in the PTI field of outgoing cell headers.

C (CLP): This value is placed in the CLP field of the cell headers.

HEC: This value is placed in the HEC (UDF1) field of outgoing cell headers. The physical layer is generally responsible for calculating HEC values; therefore, this field is used as a place holder. If the physical layer does not calculate the HEC, the user may generate the appropriate HEC value by performing a modulo-2 division of the first four octets of the cell header using the generator polynomial $G(x) = x^8 + x^2 + x + 1$.

UDF2: This value is placed in the UDF2 field of the cell header when the UTOPIA is operating in 16-bit mode.

Segmentation Circular Buffer X Base Address: The bits of this field are concatenated with the **Read Pointer** bits to form a 20-bit **word** address to external memory. This value is used to address a particular TDM or CAS value in a particular buffer. One pointer is needed for each channel in the VC.

Figure 22 - Segmentation Control Structure - SDT Format

In general, Figure 22 should be referred to for explicit details regarding the initialization of the fields within the SDT Segmentation Control Structures. However, one field needs more explanation, which is provided in the following text:

Read Pointer Field

When operating in SDT mode, each VC has an associated read pointer, which is configured within the VC's Segmentation Control Structure. This value, as described in the text accompanying Figure 22, is used by the TX_SAR to determine the location within the Segmentation Circular Buffers from which the next byte of TDM data will be read. In general, this field should be initialized to “0”, so that the TX_SAR reads the first data byte that was written into the buffer by the TDM module. However, in the case of a large number of VCs with small N, the read pointer value can be used to ease the job of the TX_SAR by distributing the cell generation over more than one frame. When the read pointer is used to scatter the cell generation, the F (First) bit of the Segmentation Control Structure should be set to ‘0’.

For example, when N=1 VCs are used, it is possible for the MT90528 to handle up to 896 VCs simultaneously. In this case, each VC only needs to be serviced once every 47 frames (once enough data from the TDM channel has been received to complete an ATM cell). Ideally, the Segmentation Control Structures should be configured to distribute cell generation so that the TX_SAR does not sit idle for 46 frames, and then try to create up to 896 cells in the 47th frame. In order to eliminate this burstiness problem (and the resulting negative impact on the CDV), the read pointer for each VC can be set to a non-zero value. For example:

VC_0 read pointer = 0

VC_1 read pointer = 1

...

VC_46 read pointer = 46

VC_47 read pointer = 0

...

By setting the read pointers of various VCs to different values, the user ensures that the TX_SAR will not be required to generate all of the cells simultaneously. For example, in frame 47, rather than having to generate 896 cells, the TX_SAR will only have to generate 20 cells (from VCs numbered 0, 47, 94, 141, 188, 235, 282, 329, 376, 423, 470, 517, 564, 611, 658, 705, 752, 799, 846, 893).

Therefore, when configuring the MT90528 to handle many VCs with low N values, it is recommended that the read pointers be distributed over multiple frames.

SDT Segmentation Pointer Tables

After writing control structures into internal memory, software must configure a pointer table in the same block of internal memory (i.e., between addresses 80000h and 87FFEh) to permit the TX_SAR hardware to locate the control structures. An SDT Segmentation Pointer Table must be created on a per-port basis for all ports which are configured to transmit SDT ATM cells. The table conforms to the format shown in Figure 23 and must start on a 32-word (64-byte) boundary. There can be up to 32 entries in each table, as there can be a maximum of 32 N=1 VCs associated with any one TDM port. Each entry in the pointer table contains a field which gives the **word** address of the SDT Segmentation Control Structure associated with a particular VC. Two extra bits in the pointer table entry indicate whether the corresponding control structure is enabled, as well as whether this is the final control structure pointer contained in the table.

For VCs transmitting channels from multiple ports, any one of the ports’ SDT Pointer Table can be chosen to contain the VC entries. If any SDT Pointer Table entry points to a VC having more than 46 channels, the TDM_DATA_FORMAT field of the corresponding TDM port’s TDM1 register must be programmed as “11”.

The per-port TX_SAR Pointer Table Base Registers (at byte addresses 1000h + p*2h) must be configured to point to the SDT Segmentation Pointer Tables for their respective ports. As well, the TXCFG bits in the register must be set to “11”, indicating that the control structures being pointed to by the table are configured for SDT mode.

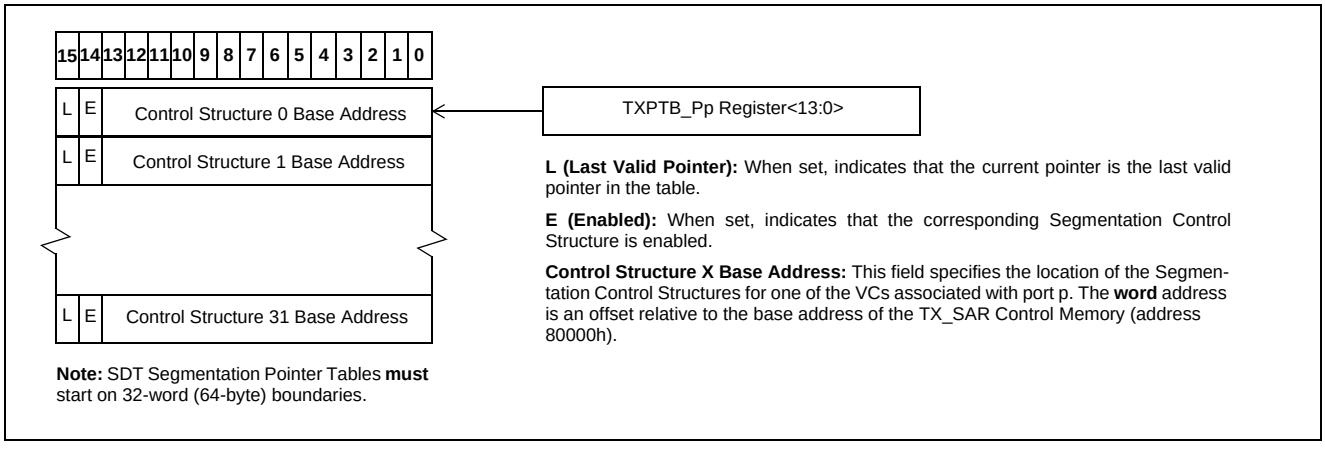


Figure 23 - SDT Segmentation Pointer Table for Port p

Once the control structures and accompanying pointer tables have been configured, the transmission of CBR cells can begin as soon as the TX_SAR is enabled, by setting the TXENB bit in the TX_SAR Master Enable Register at byte address 1044h.

4.5.3.2 Operation

In SDT mode, once the SDT Segmentation Control Structure has been configured and the TX_SAR enabled, the TX_SAR begins to generate cells with the appropriate formatting, without further software intervention. The TX_SAR reads data (consisting of TDM data bytes and, where appropriate, CAS signalling bytes) from the per-channel SDT Segmentation Circular Buffers in external memory. Refer to Section and Figure 11, “Per-Port SDT Segmentation Circular Buffers,” on page 43 for details regarding the formatting of the data which is written to these circular buffers by the TDM module. The TX_SAR prepends the TDM data with an AAL1 sequence number and with a 6-byte header as specified by the VC’s SDT Segmentation Control Structure. Additionally, as defined in the AAL1 specifications, one even-numbered cell out of each eight-cell sequence contains a pointer byte. The TX_SAR uses internal counters to determine the appropriate value for the pointer byte, which indicates the start of the next structure within the outgoing cell stream on a VC.

Figure 24 shows the complete segmentation data path in SDT mode, from the incoming TDM data bus to the outgoing UTOPIA data bus.

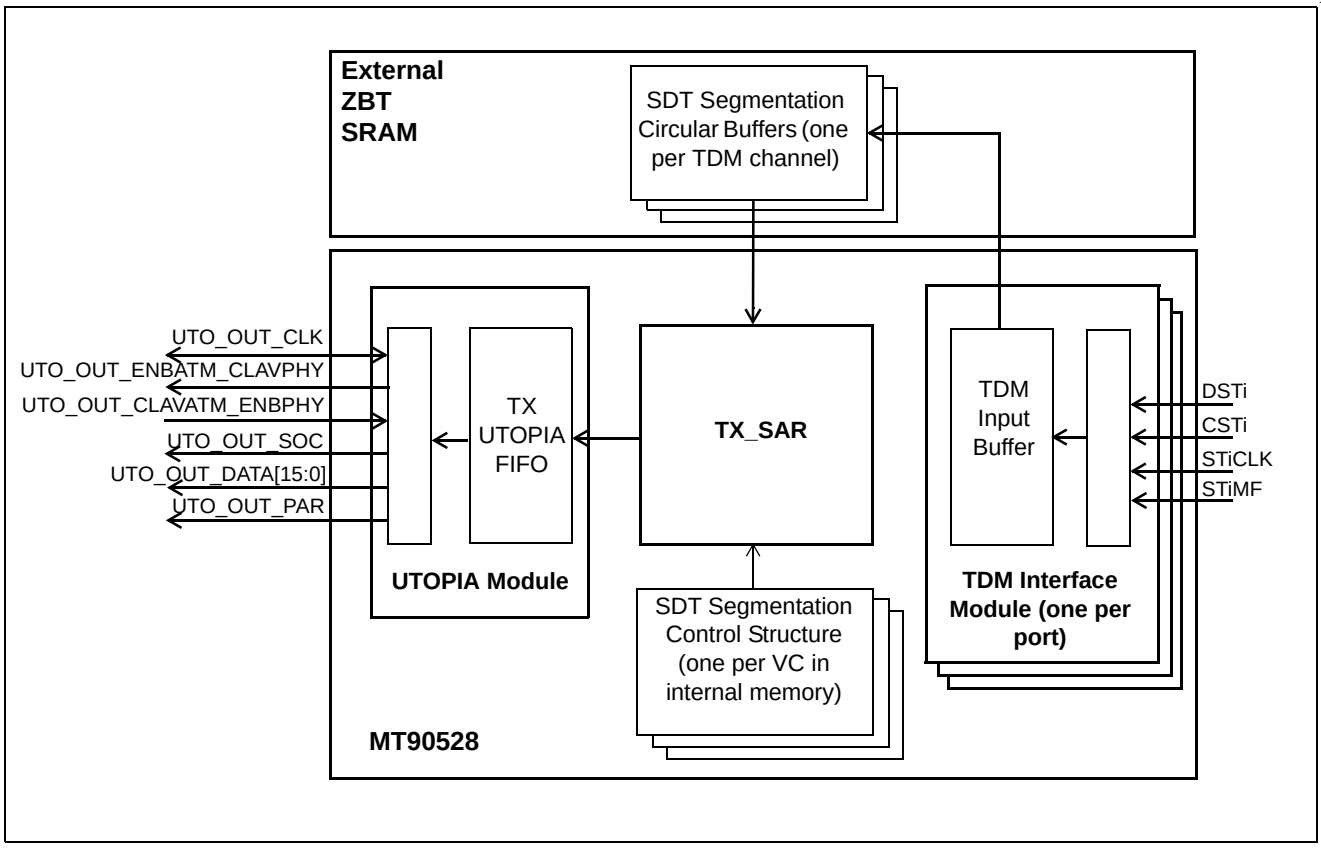


Figure 24 - Overview of CBR Data Segmentation Process (SDT Mode)

4.5.4 Data TX_SAR Module

The TX_SAR (and specifically the sub-module which shall henceforth be called the Data TX_SAR) is capable of transmitting non-CBR data cells which are not associated with any TDM port. These cells may be AAL5 signalling cells, OAM-type data cells, or any other ATM cells which need to be transmitted from a system containing an MT90528 device.

The Data TX_SAR does not process or manipulate the data cells. Rather, it simply reads cells which have been written to a multi-cell circular buffer in external memory by a CPU. It then transfers those cells to the UTOPIA module for transmission onto the UTOPIA bus.

The Data TX_SAR can operate simultaneously with the generation of AAL1 CBR cells by the TX_SAR.

4.5.4.1 Mode of Operation

The Data TX_SAR within the MT90528 must be enabled, by setting the **Data TX_SAR Enable** bit in the Data TX_SAR Control Register at address 103Eh.

The user writes the cells to a buffer located in external memory. The address and size of this buffer are programmed in the DTCON register, located at address 1038h. The cell structure format is illustrated in Figure 25.

When the Data TX_SAR is enabled, it begins to send cells from the cell buffer beginning with the cell pointed to by the Data TX_SAR Read Pointer. The Read Pointer is incremented after each cell is sent. Cell transmission halts when the Read Pointer is equal to the user-defined Data TX_SAR Write Pointer, which indicates the cell structure number being written to by the CPU. Cell transmission begins again after the Write Pointer is changed to a different value than the Read Pointer. The cell buffer is circular; the Read Pointer will never point above the top of the buffer.

A cell buffer empty event occurs whenever the Read Pointer equals the Write Pointer. This condition is cleared when the Data TX_SAR is disabled or when the Write Pointer is changed.

If the Write Pointer is set to a value equal to or greater than the cell buffer size, the cells in the buffer will be sent repetitively.

The Write Pointer should never be set to the same value as the Read Pointer when there are cells in the buffer awaiting transmission or during transmission of the cell pointed to by the Read Pointer.

If the AUTO bit is set in the Data TX_SAR Control Register at 103Eh, the Data TX_SAR sends cells to the UTOPIA module whenever the TX_SAR module is not busy transmitting CBR cells (i.e., either UDT- or SDT-formatted AAL1 cells). Contrarily, if the AUTO bit is not set, the Data TX_SAR sends out cells at a user-configurable data rate. The user may configure the time between cell transmissions by programming the Data Cell Generation Time Out Register at 1040h. Cells may be sent in time intervals from 1ms to 1s.

As mentioned above, the Data TX_SAR does not actually generate the cells to be transmitted. Rather, it simply reads 54-byte cells (consisting of 5 bytes of header, 1 “filler” header byte (UDF2 field) required for the 16-bit UTOPIA bus, and 48 bytes of payload) directly from a location in external memory which is identified by a Data TX_SAR Cell Buffer base address and the Read Pointer. The base address of the buffer is user-programmable, as is the number of cells that can be stored in the buffer. The user can select (via the register at byte address 1038h) a buffer capable of holding 16, 32, 64, or 128 cells. Each cell is allocated 64 bytes in external memory. Cells written into the Data TX_SAR Cell Buffer must conform to the format shown in Figure 25.

4.5.4.2 Error Handling

The Data TX_SAR has a single status bit to indicate whether the Data TX_SAR Cell Buffer in external memory is empty (declared when the Data TX_SAR’s read pointer is equal to the write pointer controlled by the CPU). The **Transmit Cell Buffer Empty** bit in the Data TX_SAR Status Register at 1042h can be enabled to cause an interrupt to be generated on $\overline{\text{IRQ}}$.

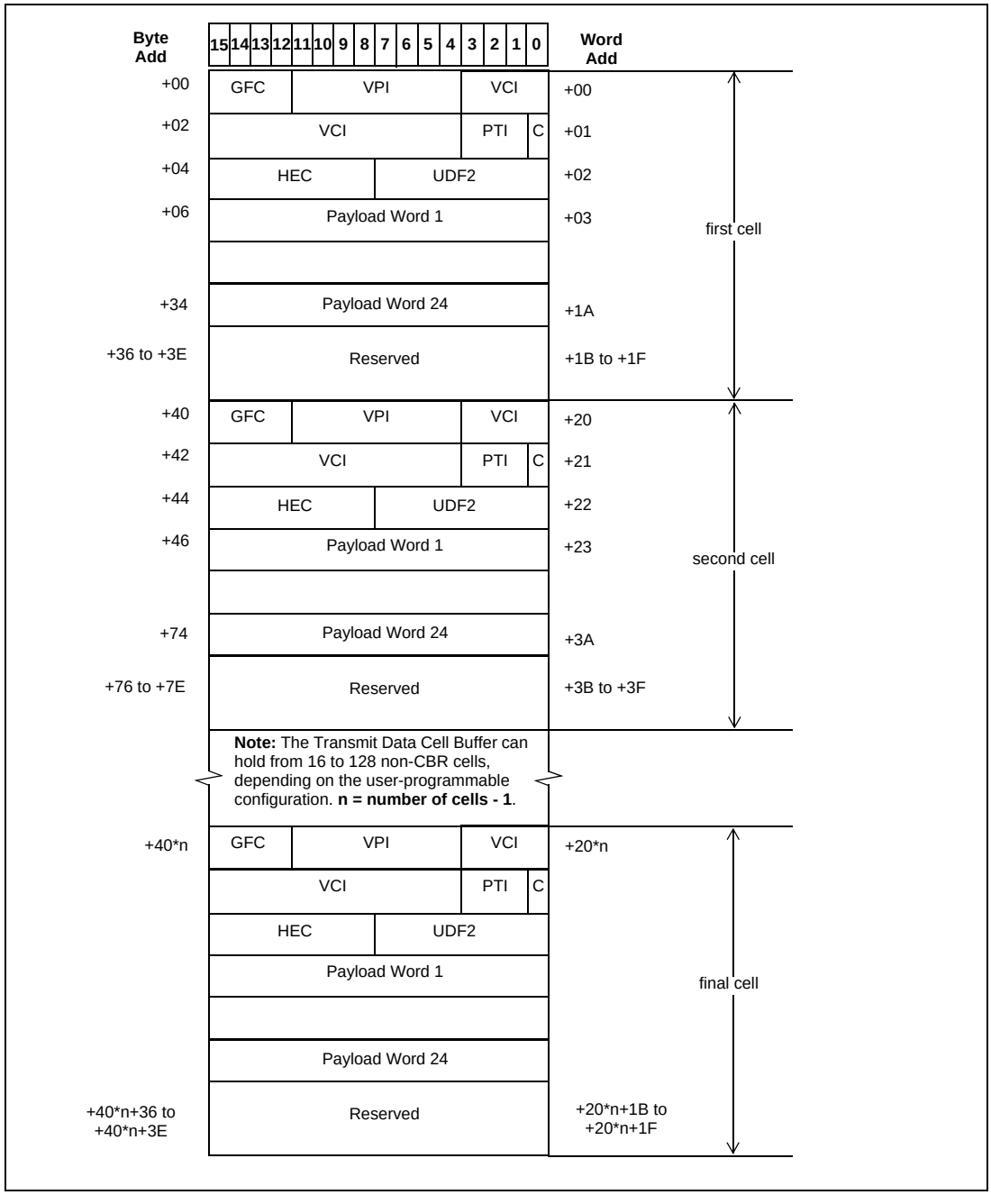


Figure 25 - TX_SAR Cell Template - Data Cell (Non-CBR) Mode

4.6 RX_SAR Modules

The RX_SAR modules of the MT90528 device (consisting of the UDT RX_SAR, the SDT RX_SAR, and the Data RX_SAR) are primarily responsible for the reassembly of TDM data extracted from CBR ATM cells. In addition, in certain modes of operation, the SDT RX_SAR extracts CAS data from received cells and sends that information, as well as multiframe indication signals, to the TDM module.

The UDT RX_SAR and SDT RX_SAR modules provide the Clock Management module with clocking information obtained from received cells.

A secondary Data RX_SAR transfers non-CBR cells from the UTOPIA interface to external memory, where the cells may be processed by user software.

4.6.1 UDT RX_SAR and SDT RX_SAR Modules

4.6.1.1 Data Flow and Processing Path Overview

At a high level of abstraction, Figure 26 shows the functionality implemented within the UDT RX_SAR and SDT RX_SAR reassembly paths of the MT90528. Within the “ATM Cell Processing” path there are a number of different steps which must be taken, depending upon the operating mode of the device. The “Clock Recovery Operations” and “MIB Statistics Gathering” paths may be taken in conjunction with any of the operating modes.

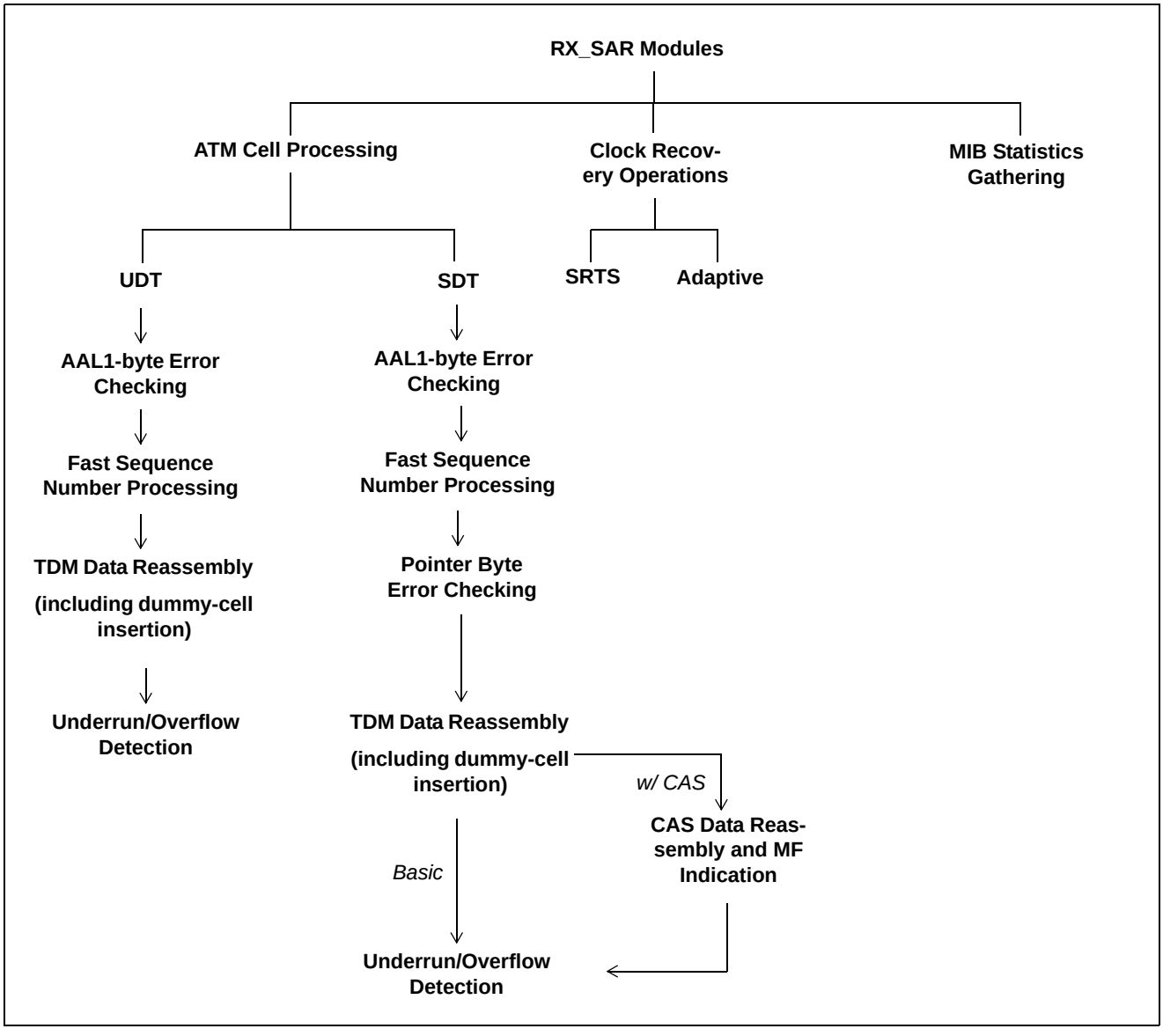


Figure 26 - High-Level Overview of the Functionality of the RX_SAR Module

The UDT RX_SAR and SDT RX_SAR modules are explained in the following sections.

In Section 4.6.1.2, the use of Reassembly Control Structures is detailed. These control structures, which are stored in internal memory, control the operation of the UDT RX_SAR and the SDT RX_SAR on a per-VC basis.

The flow of the documentation starting in Section 4.6.1.3 on page 72 generally follows the flow of received cells through the data path shown in Figure 26.

4.6.1.2 Reassembly Control Structures

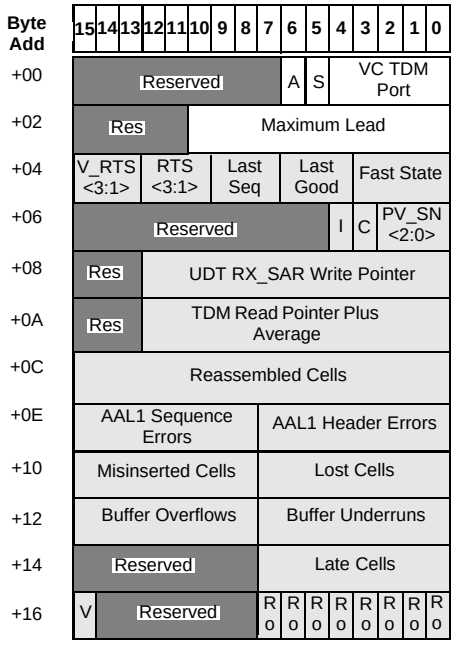
The UDT RX_SAR and the SDT RX_SAR are both instantiated only once per MT90528 device. As a result, each module must handle all of the cells being received at the device in a particular mode of operation. However, due to the nature of the device, it is possible for multiple cell streams (i.e., cells being carried on different VCs) to be received at the MT90528's UTOPIA receive interface and then sent for processing by one of the RX_SARs. In order to keep statistics and other information (e.g., current state of the Correction/Detection state machine, last received sequence number) updated on a per-VC basis, the MT90528 employs two internal memories (one each for the UDT RX_SAR and the SDT RX_SAR) to hold Reassembly Control Structures. The user must configure a control structure for each VC which is receiving cells via the MT90528.

UDT Reassembly Control Structures

Within the UDT RX_SAR, there is an internal memory which can be configured to hold up to 28 UDT Reassembly Control Structures (one per port). Each UDT Reassembly Control Structure is allocated a 32-byte block. The control structures for the various ports must be located at pre-defined locations within the internal memory. If the data on a VC is destined for port 0, the UDT Reassembly Control Structure for the VC must be programmed to begin at CPU byte-address BE000h (the base address for the UDT Reassembly Control Structure memory in the MT90528 memory map). The control structure for a VC destined for port 1 must be configured to start at CPU byte-address BE020h, and so on.

All of the fields within the control structure are explained in the text accompanying Figure 27. Upon initialization, only a few of the fields within the UDT Reassembly Control Structure need to be explicitly configured by the user. **VC TDM Port** must be configured to match the desired destination port for the VC's data. As such, the only permissible values for this field are "00000" (representing port 0) to "11011" (representing port 27). If SRTS or Adaptive clock recovery methods are to be employed on the VC, the appropriate configuration bit (either **S** or **A**) must be set. As well, the **Maximum Lead** field must be configured to a value which accounts for the expected cell delay variation (CDV) of the network, and the desired distance to be maintained between the UDT RX_SAR's write pointer and the TDM module's read pointer. More details regarding the programming of Maximum Lead are given within the section "UDT Reassembly Circular Buffers" on page 79. All of the remaining fields within the UDT Reassembly Control Structure must be cleared to '0' upon initialization. This ensures that the statistics and status fields for the VC are configured to start with cleared values.

For debug and statistics-gathering purposes, the CPU can read the UDT Reassembly Control Structure contents.



Note 1: Fields which appear in dark grey are reserved fields which must be cleared by software upon initialization.

Note 2: Fields which appear in grey are those which are updated by hardware.

Note 3: UDT Reassembly Control Structures **must** always start on 16-word (32-byte) boundaries.

A (Adaptive Enable): If set, the fill-level of the UDT Reassembly Circular Buffer associated with this VC is used to provide adaptive clocking information for the TDM port.

S (SRTS Enable): If set, this VC is carrying RTS clocking information for the TDM port.

VC TDM Port: Identifies the TDM port (0 to 27) with which this VC is associated. Must correspond to the location of this control structure within the internal memory.

Maximum Lead: Maximum allowable distance between the TDM Read Pointer and the UDT RX_SAR Write Pointer within the UDT Reassembly Circular Buffer.

V_RTS<3:1> (RTS Validity): Bits indicating whether the individual bits in RTS<3:1> are valid and can therefore be used by the PLL for clock recovery processing.

RTS<3:1>: Intermediate RTS value used by the clock recovery circuit.

Last Seq (Last Sequence Number): This state variable keeps track of the last sequence number received by the Fast SN Processing state machine.

Last Good (Last Good Sequence Number): This state variable keeps track of the last valid or in-sequence sequence number received by the Fast SN Processing SM.

Fast State: Indicates which state the Fast Sequence Number Processing SM will enter upon the arrival of the next cell from this VC.

I (Initialized): '0' = VC uninitialized; '1' = VC initialized. **Must be initialized to '0' by software**.

C (Next CD State): Indicates which state the Correction/Detection SM will enter upon the arrival of the next cell from this VC. **Must be initialized to'0' (Correction)**.

PV_SN<2:0> (Previous Valid Sequence Number): Sequence number of the last valid, in-sync cell received by the SRTS circuitry.

UDT RX_SAR Write Pointer: Indicates which location will next be written to within the UDT Reassembly Circular Buffer in internal memory.

TDM Read Pointer Plus Average: This **read-only** field contains the value of the TDM Read Pointer plus average lead. **Unless an underrun has been reported, this field is cleared to zero**.

MIB Statistics: AAL1 Sequence Errors, AAL1 Header Errors, Misinserted Cells, Lost Cells, Buffer Overflows, Buffer Underruns, and **Late Cells** are 8-bit fields for each MIB statistic which must be collected on a per-VC basis. **Reassembled Cells** is stored in a 16-bit field.

V (VC Arrival): This bit is set by the UDT RX_SAR each time a cell arrives on this VC. The CPU can clear it to '0' to provide per-VC timeout monitoring.

Ro: Status bits which indicate rollovers on MIB status fields. The eight rollover bits correspond to the order of the MIB statistics fields in the control structure: bit<0> = Reassembled Cell Rollover, bit<1> = AAL1 Header Errors Rollover, etc.

Figure 27 - Reassembly Control Structure - UDT Format

SDT Reassembly Control Structures

Within the SDT RX_SAR, there is an internal memory which is 16 Kwords long and 16 bits wide, to permit the setup of VCs of varying size and configuration. The MT90528 can handle up to 896 single-channel VCs (a full E1 of 32 channels on each of the 28 ports). Such a configuration uses the maximum internal memory resources (maximum overhead is required for each "n=1" VC). However, many other configurations with different "n" are also permissible.

Unlike the control structures in UDT mode, SDT Reassembly Control Structures do not have as many restrictions on their location. Although all of the SDT control structures must start on 32-byte (16-word) boundaries, the boundary which is selected for each control structure does not matter (e.g., the control structure for a VC on port 5 may be physically located in memory at an earlier location than the control structure for a VC on port 0). As well, it is possible for a VC to be carrying data which is destined for multiple TDM ports (e.g., Channel 0 of the VC may be destined for port 0, but channel 1 might be destined for port 27). The TDM port destination of the data is ultimately determined by the programming of the TDM SDT Reassembly Control Structure (see Figure 13 on page 46). It is important to note that the location of the SDT Reassembly Control Structure in internal memory must be correlated with the Reassembly Control Structure Address within the UTOPIA's look-up table entry for the particular VC.

When a VC is configured as basic SDT, the control structure uses from 30 bytes to 284 bytes, depending on the number of channels carried by the VC (up to 128). The various fields of the SDT Reassembly Control Structure are shown in Figure 28 and explained in Table .

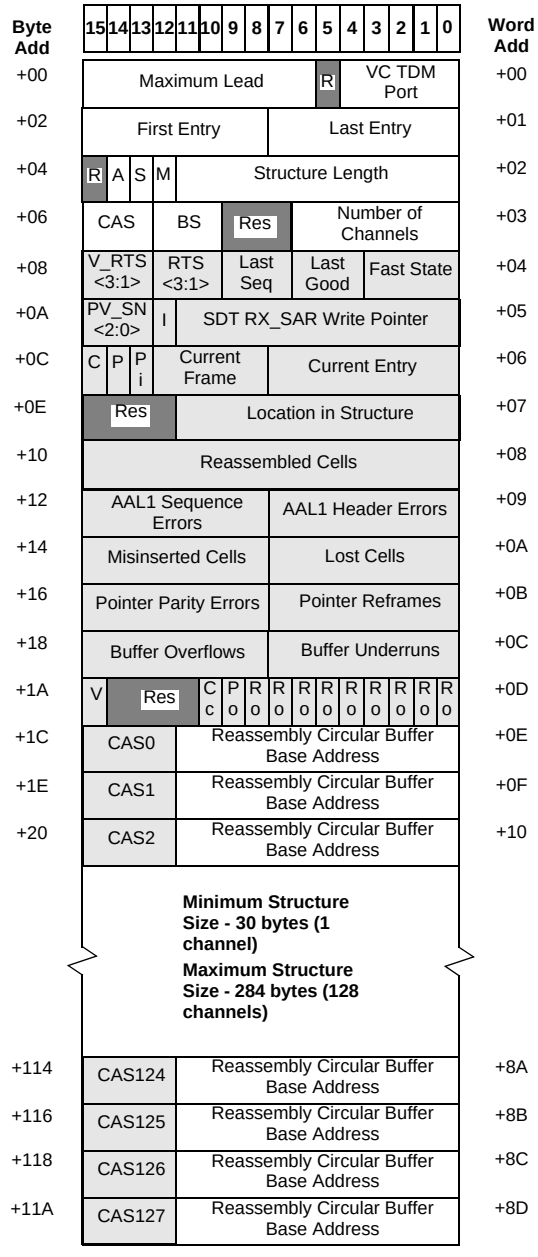
For debug and statistics-gathering purposes, the CPU can read the SDT Reassembly Control Structure contents, one word at a time.

SDT Control Structure Fields - Initialization

As in the UDT case, upon initialization, only a few of the fields within the SDT Reassembly Control Structure need to be explicitly configured by the user. The fields which must be configured are listed below. Details of the appropriate values for configuration can be found in Table on page 71.

- **Maximum Lead** must be configured to a value which accounts for the expected CDV of the network, and the desired distance to be maintained between the SDT RX_SAR's write pointer and the TDM module's read pointer. More details regarding the programming of Maximum Lead are given within the section "SDT Reassembly Circular Buffers" on page 82.
- If all of the data within the VC is destined for the same TDM port, **VC TDM Port** must be configured to match the desired destination port for the VC's data. However, if the data is destined for multiple ports (trunking), this field must be configured to match the port whose TDM read pointer will be used for slip-checking and clock recovery.
- **First Entry** must always be set to 0Eh. **Last Entry** must be programmed to the word-address of the last Reassembly Circular Buffer Base Address within the control structure.
- If SRTS or Adaptive clock recovery methods are to be employed on this VC, the appropriate configuration bit (either **S** or **A**) must be set.
- The **M (Multiframe Type)** bit is used to select either DS1 ('0') or E1 ('1') multiframing format for use when the VC is carrying CAS signalling bits. If "basic" SDT mode is being used, the value of this field does not matter.
- **Structure Length** must contain the length (less one) of the AAL1 structure size for this VC, including both TDM and CAS bytes.
- The **CAS** field must be configured if the VC being received is carrying CAS signalling nibbles.
- The **BS** field should be set to the desired size of the SDT Reassembly Circular Buffers for the VC. The configurable buffer sizes range from 64 entries to 1024 entries per channel. Note that all of the channels within the VC are allocated the same size buffers in external memory. It should also be noted that the size of the buffers must correspond to the size field given within the TDM SDT Reassembly Control Structure for the chosen TDM channel destination (port and channel specific), as shown in Figure 13 on page 46.
- **Number of Channels** must be set to the number of channels in the VC, less one (therefore, allowable values for the field are 00h to 7Fh).
- The **Pi (Pointer Initialization)** bit within the SDT Reassembly Control Structure **must** be set to '1', indicating that the control structure is ready to start receiving pointers.
- **Current Entry** must be programmed to contain the value in the First Entry field (i.e., 0Eh).
- The **Reassembly Circular Buffer Base Address** fields must contain the values of the word-addresses of the corresponding circular buffers in external memory. A two-bit value, the Reassembly Circular Buffer Base Address, is obtained from the CB_BASE_ADD field of the SDT Reassembly Control Register at byte-address 2040h. These bits form the two most significant bits of a word-address formed by concatenating these bits with the 12-bit value obtained from the Reassembly Circular Buffer Base Address. Which bits of the concatenated address are used to form the actual address to external memory is determined by the size of the buffers selected for the VC. For details regarding how these addresses are formed, See "SDT Reassembly Circular Buffers" on page 82., particularly Table 19. It should be noted that the Reassembly Circular Buffer Base Address must correspond to the address given within the TDM SDT Reassembly Control Structure for the chosen TDM channel destination (port and channel specific), as shown in Figure 13 on page 46.
- The **CASx** field for each channel in the VC (where **x** represents the channel within the VC) should be cleared if the VC is not carrying CAS. However, if the VC is programmed to receive CAS nibbles, software can configure these nibbles to contain any values desired by the user. The software-programmed values within these fields will be transferred to the TDM module (and therefore output on CSTo) until valid CAS nibbles have been extracted from received cells.

All of the remaining fields within the SDT Reassembly Control Structure **must** be cleared to '0' upon initialization. This ensures that the initialization, statistics, and status fields for the VC are configured to start with cleared values.



Note 1: Fields which appear in dark grey are reserved fields which must be cleared by software upon initialization.

Note 2: Fields which appear in grey are those which are updated by hardware.

Note 3: SDT Reassembly Control Structures **must** always start on 16-word (32-byte) boundaries.

Figure 28 - Reassembly Control Structure - SDT Format

Maximum Lead: Maximum allowable distance between the TDM Read Pointer and the SDT RX_SAR Write Pointer within a Reassembly Circular Buffer.

VC TDM Port: Identifies the TDM port (0 to 27) with which this VC is associated for slip detection and (optionally) for clock recovery.

First Entry: Indicates the location of the first Reassembly Circular Buffer Base Address within the Reassembly Control Structure. **Must be programmed to 0Eh.**

Last Entry: Indicates where the last Reassembly Circular Buffer Base Address is located within the Reassembly Control Structure. Must be programmed to have the **word**-address of the last Reassembly Circular Buffer address (e.g., if n = 2, this field contains 0Fh).

A (Adaptive Enable): If set, the fill-level of the Reassembly Circular Buffer(s) associated with this VC are used to provide adaptive clocking information for the VC TDM Port. Only one VC per TDM port can have this bit set.

S (SRTS Enable): If set, this VC is carrying RTS clocking information for the VC TDM Port. Only one VC per TDM port can have this bit set.

M (Multiframe Type): '0' = DS1 (24 frames); '1' = E1 (16 frames).

Structure Length: Indicates the length of the AAL1 structure, including TDM and CAS bytes. This field must be programmed by the user to be one less than the actual structure length. For non-CAS VCs, this field is equal to the number of channels in the VC, less one. For CAS VCs, the formula for calculating the Structure Length field is: DS1 = N*24 + roundup(N/2) - 1; E1 = N*16 + roundup(N/2) - 1.

CAS: If set, bit<0> indicates that this VC is carrying CAS information; if set, bit<1> indicates that the user wishes to control the CAS values via S/W (received CAS values not written back to control structure); if set, bit<2> indicates that a CPU service request should be sent if the new CAS value for a channel differs from the old (or if the received CAS value differs from the value set by hardware).

BS (Circular Buffer Size): "000" = 64 entries; "001" = 128 entries; "010" = 256 entries; "011" = 512 entries; "100" = 1024 entries; other = reserved.

Number of Channels: Indicates the number of channels within this VC. Field must be programmed by user to be one less than the actual number of channels in the VC (possible values = 0d to 127d).

V_RTS<3:1> (RTS Validity): Bits indicating whether the individual bits in RTS<3:1> are valid and can therefore be used by the PLL for clock recovery processing.

RTS<3:1>: Intermediate RTS value used by the Receive SRTS circuitry.

Last Seq (Last Sequence Number): This state variable keeps track of the last sequence number received by the Fast SN Processing SM.

Last Good (Last Good Sequence Number): This state variable keeps track of the last valid or in-sequence sequence number received by the Fast SN Processing SM.

Fast State: Indicates which state the Fast Sequence Number Processing state machine will enter upon the arrival of the next cell from this VC.

PV_SN<2:0> (Previous Valid Sequence Number): Sequence number of the last valid, in-sync cell received by the SRTS circuitry.

I (Initialized): '0' = VC uninitialized; '1' = VC initialized. **Must be initialized to '0' by software**.

SDT RX_SAR Write Pointer: Indicates which location will next be written within a Reassembly Circular Buffer.

C (Next CD State): Indicates which state the Correction/Detection state machine will enter upon the arrival of the next cell from this VC. **This bit must be initialized to '0' (Correction).**

P (Pointer Reframe Pending): Status bit indicating that a pointer reframe error has occurred and has yet to be compensated for or reported to the MIB. **Must be set to '0' by software.**

Pi (Pointer Initialization): Must be set to '1' by software.

Current Frame: This field indicates which frame of the multiframe is currently being received. Used only if VC is carrying CAS data.

Current Entry: Points to the address of the Reassembly Circular Buffer currently being written. **Must be initialized to 0Eh**.

Location in Structure: This field indicates how many bytes remain before the start of the next AAL1 structure. **This field must be set to '0' by software**.

MIB Statistics: AAL1 Sequence Errors, AAL1 Header Errors, Misinserted Cells, Lost Cells, Pointer Parity Errors, Pointer Reframes, Buffer Overflows, and Buffer Underruns are 8-bit fields for each MIB statistic which must be collected on a per-VC basis. **Reassembled Cells** is stored in a 16-bit field. **NOTE: The pointer reframe field will usually be incremented to '1' upon the arrival of the first valid pointer.**

V (VC Arrival): This bit is set by the SDT RX_SAR each time a cell arrives on this VC. The CPU can clear it to '0' to provide per-VC timeout monitoring.

Cc (CAS Changed): Status bit indicating that at least one CAS nibble in VC has changed since last received CAS value.

Po (Pointer Out-of-Range): Pointer out-of-range error noted if pointer-byte has an invalid value (i.e., > 93 and not a dummy value of 127).

Ro: Status bits which indicate rollovers on MIB status fields. The nine rollover bits correspond to the order of the MIB statistics fields in the control structure: bit<0> = Reassembled Cell Rollover, bit<1> = AAL1 Header Rollover, etc.

Reassembly Circular Buffer Base Address: This field forms part of the address of a Reassembly Circular Buffer. Refer to Table 19 on page 83 and the accompanying text for information regarding the addresses of SDT Reassembly Circular Buffers in external memory.

CAS0 - CAS127: Fields containing the four-bit nibbles representing the Channel Associated Signalling for the corresponding channel. These values are transmitted to the TDM module regardless of whether the received VC is configured for CAS. Must be set to initial values by software.

Table 12 - Fields within the SDT Reassembly Control Structure

4.6.1.3 Sequence Number Checking (Correction/Detection State Machine)

In both the UDT and SDT modes of operation, each AAL1 cell which is destined for the RX_SAR has its AAL1 header byte processed by a sequence number checking process standardized in ITU-T I.363.1. The first portion of the processing occurs in the Correction/Detection state machine, which is explained in this section. This algorithm examines the received AAL1 byte and determines whether the sequence number protection on the byte is correct by checking for CRC and parity errors. This state machine is primarily responsible for sending a corrected sequence number and CSI bit to the Fast Sequence Number Processing state machine (outlined in Section 4.6.1.4) for further sequence number processing.

Based on the ITU-T I.363.1 standard, the Correction/Detection state machine is capable of analyzing a byte of data. It can then correct a single-bit error in the data or detect (but not correct) a two-bit error. A single-bit error is

classified as the occurrence of either: (i) a parity error or (ii) a CRC error AND a parity error. An uncorrectable error occurs if a CRC error is detected without a corresponding parity error.

A brief description of the functionality is outlined below.

1. The state machine examines the AAL1 byte and checks for CRC and parity errors, based on hard-wired values contained within the MT90528. The state machine then outputs two pieces of information for use by the Fast SN Processing state machine: a validity indicator and a sequence number. The validity signal indicates whether or not the received byte was determined to be valid (i.e., it was either correct upon arrival, or was corrected by the Correction/Detection state machine). The sequence number is that which was determined by the Correction/ Detection machine to be the intended sequence number.
2. The type of error-processing which is performed depends upon the current state of the standardized state machine, either Correction or Detection:

CRC Error?	Parity Error?	Correctable?	Resulting SN	Valid?	AAL1 Header Error	Next State
No	No	correct - no need	SN of input byte	Yes	+0	Correction
No	Yes	Yes	SN of input byte	Yes	+1	Detection
Yes	No	No	don't care *	No	+1	Detection
Yes	Yes	Yes	corrected SN	Yes	+1	Detection

Table 13 - Operation of Correction/Detection State Machine in Correction State

CRC Error?	Parity Error?	Correctable?	Resulting SN	Valid?	AAL1 Header Error	Next State
No	No	correct - no need	SN of input byte	Yes	+0	Correction
No	Yes	No	don't care *	No	+1	Detection
Yes	No	No	don't care *	No	+1	Detection
Yes	Yes	No	don't care *	No	+1	Detection

Table 14 - Operation of Correction/Detection State Machine in Detection State

Note * - When an errored SN cannot be corrected, the Correction/Detection state machine outputs the SN of the input byte, uncorrected.

3. The most significant bit of the resulting sequence number (i.e., the CSI bit) may be processed further by the SRTS clock recovery sub-module (see Section) or, in the SDT case, by the pointer-processing sub-module (see "Pointer Processing" on page 81). The 3 least significant bits are transmitted to the Fast Sequence Number Processing state machine as the current cell's sequence number.
4. At the end of cell processing, two pieces of information related to the Correction/Detection state machine are updated in the Reassembly Control Structure for the VC: the next state of this state machine (either Correction or Detection) and the AAL1 Header Errors field.

4.6.1.4 Sequence Number Checking (Fast SN Processing State Machine)

After being processed by the Correction/Detection state machine, **all** AAL1 header bytes (whether correctable or not) and their corresponding validity indicators are passed to the Fast SN Processing state machine standardized within ITU-T I.363.1. This second portion of the Sequence Number Checking sub-module is responsible for analyzing the received sequence number values and determining whether the cells are being received in the correct order. The Fast Sequence Number Processing state machine can detect and compensate for lost cells. In addition, it can compensate for events which it determines to be misinserted cells.

UDT Mode of Operation

Although based on the state machine standardized in ITU-T I.363.1, additional functionality was added to the UDT RX_SAR's state machine in the form of two extra states:

- The **single_cell_loss_misinsertion** state was added to provide for the insertion of in-order dummy cells in the event of a single cell loss or misinsertion. As outlined in the table below, any time that an apparent single-cell loss occurs, a dummy cell is inserted and then the received cell is accepted into the port's Reassembly Circular Buffer. If the event is indeed a single-cell loss, the subsequent received cell is accepted and the state machine returns to the **sync** state. If the apparent single-cell loss turns out to have been a cell misinsertion event, the state machine returns to **sync**, but the most recently received (i.e., late) cell is discarded because a dummy cell was previously inserted in place of the misinserted cell. Similarly, if the apparent single-cell loss turns out to have been a sequence number protection failure, the state machine returns to **sync** and the most recently received cell is discarded because a dummy cell was previously inserted (erroneously) when all of the cells were actually being received in order.
- The **late_cell_insertion** state was added as a special user-programmable feature to provide CDV monitoring. If the user enables the late-cell-checking feature (by setting the CHECK_LATE_ARRIVALS bit in the UDT Reassembly Control Register at 2000h), when a per-port late-cell timeout counter reaches the value programmed by the user, a late cell timeout is reached and the Fast SN Processing state machine transitions into the **late_cell_insertion** state, inserting a single dummy cell on the transition. Once in the **late_cell_insertion** state, the subsequent cell arrival will determine the type of event that occurred. If the originally expected cell arrives, this is a late cell arrival case; the late cell is discarded and the state machine returns to **sync**. If the cell which arrives has a sequence number greater by one than that which was originally expected, a single cell loss has occurred; the received cell is accepted and the state machine returns to **sync**.

The operation of the state machine is summarized in the following table:

Current State	Transition Event	Action Taken	Next State	Note
x (don't care)	reset asserted	- none	reset_state	
reset_state	reset de-asserted	- none	start	
start	invalid sequence number	- discard cell	start	
	valid sequence number	- discard cell	out_of_sync	
out_of_sync	invalid sequence number	- discard cell	start	
	received cell is not in sequence with previous cell	- discard cell	out_of_sync	
	received cell is in sequence with previous cell	- accept received cell - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**

Table 15 - Operation of UDT Fast Sequence Number Processing State Machine

Current State	Transition Event	Action Taken	Next State	Note
sync	late cell timeout period reached and CHECK_LATE_ARRIVALS = '1'	- UDT RX_SAR inserts a single dummy cell	late_cell_insertion	
	invalid sequence number	- accept received cell	invalid	
	received cell is in sequence with previous cell	- accept received cell - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell is not in sequence with the previously-received cell -> received cell has a sequence number one greater than the expected sequence number	- assume single-cell loss event - UDT RX_SAR inserts a single dummy cell - after dummy cell insertion, accept received cell (in-order dummy cell insertion) - declare **aal1_seq_error**	single_cell_loss_ misinsertion	
	received cell is not in sequence with the previously-received cell -> received cell has a sequence number that is NOT one greater than the expected sequence number	- cannot assume what happened (may be a multi-cell loss case) - accept received cell (thus, if this is a multi-cell loss case, out-of-order dummy cell insertion will occur) - declare **aal1_seq_error**	out_of_seq	
invalid	invalid sequence number	- discard cell	start	
	received cell is in sequence with last "good" cell (i.e., cell misinsertion)	- discard cell - declare **misinserted_cell_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has a valid sequence number that is two greater than the last "good" cell (i.e., sequence number protection failure)	- accept received cell - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has valid sequence number, but doesn't meet either of the 2 previous criteria	- discard cell	out_of_sync	
out_of_seq	invalid sequence number	- discard cell	start	
	received cell is in sequence with last received cell (i.e., multiple cell loss)	- calculate number of lost cells (up to 7) - UDT RX_SAR inserts dummy cell(s) - after dummy cell insertion(s), accept received cell - declare **lost_cell_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has a valid sequence number that is two greater than the last in-sequence cell (i.e., sequence number protection failure)	- accept received cell - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has valid sequence number, but doesn't meet either of the 2 previous criteria	- discard cell	out_of_sync	

Table 15 - Operation of UDT Fast Sequence Number Processing State Machine

Current State	Transition Event	Action Taken	Next State	Note
single_cell_loss_ misinsertion	invalid sequence number	- discard cell	start	
	received cell is in sequence with last received cell (i.e., single cell loss)	- accept received cell - declare **lost_cell_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell is in sequence with last in-sequence cell (i.e., cell misinsertion)	- discard cell (dummy cell already inserted to take place of misinserted cell) - declare **misinserted_cell_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has a valid sequence number that is two greater than the last in-sequence cell (i.e., sequence number protection failure)	- discard received cell (extra dummy cell was inserted when all cells were actually received in order) - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has valid sequence number, but doesn't meet any of the 3 previous criteria	- discard cell	out_of_sync	
late_cell_insertion	invalid sequence number	- discard cell	start	
	received cell has a sequence number one greater than the originally expected sequence number (i.e., this appears to be a single-cell loss)	- accept received cell (dummy cell was already inserted to replace the lost cell) - declare **lost_cell_error** - declare **aal1_seq_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell is that which was originally expected (i.e., late cell arrival)	- discard cell (because a dummy cell was already inserted to replace this one) - declare **late_cell_error** - per-port timeout circuitry is enabled to permit late-cell insertions	sync	**
	received cell has valid sequence number, but doesn't meet either of the 2 previous criteria	- discard cell - declare **aal1_seq_error**	out_of_sync	

Table 15 - Operation of UDT Fast Sequence Number Processing State Machine

Note **: The per-port timeout circuitry for late-cell insertion is enabled only when the state machine is entering the sync state. Therefore, late-cell insertion is only possible when the Fast SN Processing SM is in the "sync" state.

Here are some examples of incoming cell streams containing errors and the corresponding corrective actions taken by the UDT RX_SAR.

Description of Error	Sample Incoming Cell Stream	Cells Used for Reassembly	Errors Declared
Sequence number protection failure (looks like single cell loss)	1 - 3* - 3 - 4 - 5	1 - D_2 - 3* - 4 - 5	1 AAL1 Sequence Error
NOTE: D indicates the insertion of a dummy cell containing user-programmable data.			

Table 16 - Examples of Operation of the UDT Fast Sequence Number Processing State Machine

Description of Error	Sample Incoming Cell Stream	Cells Used for Reassembly	Errors Declared
Sequence number protection failure (looks like multiple cell loss)	1 - 4* - 3 - 4 - 5	1 - 4* - 3 - 4 - 5	1 AAL1 Sequence Error
Single lost cell	1 - 2 - 4 - 5	1 - 2 - D_3 - 4 - 5	1 AAL1 Sequence Error 1 Lost Cell
Multiple lost cells (from 2 to 7 lost cells)	1 - 2 - 6 - 7	1 - 2 - 6 - D_3 - D_4 - D_5 - 7	1 AAL1 Sequence Error 3 Lost Cells
Misinserted (swapped) cell	1 - 2 - 4 - 3 - 5 - 6	1 - 2 - D_3 - 4 - 5 - 6	1 AAL1 Sequence Error 1 Misinserted Cell
NOTE: D indicates the insertion of a dummy cell containing user-programmable data.			

Table 16 - Examples of Operation of the UDT Fast Sequence Number Processing State Machine

SDT Mode of Operation

The SDT version of the Fast Sequence Number Checking state machine is very similar to the UDT version. However, in the SDT version, no extra states are added for increased functionality. Unlike the UDT version, there is no provision for the insertion of dummy cells in late-cell cases, nor for in-order dummy cell insertion when single-cell losses are assumed. Because the SDT machine has fewer states than the UDT version, there are some differences in the way in which certain cell arrival sequences are interpreted by the state machines. The following table outlines the operation of the SDT state machine:

Current State	Transition Event	Action Taken	Next State
x (don't care)	reset asserted	- none	reset_state
reset_state	reset de-asserted	- none	start
start	invalid sequence number	- discard cell	start
	valid sequence number	- discard cell	out_of_sync
out_of_sync	invalid sequence number	- discard cell	start
	received cell is not in sequence with previous cell	- discard cell	out_of_sync
	received cell is in sequence with previous cell	- accept received cell	sync
sync	invalid sequence number	- accept received cell	invalid
	received cell is not in sequence with the previously-received cell	- accept received cell - declare **aal1_seq_error**	out_of_seq
	received cell is in sequence with previous cell	- accept received cell - permit SDT RX_SAR to update CAS information based on this cell's contents	sync
invalid	invalid sequence number	- discard cell	start
	received cell is in sequence with last "good" cell (i.e., cell misinsertion)	- discard cell (because misinserted cell was accepted when it shouldn't have been) - declare **misinserted_cell_error**	sync
	received cell has a valid sequence number that is two greater than the last "good" cell (i.e., sequence number protection failure)	- accept received cell	sync
	received cell has valid sequence number, but doesn't meet either of the 2 previous criteria	- discard cell	out_of_sync

Table 17 - Operation of SDT Fast Sequence Number Processing State Machine

Current State	Transition Event	Action Taken	Next State
out_of_seq	invalid sequence number	- discard cell	start
	received cell is in sequence with last “good” cell (i.e., cell misinsertion)	- discard cell (because misinserted cell was accepted when it shouldn’t have been) - declare **misinserted_cell_error**	sync
	received cell is in sequence with last received cell (i.e., cell loss)	- calculate number of lost cells (up to 6) - SDT RX_SAR inserts dummy cell(s) - after dummy cell insertion(s), accept received cell - declare **lost_cell_error**	sync
	received cell has a valid sequence number that is two greater than the last in-sequence cell (i.e., sequence number protection failure)	- accept received cell	sync
	received cell has valid sequence number, but doesn’t meet any of the 3 previous criteria	- discard cell	out_of_sync

Table 17 - Operation of SDT Fast Sequence Number Processing State Machine

Here are some examples of incoming cell streams containing errors and the corresponding corrective actions taken by the SDT RX_SAR.

Description of Error	Sample Incoming Cell Stream	Cells Used for Reassembly	Errors Declared
Sequence number protection failure (looks like single cell loss)	1 - 3* - 3 - 4 - 5	1 - 3* - 3 - 4 - 5	1 AAL1 Sequence Error
Sequence number protection failure (looks like multiple cell loss)	1 - 4* - 3 - 4 - 5	1 - 4* - 3 - 4 - 5	1 AAL1 Sequence Error
Single lost cell	1 - 2 - 4 - 5	1 - 2 - 4 - D_3 - 5	1 AAL1 Sequence Error 1 Lost Cell
Multiple lost cells (from 2 to 6 lost cells)	1 - 2 - 6 - 7	1 - 2 - 6 - D_3 - D_4 - D_5 - 7	1 AAL1 Sequence Error 3 Lost Cells
Misinserted (swapped) cell	1 - 2 - 4 - 3 - 5 - 6	1 - 2 - 4 - 5 - D_4 - 6	2 AAL1 Sequence Errors 1 Misinserted Cell 1 Lost Cell
NOTE: D indicates the insertion of a dummy cell containing user-programmable data.			

Table 18 - Examples of Operation of SDT Fast Sequence Number Processing State Machine

4.6.1.5 Received Cell Processing

The RX_SARs are responsible for extracting data from received cells and transferring that data to the TDM module, for eventual transmission onto the TDM output bus. In addition, these modules are responsible for:

- performing slip checking and RX_SAR write-pointer adjustment prior to transferring data to the TDM module
- generating dummy cells in the case of sequence errors such as lost or misinserted cells
- SDT pointer processing
- extracting CAS from SDT cells and transferring it to the TDM module

UDT Mode of Operation

In “normal” operation (i.e., the UDT RX_SAR’s Fast SN Processing state machine is in “sync”), the UDT RX_SAR is responsible for transferring a UDT cell received at the UTOPIA interface to a single UDT Reassembly Circular Buffer in internal memory (corresponding to the TDM port for which the data is destined). However, if it is not in “sync”, the UDT RX_SAR may also be responsible for inserting up to 7 dummy cells (each filled with 47 bytes of user-defined data) into the port’s UDT Reassembly Circular Buffer.

Regardless of the state of the Fast SN Processing state machine, a comparison is made between the value of the UDT RX_SAR’s write pointer and the TDM module’s read pointer, prior to the transfer of each cell to the circular buffer. The result of the comparison determines whether a slip-error needs to be reported in the MIB statistics, and may also result in an adjustment of the write pointer’s location before a cell is written to the UDT Reassembly Circular Buffer (see UDT Overflow and Underrun Detection below).

TDM Data Transfer

Normally the UDT RX_SAR simply transfers 47-byte blocks of data from the UTOPIA interface to a port’s UDT Reassembly Circular Buffer. However, in the case of a cell loss or misinsertion, up to 7 dummy cells may be inserted into the circular buffer before the received cell is accepted. If the user has set the **UDT_INSERT_LOST** bit in the UDT Reassembly Control Register at byte-address 2000h, the UDT RX_SAR is configured to insert the number of dummy cells calculated by the Fast SN Processing state machine in a cell loss case. On the other hand, if the user has not set the UDT_INSERT_LOST bit, the UDT RX_SAR will insert a maximum of 2 dummy cells (i.e., even if the number of lost cells is greater than 2, only 2 dummy cells may be inserted) into the UDT Reassembly Circular Buffer in a cell-loss event.

UDT Reassembly Circular Buffers

In the UDT mode of operation, each VC has a specified UDT Reassembly Circular Buffer located in internal memory. Each buffer is 2048 bytes long and is therefore capable of storing over 43 cells worth of data. The user can adjust the **Maximum Lead** field in the VC’s UDT Reassembly Control Structure to control the CDV tolerance of the VC. The Maximum Lead field, as explained in Section , “UDT Reassembly Control Structures,” on page 68, is user-programmable and determines the maximum distance between the TDM module’s read pointer and the UDT RX_SAR’s write pointer. In general, the operations of the UDT RX_SAR and the TDM module are synchronized so that the UDT RX_SAR’s write pointer and the TDM module’s read pointer are always an average distance (equivalent to Maximum Lead / 2) apart. This phenomenon occurs because most of the time, each time that the UDT RX_SAR writes a complete cell to the circular buffer, the TDM module reads the complete cell (1:1 relationship).

UDT Overflow and Underrun Detection

The UDT RX_SAR is responsible for generating buffer overflow and buffer underrun error notifications on a per-VC basis. In addition to determining if errors occur, the UDT RX_SAR also attempts to compensate for these slips by adjusting its write pointer. The goal of the write pointer adjustment is to prevent the occurrence of subsequent slips.

When the first cell is about to be written to the UDT Reassembly Circular Buffer for a VC, the UDT RX_SAR looks at the current value of the TDM read pointer and adjusts the value of its write pointer to be equal to **TDM read pointer + avg_lead** (where avg_lead is equal to Maximum_Lead / 2). Therefore, if no slips occur, the write pointer should always be an “average” distance away from the TDM read pointer.

For all subsequent cells, an algorithmic slip-checking routine is performed for every cell which is written to the UDT Reassembly Circular Buffer, whether it is a dummy cell or a received ATM cell. Each time a cell is to be written to internal memory, the algorithm looks at the relationship between the UDT RX_SAR’s write pointer and the TDM module’s read pointer. The algorithm then determines whether the next write to occur will be an “okay” condition, an overflow, or an underrun. Generally speaking, an “okay” condition means that the UDT RX_SAR is trying to write to a memory location which is within a distance of Maximum Lead from the TDM read pointer. Overflow conditions are conditions in which there is a risk of the UDT RX_SAR over-writing data which has yet to be read by the TDM

module. Underruns occur when the TDM has begun to re-read data from the buffer because it has not been replaced by new data from the UDT RX_SAR.

If an “okay” condition is detected, the UDT RX_SAR is permitted to write to the UDT Reassembly Circular Buffer at the location determined by the UDT RX_SAR write pointer from the VC’s UDT Reassembly Control Structure. In the case of a slip (either an underrun or an overflow), the UDT RX_SAR’s write pointer is adjusted such that the cell is written to the circular buffer at the location of TDM read pointer + avg_lead. In addition, when slips are detected, the corresponding MIB statistics fields (**Buffer Underruns** or **Buffer Overflows**) in the active VC’s UDT Reassembly Control Structure are incremented.

Only in rare instances (e.g., when the TDM output clock, SToCLK, is very different from the TDM input clock, STiCLK) will slips occur. In such a case, two cells may be written to internal memory before the TDM module can read a single cell (or, perhaps two cells may be read from memory before another one can be written by the UDT RX_SAR). Since both the UDT RX_SAR and the TDM module operate with 47-byte blocks of data, it is necessary to set Maximum Lead to at least 94d (so that the average distance between the read and write pointers is 47d, or the equivalent of one cell of data). If Maximum Lead is not set to > 94d, even a minor slip (e.g., a cell that arrives one clock cycle after the TDM starts reading from the buffer) appears as a gross slip (i.e., underrun or overflow). Because gross slips cause the UDT RX_SAR’s write pointer to be re-aligned, data in the buffers may be overwritten. As well, if adaptive clock recovery is being used (see Section , “Digital Phaseword Generation for Adaptive Clock Recovery,” on page 87), repeated gross slips mean that the PLL cannot track the incoming data to SToCLK, and gross slips will likely continue to occur. The following equation can be used for setting Maximum Lead:

maxlead = 2*n*CDV+94 where n=256 for E1 and n=193 for DS1, and CDV is in milliseconds.

Overall, the Reassembly Circular Buffers in UDT mode are very large. Therefore, there is ample room to adjust the value of Maximum Lead and thereby reduce the risk of overflows. It should be stated, however, that the penalty for a large Maximum Lead value will be a start-up delay: the TDM module will read invalid data until it reaches the location of “TDM read pointer + avg_lead” at which the UDT RX_SAR started writing to the buffer. Also, there will be a continuing delay in the reception of data on DSTo because of the distance between the write pointer and the read pointer (i.e., data written to the buffer by the UDT RX_SAR isn’t immediately read out by the TDM module).

UDT Received Cell Counter

The UDT RX_SAR also provides the user with the number of UDT cells received from the UTOPIA block. This 16-bit counter value can be viewed in register URCCR at address 2006h. This counter is an overall UDT cell counter: it is incremented every time a UDT cell is received from the UTOPIA (regardless of whether the cells are discarded by the UDT RX_SAR). When this counter rolls over, a status bit gets set in the URSR register at address 2004h. This status bit can be cleared by software. This rollover condition can also generate a service request to the CPU if the corresponding service enable bit is set.

The user is also provided with a per-VC cell counter. This counter is located in the UDT Reassembly Control Structure (see Figure 28 on page 71). The operation of this counter is similar to the overall UDT cell counter. When the per-VC counter rolls over, a status bit gets set in the control structure and can be cleared by the user. The rollover condition can also generate a request to the CPU if the UDT_REAS_ROLL_SE bit is set in the URSER register at address 2002h. The CPU can then read the contents of the SERVICE_PORT field of the URSR register at address 2004h to identify which control structure generated the service request.

SDT Mode of Operation

In “normal” operation (i.e., the SDT RX_SAR’s Fast SN Processing state machine is in “sync”), the SDT RX_SAR is primarily responsible for transferring TDM and CAS data (if applicable) from SDT cells received at the UTOPIA interface to multiple SDT Reassembly Circular Buffers in external memory. In addition, SDT pointers must be analyzed to ensure that the extracted data is being directed to the correct TDM channels.

As in the UDT RX_SAR, the SDT RX_SAR is responsible for compensating for sequence number error conditions. Up to 6 dummy cells may be inserted into the various SDT Reassembly Circular Buffers corresponding to the VC in question.

The SDT RX_SAR compares the value of the SDT RX_SAR's write pointer and the TDM module's read pointer, prior to the transfer of each cell to the SDT Reassembly Circular Buffers. The result of the comparison determines whether a slip-error needs to be reported in the MIB statistics, and may also result in an adjustment of the write pointer's location before a cell is written to the SDT Reassembly Circular Buffers (see "SDT Overflow and Underrun Detection" on page 85).

Pointer Processing

Within SDT-formatted cells, pointers are used to indicate the location of the first channel of data within an AAL1 structure.

A pointer can be received only from an even-numbered cell which is identified as a pointer-type cell because its CSI bit is set. Pointers are received in this manner for all SDT VCs, except for non-CAS cells carrying one channel. In that special case, no pointers should be received.

Once an even-numbered cell with a set CSI bit is received, the pointer byte of the cell is processed. First, some error-checking procedures are performed:

- the pointer byte is examined for even-parity errors. If there is a parity error, the contents of the pointer byte are ignored, the **Pointer Parity Errors** MIB statistic field in the SDT Reassembly Control Structure is incremented, and the pointer-processing routine is exited.
- if no parity error is found, the 7 least-significant bits of the pointer byte (the 8-bit pointer byte, less the parity bit) are then examined to see if they exceed the maximum allowable "valid" pointer value of 93d (5Dh). If either of the following cases is true, the pointer processing routine is exited:
  - if the pointer byte has a value of 127d (7Fh), it is a "dummy" pointer (a valid pointer value); this pointer value is ignored by the SDT RX_SAR.
  - if the pointer byte has a value exceeding 93d and does not equal 127d, it is an illegal pointer value; therefore, the pointer value is ignored and a Pointer_Out_of_Range error is detected, causing the **Po** status bit of the SDT Reassembly Control Structure for the VC to be set.

If the above error conditions are not met, the pointer byte is considered to be valid and is processed as such by the SDT RX_SAR:

- the pointer byte is automatically considered to be correct (based on the fact that there is a lot of protection on the AAL1 byte, so bytes should not be received marked erroneously as pointers). Therefore, the "golden" received pointer value is always used to determine where the SDT RX_SAR should currently be operating within a VC's AAL1 structure. Regardless of where the SDT RX_SAR is pointing in the AAL1 structure, it is adjusted to point to the location identified by the received pointer byte.
- if the received pointer matches the SDT RX_SAR's internal location controller, all is well and no errors are reported.
- if the internal location controller doesn't match the received pointer, a framing/data misalignment error has occurred:
  - if the received pointer is equal to 0, the pointer misalignment is corrected immediately; therefore, the **Pointer Reframes** statistic field in the SDT Reassembly Control Structure is incremented.
  - if the received pointer is not equal to 0, the misalignment between the internal controller and the received pointer is not resolved immediately:
    - if the internal controller reaches the start of the AAL1 structure during the current cell, re-synchronization occurs and the Pointer Reframes statistic field in the SDT Reassembly Control Structure is incremented.

- if the internal controller does not reach the start of the AAL1 structure during the current cell, the **P (Pointer Reframe Pending)** bit of the SDT Reassembly Control Structure is set. Ultimately, when re-synchronization does occur, the P status bit is cleared and the Pointer Reframes statistic field in the SDT Reassembly Control Structure is incremented.

Note: Even in normal operation, one pointer reframe will usually be reported on each SDT VC, shortly after start-up. Because the first cell received on a VC is always discarded by the SDT Fast SN Processing state machine (as per the ITU-T I.363.1 standard), the first available pointer is always discarded. Therefore, the SDT RX_SAR processes a minimum of 7 cells before another pointer is received. Thus, the data for the first 8-cell sequence is generally misaligned and directed toward the wrong TDM channels. When the second pointer is received, the internal location controller is adjusted to the value contained in the received pointer byte and, in most cases, a pointer reframe is reported.

SDT Reassembly Circular Buffers

In the SDT mode of operation, TDM data is processed on a per-channel basis, rather than on a per-VC basis, as in the UDT case. As a result, when operating in SDT mode, each channel within a VC is allocated its own SDT Reassembly Circular Buffer in external memory.

SDT Reassembly Circular Buffers have programmable lengths (on a per-VC basis). The user may configure a VC such that the buffers associated with the VC have lengths of 64, 128, 256, 512, or 1024 entries, based on the configuration of the **BS (Buffer Size)** bits in the SDT Reassembly Control Structure for the VC. Note that all of the buffers for a particular VC have the same size. The size of buffers selected should be influenced by the expected CDV on a VC. For instance, if a large CDV is expected, a longer buffer would be desirable, so that there is sufficient data to play out to the TDM bus in the period between cell arrivals.

The user can adjust the **Maximum Lead** field in the VC's SDT Reassembly Control Structure to provide further control over the CDV tolerance of the VC. The Maximum Lead field, as outlined in "SDT Reassembly Control Structures" on page 69, is user-programmable and determines the maximum distance between the TDM module's read pointer and the SDT RX_SAR's write pointer. In general, Maximum Lead should be set to a value which, when used in combination with Buffer Size, will result in the desired CDV buffering. The setting of Maximum Lead effectively shortens the buffer length, ensuring that there is no excessive delay between the time that data is received at the buffer input and when it is played out on the TDM output bus. However, if Maximum Lead is not set in accordance with the CDV of the incoming cells, it can result in the reporting of slips (underruns or overflows), which may cause data received at the SDT Reassembly Circular Buffers to be overwritten or skipped. In general, Maximum Lead should be set to a value calculated as follows:

Maximum Lead in bytes = desired buffer limit in bytes = 2 + (2 * CDV) / 0.125 ms, where CDV is in milliseconds.

Because there is no pre-defined mapping for the SDT Reassembly Circular Buffers, they can be programmed to start anywhere in the external memory for the MT90528 device (with some restrictions, explained here). The address of each SDT Reassembly Circular Buffer is formed as follows. A two-bit value is obtained from the **CB_BASE_ADD** field of the SDT Reassembly Control Register at byte-address 2040h. These bits form the two most significant bits of the address to external memory. The complete address is formed by concatenating these bits with the 12-bit value obtained from a **Reassembly Circular Buffer Base Address** field within each SDT Reassembly Control Structure.

The number of bits of the concatenated (i.e., 14-bit) address which are used to form the actual address to external memory is determined by the size of the buffers selected for the VC. For instance, if 64-entry buffers are selected, all 14 bits of the concatenated address are used. However, if 1024-entry buffers are selected, only the bottom 10 bits of the address are used. Refer to Table 19 below for more details regarding how the base addresses of the SDT Reassembly Circular Buffers are formed.

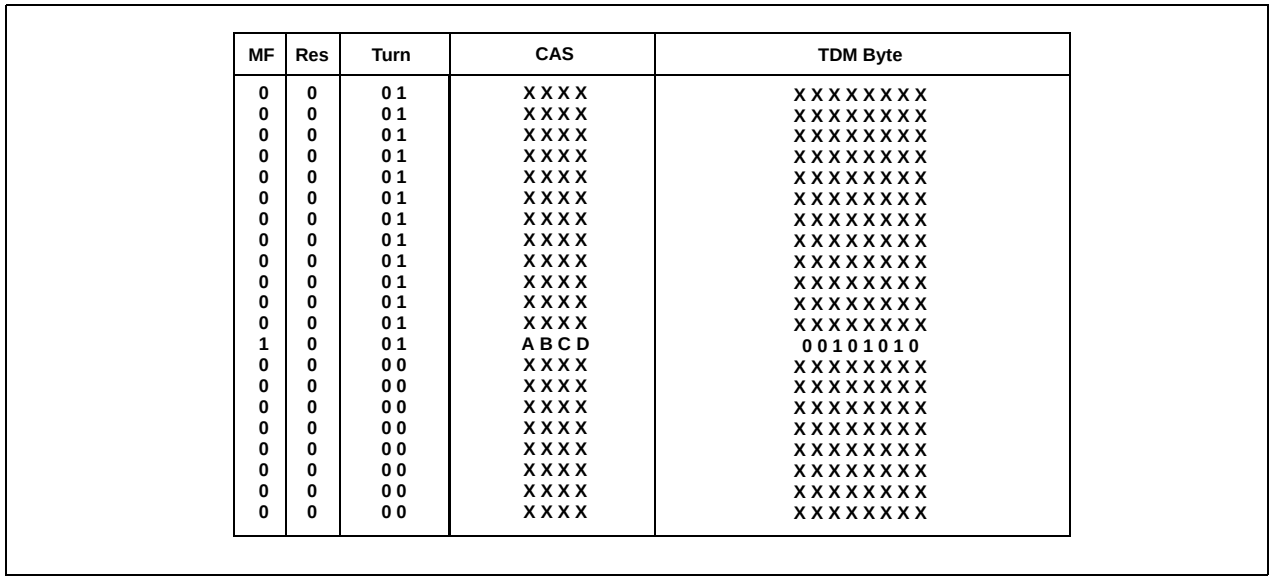
For ease of programming, it is suggested that consecutive addresses be used. For instance, in a 3-channel VC, the addresses configured in the Reassembly Circular Buffer Base Address fields should be set to 000h, 001h, and

002h, regardless of the size of the buffers selected. It must be noted that the Reassembly Circular Buffer Base Address must correspond to the address given within the TDM SDT Reassembly Control Structure (see Figure 13 on page 46) for the chosen TDM channel destination (port- and channel- specific).

Buffer Size	Address to External Memory
64 entries	{cb_base_add<1:0>,reassembly_circular_buffer_base_add<11:0>,6'b0}
128 entries	{cb_base_add<0>,reassembly_circular_buffer_base_add<11:0>,7'b0}
256 entries	{reassembly_circular_buffer_base_add<11:0>,8'b0}
512 entries	{reassembly_circular_buffer_base_add<10:0>,9'b0}
1024 entries	{reassembly_circular_buffer_base_add<9:0>,10'b0}

Table 19 - Formation of SDT Reassembly Circular Buffer Base Addresses to External Memory

Each 16-bit entry in external memory contains a variety of information. Each entry is composed of the fields shown in Figure 29 and explained in the text below.



MF	Res	Turn	CAS	TDM Byte
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
0	0	01	XXXX	XXXXXXXX
1	0	01	ABCD	00101010
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX
0	0	00	XXXX	XXXXXXXX

Figure 29 - Per-Channel SDT Reassembly Circular Buffer

- **MF -** multiframe indicator; this bit is used only when a VC is carrying CAS data (if a VC isn't carrying CAS, the MF bits are always zero); the MF bit is set in the buffer for every channel of a VC, each time that the SDT RX_SAR determines the location of the start of the next multiframe
- **Res -** reserved field; this field always contains a zero
- **Turn -** this field contains a copy of the two most-significant bits of the SDT RX_SAR write pointer for the VC. These bits represent the "turn" of the circular buffer and are used by the TDM module for underrun detection.
- **CAS -** If CAS data is being processed, this field contains the nibble of data which was last received by this channel (i.e., in the previous multiframe). CAS data is repeated for an entire multiframe (i.e., 24 consecutive entries in DS1 case; 16 consecutive entries in E1 case).
- **TDM Byte -** This field contains the TDM data bytes which are extracted from received cells. If dummy cells have been inserted, this field contains the value of the dummy data programmed by the user.

SDT TDM Data Transfer and CAS Nibble Processing

The overall byte extraction process within the SDT RX_SAR is quite similar to that used by the UDT RX_SAR. In general, the SDT RX_SAR is responsible for transferring a cell received at the UTOPIA interface to the (one or many) SDT Reassembly Circular Buffer(s) for the VC. In a cell loss or misinsertion condition, the SDT RX_SAR is

responsible for determining the number of dummy cells to be inserted, transferring the appropriate dummy data to the various SDT Reassembly Circular Buffers and, ultimately, transferring the received cell from the UTOPIA module to the SDT Reassembly Circular Buffer(s). Besides extracting TDM data bytes, the SDT RX_SAR must also, in certain modes, extract CAS nibbles, which were previously explained in “SDT Reassembly Circular Buffers” on page 82.

As in the UDT mode of operation in a cell insertion case, the SDT RX_SAR, under user control, can limit the number of cells to be inserted into the SDT Reassembly Circular Buffer(s). By default, a maximum of two dummy cells will be inserted in a cell loss case. However, if the user sets the **SDT_INSERT_LOST** bit in the SDT Reassembly Control Register at byte-address 2040h, the SDT RX_SAR inserts the number of dummy cells calculated by the Fast SN Processing state machine in a cell loss case. SDT dummy cells always contain 47 bytes of user-defined data - no attempt is made to speculate whether pointers or CAS data were present in lost cells. Therefore, it is possible for pointer reframes to occur after dummy-cell insertions, because extra dummy bytes may have been inserted into the circular buffers (e.g., if a missing cell contained a pointer, only 46 bytes of dummy fill should have been inserted into the buffers; however, 47 bytes were inserted, causing a misalignment between the internal counters of the SDT RX_SAR and the received SDT pointers).

Once the pointer byte (if present) has been processed and before any accesses are made to the SDT Reassembly Circular Buffers in external memory, the SDT RX_SAR accesses the SDT Reassembly Control Structure in internal memory to obtain the value of the internal pointer, **Current Entry**. This field, which is used to determine to which channel within the VC the next byte of data is destined, is initialized to point to the **First Entry** in the VC. Once Current Entry reaches the last channel in a VC (identified by **Last Entry**, as programmed by the user in the control structure), it wraps around to First Entry, and the process starts again.The only time that Current Entry digresses from this path (advancing from First Entry to Last Entry, and then wrapping around) is when a pointer reframe occurs, as explained in “Pointer Processing” on page 81. When a reframe occurs, the Current Entry pointer is reset to point to First Entry.

In CAS VCs, another internal variable, **Current Frame**, tracks the advancement through the SDT Reassembly Control Structure. This variable is used to determine the location at which processing is occurring within a multiframe. Current Frame increments by one each time that Current Entry wraps around (indicating that all of the channels in the VC and, therefore, the frame have been serviced). The SDT RX_SAR uses the Current Frame variable to determine whether to process the current frame of data as TDM payload bytes, or as CAS nibbles; the last frame of each multiframe (frame 16 in the E1 case, frame 24 in the DS1 case) carries CAS data. Current Frame is reset to 0 each time it finishes processing the final frame of a multiframe, or when a forced pointer reframe occurs.

The Current Entry field points to the **Reassembly Circular Buffer Base Address** within the SDT Reassembly Control Structure which corresponds to the output TDM channel to which the current byte of received cell data is destined. The pointer is used in combination with the SDT RX_SAR Write Pointer to determine the exact location in external memory to which the data is written. Each SDT Reassembly Circular Buffer for a VC is addressed by the same write pointer. The write pointer is incremented by one each time that all of the buffers for the VC have been written to (i.e., each time Current Entry wraps around).

The data written to each circular buffer entry has the format shown in Figure 29, “Per-Channel SDT Reassembly Circular Buffer,” on page 83. When a VC is not carrying CAS, multiframes are not used. Therefore, the MF bit is always 0. Also, in non-CAS VCs, since no CAS is being extracted from received cells, the user should, in most cases, configure the SDT Reassembly Control Structure for the VC so that the **CASx** field in each entry in the control structure is 0. Therefore, all zeroes will be written to the CAS field within the corresponding channel’s Reassembly Circular Buffer. However, if the user wants to send specific CPU-defined signalling out on a channel’s CSTo output, the user can put the desired data in the CASx fields of the control structure. Whatever data is present in the CASx fields is always transferred to external memory.

When the processing of CAS nibbles is enabled (i.e., the **CAS<0>** bit in the SDT Reassembly Control Structure for a VC is set) the module first has to determine the location of the CAS nibbles within the received cells. In general, data which is extracted from cells when the Current Frame is equal to the CAS frame (frame 16 in E1 mode; frame 24 in DS1 mode), is considered to be CAS. However, within the MT90528, extra checking routines are performed to

ensure that the data that is extracted from the received cells is really CAS, before it is treated as such. If there is any doubt about the integrity of the CAS (e.g., Fast SN Processing state machine is not in sync; a pointer reframe is pending), the received data is not processed as CAS. Instead, the CASx fields in the SDT Reassembly Control Structure are not updated until the error conditions have been removed and there is confidence regarding the alignment of TDM and CAS data with the correct TDM output channels. Another point should be made: the CASx fields are only updated if the **CAS<1>** bit in the SDT Reassembly Control Structure for the VC is **cleared**, indicating that the user wishes to use the received CAS nibbles, rather than user-defined signalling.

If all of the error-checking conditions outlined above are met, the extracted CAS nibble is written to the CASx field of the SDT Reassembly Control Structure, corresponding to the Current Entry pointer. Note that strict multiframing is not used in the MT90528 device, due to concern about delay. Although CAS and TDM data are meant to be aligned, the MT90528 device would have to store up all of the data for an entire AAL1 structure (i.e., a complete multiframe) if the TDM data was to be output simultaneously with the corresponding CAS data. The resultant delay in the reception of data at the TDM ports is considered to be undesirable, so extra buffering of TDM data is not performed. Instead, when all of the channels in the VC have had their corresponding CAS nibbles processed, the Current Entry and Current Frame values wrap around. In the frame following that in which CAS data is received (i.e., the first frame of the multiframe), the new CAS data is output to the TDM module. As well, the **MF** (multiframe) bit is set in each SDT Reassembly Circular Buffer corresponding to the VC. This indicator is used by the TDM module to align data with the SToMF signal on the TDM interface bus.

One other user-programmable option is possible with respect to the reception of CAS data. When a CAS nibble is received and is considered valid, regardless of whether the user has decided to enable write-backs via the clearing of CAS<1>, it is possible for an examination of the nibble to be performed. If the user sets **CAS<2>**, the received nibble is compared to the previous CAS nibble for the channel (stored in CASx). If the nibble has changed, the **Cc (CAS Changed)** bit of the VC's SDT Reassembly Control Structure is set. User software could be configured to read the VC's CAS nibbles and monitor for changes when the Cc bit is set.

SDT Overflow and Underrun Detection

The SDT RX_SAR is responsible for generating buffer overflow and buffer underrun error notifications on a per-VC basis. In addition to determining if errors occur, the SDT RX_SAR also attempts to compensate for these slips by adjusting its write pointer. The goal of the write pointer adjustment is to prevent the occurrence of multiple consecutive slips.

Upon start-up, the SDT RX_SAR write pointer is set to a pre-defined slip-pointer value, regardless of the current relationship between the SDT RX_SAR write pointer and the TDM read pointer. Therefore, if no slips occur, the write pointer should always be an "average" distance away from the TDM read pointer.

For all cells other than the first cell received on a VC, an algorithmic slip-checking routine is performed when the cell is about to be written to the SDT Reassembly Circular Buffer(s). Each time a cell is to be written to external memory, the algorithm looks at the relationship between the SDT RX_SAR's write pointer and the controlling port's TDM module's read pointer (the controlling port is determined by the setting of the **VC TDM Port** field). The algorithm then determines whether the next write to occur will be an "okay" condition, an overflow, or an underrun. Generally speaking, an "okay" condition means that the SDT RX_SAR is trying to write to a memory location which is within a pre-defined distance (determined by Maximum Lead) from the TDM read pointer. Overflow conditions are conditions in which there is a risk of the SDT RX_SAR over-writing data which has yet to be read by the TDM module. Underruns occur when the TDM has begun to re-read data from the buffer because it has not been replaced by new data from the SDT RX_SAR.

If an "okay" condition is detected, the SDT RX_SAR is permitted to write to the SDT Reassembly Circular Buffer(s) at the location determined by the **SDT RX_SAR Write Pointer** and the **Reassembly Circular Buffer Base Addresses** fields from the VC's SDT Reassembly Control Structure. In the case of a slip (either an underrun or an overflow), the SDT RX_SAR's write pointer is adjusted such that the cell is written to the circular buffer at the location of the pre-calculated slip pointer. In addition, when slips are detected, the corresponding MIB statistics fields (**Buffer Underruns** or **Buffer Overflows**) in the active VC's SDT Reassembly Control Structure are incremented.

SDT Received Cell Counter

The SDT RX_SAR also provides the user with the number of SDT cells received from the UTOPIA block. This 16-bit counter value can be viewed in register SRCCR at address 2048h. This counter is an overall SDT cell counter: it is incremented every time an SDT cell is received from the UTOPIA (regardless of whether the cells are discarded by the SDT RX_SAR). When this counter rolls over, a status bit gets set in the SRCSR register at address 2046h. This status bit can be cleared by software. This rollover condition can also generate a service request to the CPU if the corresponding service enable bit is set.

The user is also provided with a per-VC cell counter. This counter is located in the SDT Reassembly Control Structure (see Figure 28 on page 71). The operation of this counter is similar to the overall SDT cell counter. When the per-VC counter rolls over, a status bit gets set in the control structure and can be cleared by the user. The rollover condition can also generate a request to the CPU if the SDT_REAS_ROLL_SE bit is set in the SRSER register at address 2042h. The CPU can then read the contents of the SERVICE_ADD field of the SRSR register at address 2044h to identify which control structure generated the service request.

Complete Reassembly Data Flow Overview

The following figures give a top-level view of the data flow in the reassembly direction within the MT90528 device.

Figure 30 shows the complete segmentation data path in UDT mode, from the incoming TDM data bus to the outgoing UTOPIA data bus, whereas Figure 31 shows the complete segmentation data path in SDT mode.

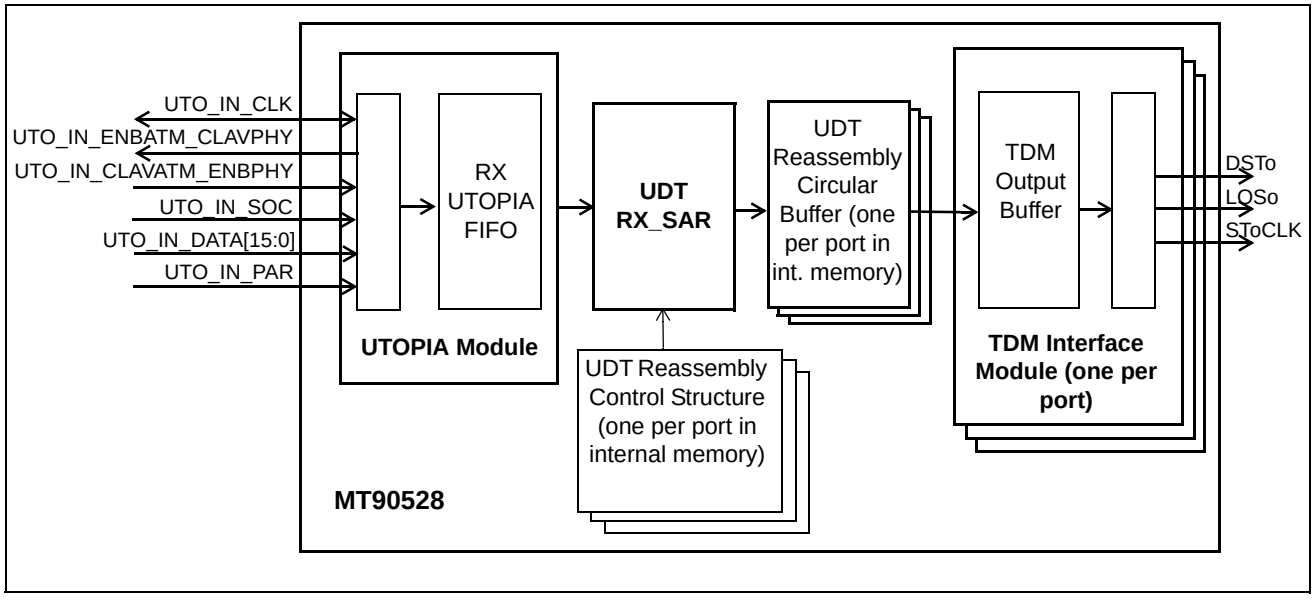


Figure 30 - Overview of CBR Data Reassembly Process (UDT Mode)

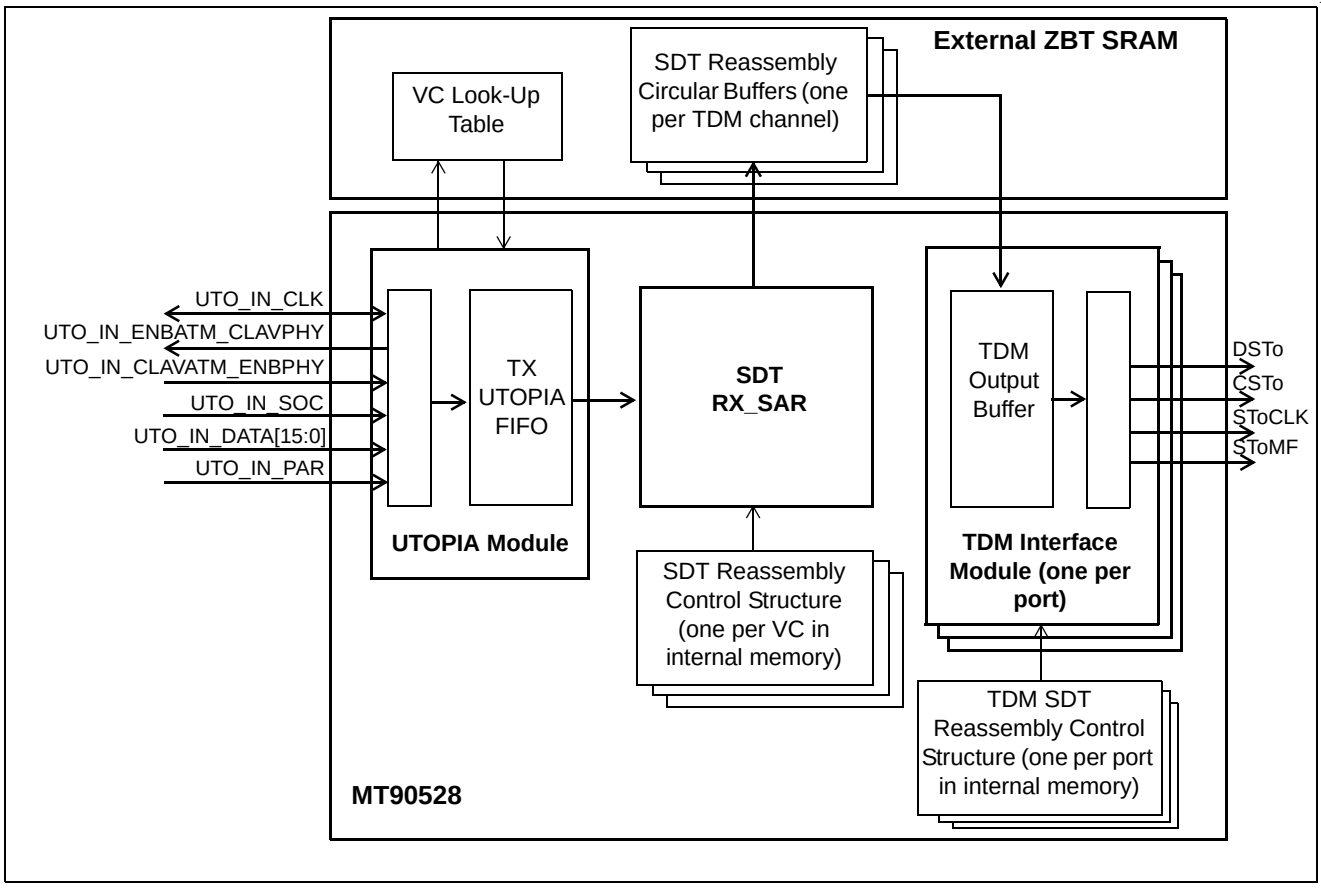


Figure 31 - Overview of CBR Data Reassembly Process (SDT Mode)

4.6.1.6 Clock Recovery Operations

The SDT RX_SAR and the UDT RX_SAR are responsible for generating data required for the performance of clock recovery operations within the MT90528. In the case of adaptive clock recovery, the active RX_SAR must generate a digital phaseword for transport to the internal per-port PLL. If SRTS clock recovery is being used, the RX_SAR extracts 4-bit RTS values from incoming ATM cells and sends them to the corresponding port's PLL.

Digital Phaseword Generation for Adaptive Clock Recovery

If the user has decided to use adaptive clock recovery to generate the TDM output clock, SToCLK, for a port, the **A (Adaptive Enable)** bit in the UDT/SDT Reassembly Control Structure for the port must be set. In the UDT case, there is only one VC per port. However, in the SDT case, only a single VC per port (where the port is identified by the value in the **VC TDM Port** field of the Reassembly Control Structure) may have its A bit set. **Note:** In addition to the Reassembly Control Structure, the PLL for the port must also be configured to operate in adaptive mode.

If the A bit is set, the UDT RX_SAR or the SDT RX_SAR is responsible for generating a digital phaseword for the port's PLL. These phasewords represent the fill level of the Reassembly Circular Buffer(s) for a port.

In UDT mode, if it is determined that a VC is cut (see Section 4.6.2.1 on page 88), no cells are being received at the UDT RX_SAR. As a result, there is no frame of reference with which to adjust the output TDM clock rate. Accordingly, the PLL is placed into holdover mode until cells are once again being received on the VC. At that point, the output clock rate can be adjusted based on the buffer fill level.

For more information, see Section 4.7.2.6, "Adaptive Clock Recovery Circuit," on page 103.

RTS Reception for SRTS Clock Recovery

Although the actual SRTS clock recovery processing is a function of the Clock Management module of the MT90528 device, the UDT RX_SAR and the SDT RX_SAR are responsible for the extraction of RTS nibbles from incoming cells, for transfer to the clocking module.

In order to provide SRTS clock recovery, the UDT RX_SAR and SDT RX_SAR extract the RTSs (Residual Time Stamps) carried in the CSI bits of received ATM cells. Each time an odd-sequence-numbered cell from a pre-selected VC arrives, the RX_SAR extracts the CSI bit from the AAL1 header byte for the cell and stores it. When the entire RTS nibble (4 bits) has been received, it is transmitted to the Clock Management module of the MT90528 device.

In UDT mode, there is only one VC per TDM port, so the user may select it to recover RTS timing information by setting the **S (SRTS Enable)** bit in the UDT Reassembly Control Structure for the port's VC. In SDT mode, it is possible to have multiple VCs per TDM port; however, the user may select only a single VC as the source of clock recovery data for a port (the port identified by the VC TDM Port field). This selection is made by setting the **S (SRTS Enable)** bit in the SDT Reassembly Control Structure for the selected VC.

SRTS clock recovery within the MT90528 device is performed on a per-port basis, with a maximum of one VC per port carrying clocking information. Because there is only one RTS Reception sub-module to handle all of the UDT VCs (and another RTS Reception sub-module for all of the SDT VCs), variables associated with the recovery of the individual RTS bits are stored in internal memory (in the form of fields within the Reassembly Control Structures for the VCs).

Because RTS values are extracted from received cells, there is always the possibility of error (e.g., cells are received out of order, so the RTS bits are also in the wrong order). As such, a protection mechanism is included in the RTS extraction sub-module. Each time that the RX_SAR sends an RTS nibble to the port's Clock Management module, it also sends an extra bit. This bit indicates whether the current RTS value is valid. If the RTS value is invalid, the PLL discards the RTS value (as well as the locally-generated RTS value used for comparison). The PLL goes into holdover mode, in which the output clock rate is not adjusted based on the input signals. When the next "valid" RTS value is received, the PLL resumes making adjustments to the output clock rate.

For more information, see Section 4.7.2.5, "Receive SRTS Circuit Sub-Module," on page 102.

Note that in SDT mode, when using SRTS clock recovery, the MT90528 can have a maximum of 32 channels per VC. Also, no support for SRTS clock recovery is provided when operating in CAS mode.

4.6.2 Timeout Circuitry

The timeout circuitry is used to perform a variety of tasks related to the inter-arrival time between two consecutive cells on a VC.

4.6.2.1 Cut VC Monitoring

The first task performed by the timeout circuitry is related to the per-VC MIB statistic, **atmfCESCellLossStatus**. According to the CES standard, this integer-valued status field must be set to a loss value "when cells are continuously lost for the number of milliseconds specified by **atmfCESCellLossIntegrationPeriod**". Within the MT90528, rudimentary support for this statistic is provided on a per-VC basis. This functionality is supported via the **VC Arrival** (**V**) bit within each UDT/SDT Reassembly Control Structure. This bit is set by the UDT RX_SAR or the SDT RX_SAR each time a cell arrives on a particular VC. However, the CPU can, via software, clear this bit to a value of '0'. Software can then monitor the value of this bit at regular intervals. If the bit is still '0' when polled, no cells have been received on the VC since the bit was last cleared by the CPU. If the bit is still '0' after a user-configurable period of time, as defined within the user's software, a cut-VC (cell loss) may be declared. Therefore, the usage of this control structure bit, with software support, provides per-VC timeout monitoring as defined within the CES specification.

In addition to the above per-VC monitoring, the MT90528 also features extra cut-VC monitoring in the UDT case. This extra functionality is provided on a per-port basis (note that for the UDT mode of operation, per-port is the equivalent of per-VC). In order to enable this monitoring, the user must configure the MIB Timeout Configuration Register at byte-address 3000h to set the **Reassembly Cell Loss Integration Period**. The value written in this field is used by each of the per-port timeout circuits in the MT90528 (i.e., it is a device-wide value and is not programmable on a per-port basis). The value within the field is expressed in terms of milliseconds and has a default value of 2.5 s. When any of the 28 per-port timeout counters reaches the timeout period without a cell arriving on the VC for the port, the **CUT_VC_STATUS** bit for the port is set in the port's corresponding Timeout Configuration Register.

4.6.2.2 Late Cell Insertion

In UDT mode, the MT90528 provides per-port CDV monitoring. The user must, on a per-port basis, configure the **LATE_CELL_PERIOD** field in the port's Timeout Configuration Register. The value within the field is expressed in terms of 125 μs increments, and has a default value of 256 ms. If an internal counter reaches the LATE_CELL_PERIOD, the **LATE_CELL_STATUS** bit for the "late" VC will be set in the Timeout Configuration Register for the port.

Additionally, as explained in section "UDT Mode of Operation" on page 74, if the UDT RX_SAR has been configured by the user to insert dummy cells in late-cell cases and the internal counter reaches LATE_CELL_PERIOD, a dummy cell will be inserted into the port's UDT Reassembly Circular Buffer.

4.6.2.3 Underrun Detection

The per-port timeout circuitry provides underrun detection in the UDT mode of operation.

In UDT mode, underruns are detected automatically if the TDM read pointer to a UDT Reassembly Circular Buffer is ever equal to the UDT RX_SAR's current write pointer for the corresponding port. An underrun is noted because the TDM module is reading an address within the UDT Reassembly Circular Buffer which has yet to be written by the UDT RX_SAR. When a UDT underrun is detected, notification is sent to the UDT RX_SAR, so that it can make adjustments to its next write pointer value, and so that the MIB statistics can be updated accordingly. At the same time, notification of the underrun is sent to the TDM module, causing the TDM module to output silence data (i.e., all ones) on DSTo for the port, until the underrun condition is resolved.

4.6.3 Data RX_SAR Module

Whereas the UDT RX_SAR and SDT RX_SAR handle CBR AAL1 cells, the Data RX_SAR handles non-CBR data cells. These cells may be AAL5 signalling cells, OAM-type data cells, or any other ATM cells which are received on VCs which meet the VPI/VCI matching restrictions of the UTOPIA interface of the MT90528.

The Data RX_SAR does not process or manipulate the data cells. Rather, it simply accepts cells which have been sent to it by the UTOPIA's VPI/VCI filter mechanism. Once cells are accepted by the Data RX_SAR, they are stored in a multi-cell circular buffer in external memory, where they can be analyzed by a CPU, under software control.

4.6.3.1 Mode of Operation

Unlike the UDT RX_SAR and the SDT RX_SAR, the Data RX_SAR within the MT90528 can be disabled (default = "off"). Unless enabled by setting the **Data RX_SAR Enable** bit in the Data RX_SAR Control Register at address 2020h, the Data RX_SAR ignores any incoming data cells, even if they are recognized as data cells by the UTOPIA module.

The entire 54-byte received cell (i.e., 5 bytes of header, 1 "filler" header byte (UDF2 field) required for the 16-bit UTOPIA bus, and 48 bytes of payload) is copied to a location in external memory which is identified by the Data RX_SAR Cell Buffer base address and a hardware write pointer. The base address of the buffer is user-programmable (in the Data RX_SAR Configuration Register at 2024h), as is the number of cells that can be stored

in the buffer. The user can select (via the register at byte address 2024h) a buffer capable of holding 16, 32, 64, or 128 cells. Each cell is allocated 64 bytes in external memory.

A particular cell entry within the buffer is selected to be written to via the Data RX_SAR write pointer. The write pointer can not be modified by the CPU; therefore, following the assertion of Data RX_SAR Enable, writes always begin at cell location #0 within the buffer.

Received Data Cell Counter

The Data RX_SAR also provides the user with the number of data cells received from the UTOPIA block. This 16-bit counter value can be viewed in register DRCCR at address 202Ah. This counter is incremented every time a data cell is received from the UTOPIA. It is not reset when the Data RX_SAR is disabled. When this counter rolls over, a status bit gets set in the DRSR register at address 2022h. This status bit can be cleared by software. This rollover condition can also generate a service request to the CPU if the corresponding service enable bit is set in the DRCR register at address 2020h.

4.6.3.2 Error Handling

In order to prevent the CPU from reading cell locations that have not yet been written, a register is provided to store the value of the CPU's read pointer. Upon start-up, this register is reset to point to the final cell location within the buffer. In general, to prevent slip conditions, software should be designed to ensure that the CPU's read pointer is never pointing to a cell location pointed to by the Data RX_SAR write pointer. During a cell-write operation, the write pointer indicates the cell location which is currently being written (the cell is not yet valid for reading). At the end of the write process, the write pointer is incremented, pointing to the cell location which will be written with the next received data cell. Contrarily, the CPU's read pointer should be incremented at the beginning of a cell-read, to point to the cell location that is **currently** being read. At the end of a cell-read, software should **not** increment the read pointer.

The **Data RX_SAR Cell Arrival** status bit is provided to permit greater software control. This bit in the Data RX_SAR Status Register (address 2022h) is set each time that a cell has been completely written into the Data RX_SAR Cell Buffer. The bit signifies to the CPU that valid data has been written into the buffer. Software can clear this status bit by performing a write of '0' to the register bit location.

At the end of each cell-write cycle, a comparison is made between the CPU's read pointer and the Data RX_SAR's write pointer. If the write pointer is at a distance of half the buffer size from the CPU's read pointer, a buffer half full condition is flagged by setting a status bit (**Data RX_SAR Buffer Half Full**) in the Data RX_SAR Status Register (DRSR). Software can clear this bit by writing '0' to the register bit location.

If a buffer half full condition is not detected, the CPU's read pointer is compared to the Data RX_SAR's write pointer. If they are equal, an overrun condition is flagged by setting a status bit (**Data RX_SAR Cell Buffer Overrun Error**) in the Data RX_SAR Status Register at address 2022h. This status bit can be cleared by performing a write of '0' to the register bit location. The overrun status bit may be interpreted by the user's software in two possible ways:

- If the CPU is in the middle of a read operation (i.e., it has started processing a cell in the buffer, but has not read the entire cell), this flag signifies that a buffer overrun event has occurred - the Data RX_SAR has over-written the cell location which is being read by the CPU. In this case, software should discard the portion of the cell already read by the CPU and advance the read pointer so that it is pointing to a valid cell location.
- On the other hand, if the CPU is not performing a read operation, the flag signifies that a buffer overrun is about to occur. Specifically, an overrun could occur on the next cell-write. If the CPU does not read the complete subsequent cell in the buffer before the next cell-write occurs, any data stored in that cell location will be overwritten by the Data RX_SAR. As such, the next cell (which may or may not actually be overwritten) should still be treated as corrupted.

4.7 Clock Management Module

The Clock Management module of the MT90528 is designed to provide both clock control and clock recovery functions. The primary control function of the module is to generate clock signals and frame pulses to be output via the MT90528's TDM interface. With regard to clock recovery, the Clock Management module is responsible for performing synchronous clock recovery, Synchronous Residual Time Stamp (SRTS) clock recovery, and Adaptive (ACM) clock recovery, as required to meet the CES specification, af-vtoa-0078.000.

4.7.1 Overview

4.7.1.1 Clock Control

When the DS1/E1 ports of the device are operating in UDT mode, the Clock Management module generates the per-port PCM output clocks required to interface with LIUs or framer/LIUs, based on a user-selectable clock source. When operating in SDT mode, the Clock Management module generates the output clock signals as in UDT mode. However, rather than interfacing with LIUs or framer/LIUs, these signals are output to framer devices.

TDM backplane mode is a sub-set of SDT operation in which the MT90528 device interfaces directly to a TDM backplane. In this mode, each TDM port of the device is serviced by a common clock in both the input and output directions. When operating in TDM backplane mode, the Clock Management module is responsible for the generation of bidirectional clock and frame pulse signals. In order to support a variety of customer applications, the clock can be running at either once or twice the TDM data rate.

When operating in backplane slave mode, the backplane clock signal and frame pulse are routed directly from the external pins through the Clock Management module to the TDM bus module. Contrarily, when the MT90528 is operating as the TDM backplane master, it is the responsibility of the Clock Management module to generate both the clock and frame pulse signals. These signals are transmitted to external device pins as well as to the TDM bus module.

As a secondary clock control function, the Clock Management module always provides a continuous TDM line rate clock to the TDM bus module when operating in UDT mode. In the event of a Loss of Signal (LOS) condition, the Clock Management module automatically routes the port's internally-generated PLL clock to the TDM bus module if the user has selected the port's STiCLK as the source for SToCLK. The TDM bus module uses a user-programmable configuration bit (TDM_LOS_CLK in the per-port TDM Control Register 1) to select either the external input clock for the port or the port's internally-generated PLL clock as the source of the TDM sampling clock.

As a clock control function which permits clock recovery at the remote end, the Clock Management module generates Residual Time Stamp (RTS) signals based on the relationship between the network clock and the local bit-rate clock, on a per-port basis. In the segmentation direction, the RTS values are output to the TX_SAR header generation module, where they are inserted into ATM cells for transmission to the remote end.

4.7.1.2 Clock Recovery

In order to meet the CES specification for SDT and UDT operation, the MT90528 provides synchronous, SRTS, and adaptive clock recovery methods.

The MT90528 permits synchronous clock recovery in UDT, SDT, and TDM backplane modes. The MT90528 provides synchronous clock recovery via either an internal PLL or an external PLL. In order to comply with the CES specification, the reference source for the optional external PLL must be traceable to a Primary Reference Source (PRS). The user has the option of sourcing the external PLL from a network clock, clocks generated by the MT90528's internal PLLs, or TDM input clocks.

SRTS clock recovery is provided as outlined in U.S. Patent No. 5,260,978. Although the CES specification indicates that SRTS is not required for SDT clock recovery, the MT90528 device permits the use of SRTS in the SDT mode of operation when not operating in the CAS sub-mode. In the reassembly direction, RTS values extracted from

incoming ATM cells by the UDT RX_SAR or SDT RX_SAR are input to the Clock Management module. Within this module, the RTS values are compared with the network clock and a new line-rate clock is generated by an internal PLL. This clock may be sent directly to the TDM bus module for use as a TDM output clock or it may be used as a reference clock for an external PLL.

Adaptive clock recovery is performed by the Clock Management module on a per-port basis, based on the fill level of the Reassembly Circular Buffers.

An overview of the functionality of the Clock Management module is given in Figure 32.

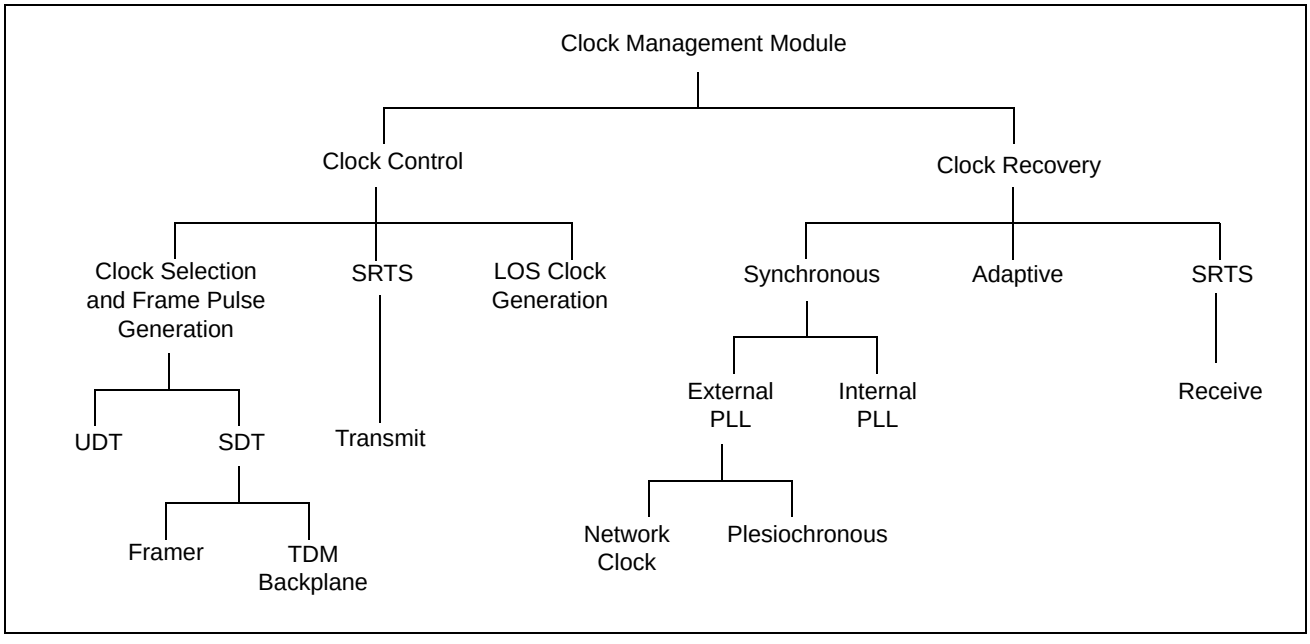
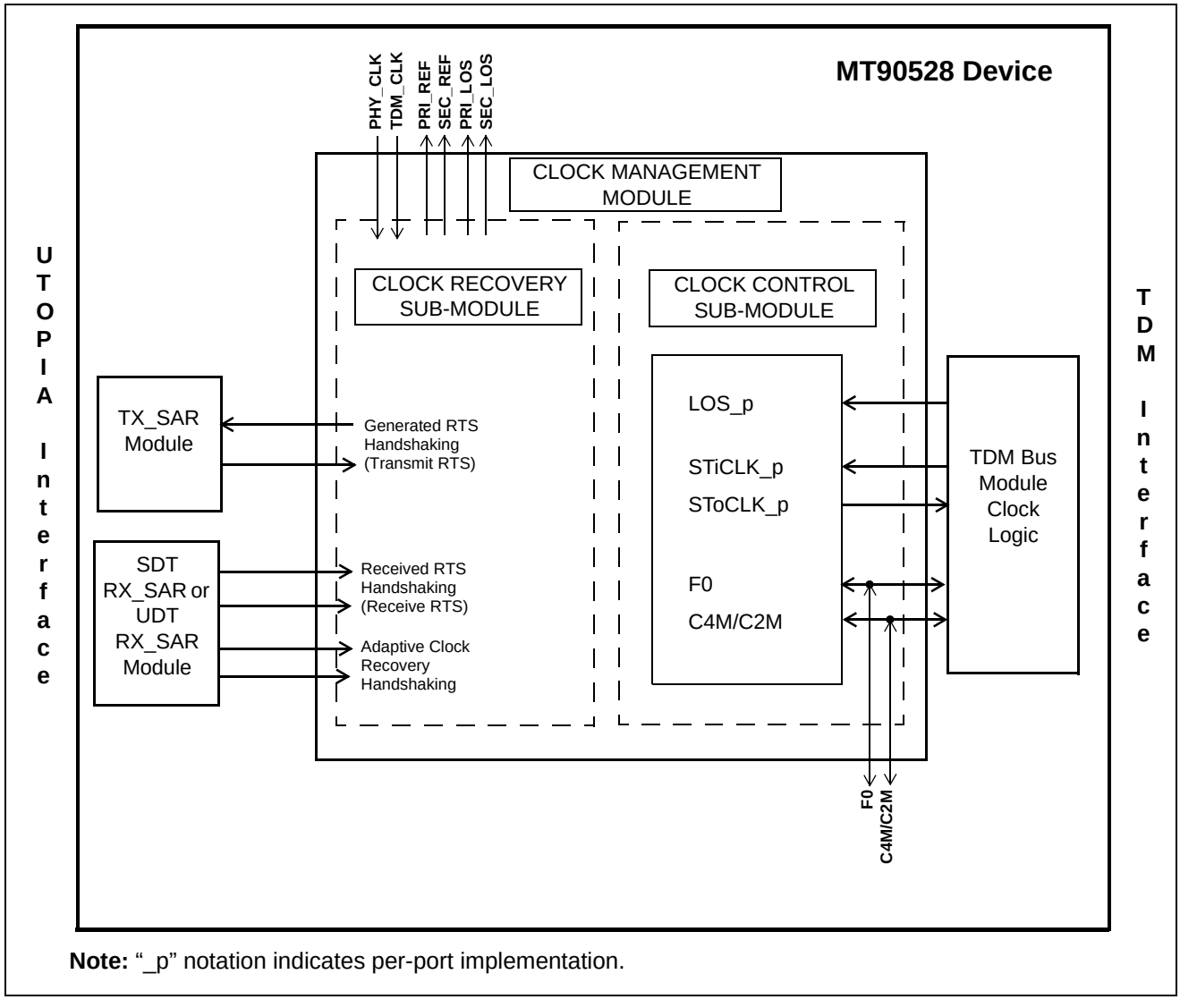


Figure 32 - Functions of the Clock Management Module

At a high level of abstraction, Figure 33 gives a general overview of the interaction between the Clock Management module and other modules within the MT90528 device. The internal configuration of the Clock Management module is examined more fully in the subsequent sub-module descriptions.



Note: "_p" notation indicates per-port implementation.

Figure 33 - High-Level Block Diagram of the Clock Management Module

4.7.2 Functional Description

4.7.2.1 Interface to TDM Sub-Module

This sub-module acts as the interface between the Clock Management module and the TDM Interface module. STiCLK_p signals received at the TDM interface are input to this sub-module and are directed to other portions of the Clock Management module. In the output direction, SToCLK_p, C4M/C2M, and framing signals are generated by this sub-module for output to the TDM Interface module. The user has full programmability to select the source of the output clock for each TDM port.

A single interface is used to communicate with the TDM Interface module when using either UDT or SDT formatting. A separate interface and additional clocking circuitry are provided for operation in TDM backplane mode. Both interfaces and the associated circuitry are shown in Figure 34 on page 95 and are explained more fully in the text which follows.

Operation of SDT/UDT Interface

There are 4 possible user-selectable clock sources for SToCLK:

- the STiCLK signal for the port
- the clock generated by the port's internal digital PLL and transmitted via PLLCLK
- a synchronous clock generated from one of a number of user-selectable sources. This is a common clock which is available to all of the DS1/E1 ports of the MT90528.
- a divided-down version of the system clock (MCLK/2).

The user is able to select the desired clock source via the CLKSEL bits (found in the per-port Clocking Configuration Register at 5200h + p*10h), with MCLK/2 being the default clock which is output on SToCLK. In the event of an LOS condition, the multiplexer automatically selects the port's PLLCLK reference to be output on SToCLK, if the user had originally selected to use STiCLK as the source of SToCLK. In this way, even if the port's TDM input clock signal fails, the SToCLK signal is still valid. (**Note:** The port's internal PLL goes into holdover mode upon receiving the LOS indication.)

The user selects (via register bits) what type of clock is generated by the internal PLL. This clock may have one of the following possible sources:

- a synchronous clock generated using the port's STiCLK input reference (in Line Clocking mode)
- a synchronous clock generated using a network reference (in Network mode)
- the SRTS-recovered clock for the port (in SRTS mode)
- the clock generated using Adaptive Clock Recovery methods for the port (in Adaptive mode).

More information about the PLL implementation can be found in Section 4.7.2.7, "Internal Digital PLL Sub-Module," on page 104.

Operation in TDM Backplane Mode

When operating in TDM backplane mode, there are two signals which are exchanged between the backplane and the MT90528 device: F0 and C4M/C2M. These bidirectional signals (inputs when the MT90528 is slaved to the backplane; outputs when the MT90528 is the backplane master) are generated only once per device. Unlike the per-port clock and framing signals, these signals are directed into the Clock Management module from the external pins. These signals are then transferred to the TDM bus module.

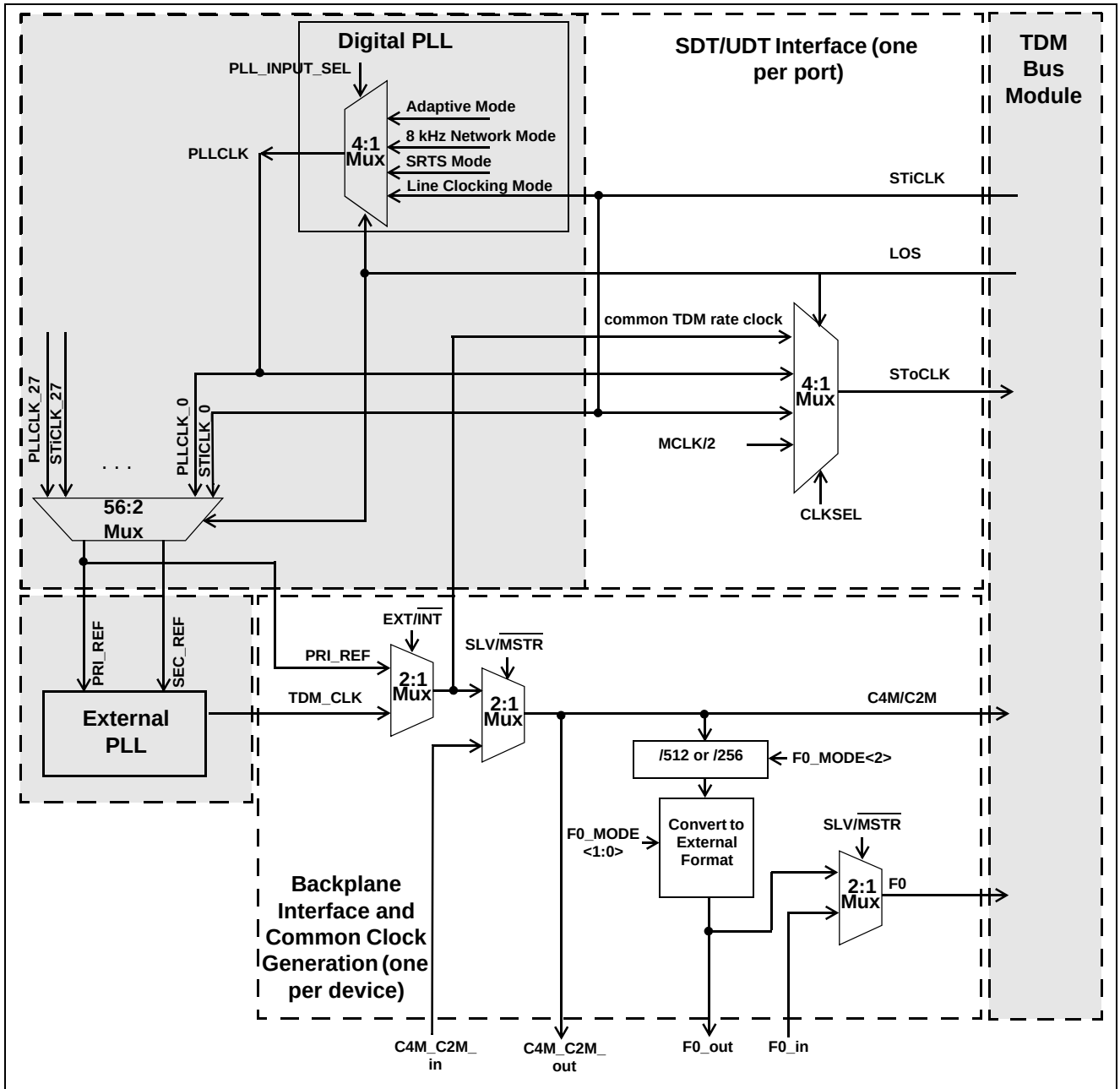
If the MT90528 is operating in slave mode, the C4M/C2M signal is routed to the TDM bus module, where it is used as both the sample and drive clock for each of the DS1/E1 ports. The F0 signal from the external pin is transmitted, unchanged, to the TDM bus module.

When operating in master mode, the Clock Management module generates both the C4M/C2M signal and the F0 signal. These signals are transmitted to external device pins as well as to the TDM bus module. The C4M/C2M signal is generated from a common TDM line rate clock, as explained in Section below. The internal frame pulse signal, F0, is generated as a divided-down version of the C4M/C2M clock. The frame pulse signal is configured to a user-programmable format (either an ST-BUS or Generic frame pulse) prior to being output to both the TDM bus module and the F0 pin.

Common Clock Source Generation

An additional function of the circuitry shown in Figure 34 is the generation of a common TDM line rate clock for use by all of the DS1/E1 ports of the MT90528 device when it is **not** in backplane mode. The user is able to select the source for this signal (labelled as common TDM rate clock in Figure 34) as coming from either an internal or an external reference. If an external reference is selected, the common clock is sourced from the TDM_CLK pin. On the other hand, should the user not want to employ an external PLL, an internal reference may be selected. In this case, the common clock comes from the PRI_REF reference signal. The PRI_REF signal, which is explained in

Section 4.7.2.2, “Synchronous Clocking Circuit” may be sourced from the internal PLL clock or the TDM input clock for any DS1/E1 port of the device.



Note1: Shaded sections of figure above indicate circuitry outlined elsewhere in this document.
Note2: The SDT/UDT interface is replicated on a per-port basis. The backplane interface and common clock generation circuitry are only implemented once per device.

Figure 34 - Interface to TDM Bus Module and Common Clock Generation Circuitry

4.7.2.2 Synchronous Clocking Circuit

There are two possible options for generating a synchronous clock which is traceable to a Primary Reference Source (PRS). The first option, referred to as Synchronous Clock #1, is generated via an internal digital PLL. The second, Synchronous Clock #2, is provided via an external PLL. These options are available for UDT, SDT, and TDM Backplane modes of operation.

Synchronous Clock #1 (Internal Digital PLL)

Each port within the MT90528 device has its own internal digital PLL. Refer to Section 4.7.2.7, “Internal Digital PLL Sub-Module,” on page 104 for information regarding the specifics of the design and its operation. This PLL performs various functions within the MT90528, including SRTS clock recovery (outlined in Section 4.7.2.5), adaptive clock recovery (described in Section 4.7.2.6), and PRS-traceable clock generation, which is explained here. Each PLL continuously generates a clock which runs at the TDM line rate.

In this mode, the reference clock for all of the PLLs is provided by an 8 kHz clock, derived as a divided-down version of the network clock. The generation of this reference clock is explained in Section 4.7.2.3 on page 98. The implementation of the synchronous clock generation is shown in Figure 35.

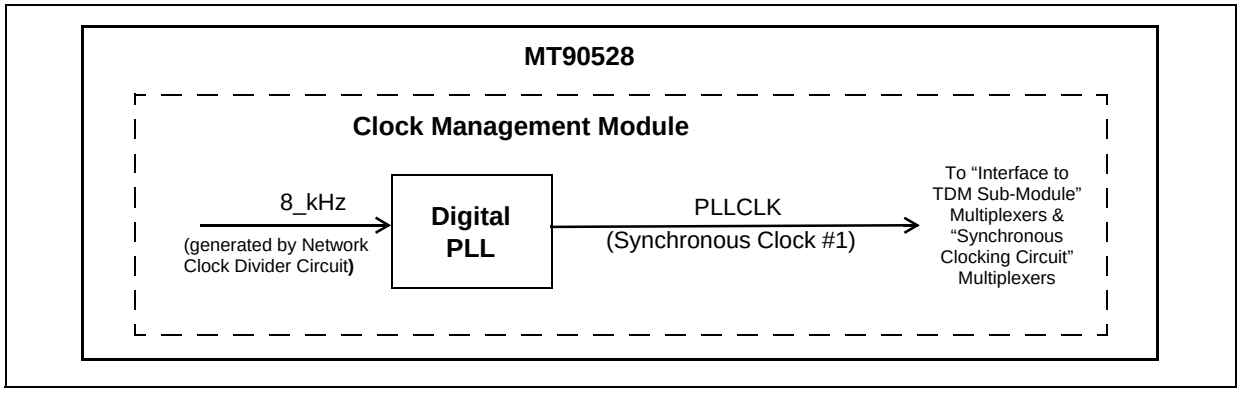


Figure 35 - Synchronous Source Multiplied to TDM Bus Rate by Internal PLL

The clock output from the PLL (PLLCLK for each of the DS1/E1 ports) is transmitted to the port’s corresponding SToCLK multiplexer.

Synchronous Clock #2 (External PLL)

As an alternative to the internal PLL, an external PLL may be used to provide a synchronous clock for transmission onto the TDM output bus. Using this method, a PRS-traceable signal from an external PLL is input to the MT90528 via the TDM_CLK pin. Since this is a “common” clock signal (i.e., one per device), TDM_CLK is routed to a multiplexer, as shown previously in Figure 34. The output of this multiplexer is a common clock which is routed to the clock selection multiplexers (one per port) in the “Interface to TDM sub-module”, detailed previously in Section 4.7.2.1. The implementation of the synchronous clock generation is shown in Figure 38.

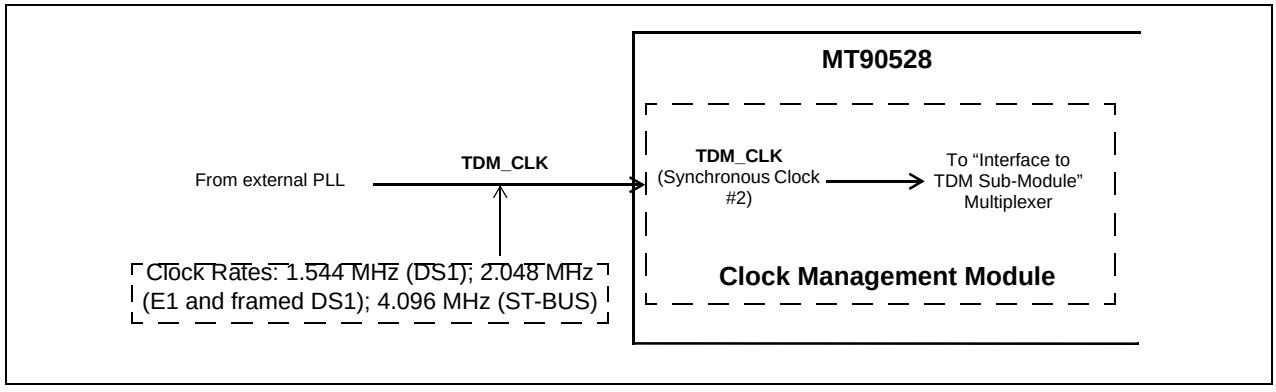


Figure 36 - Synchronous TDM-Rate Clock Generated by External PLL

Although the simple process outlined above provides synchronous clocking, the MT90528 also provides circuitry internal to the device which allows the use of plesiochronous clock recovery methods. Using the circuitry shown in Figure 37, the user is able to select a signal to provide a reference clock for the external PLL. The sources available are the per-port STiCLK inputs and the PLLCLK signals which are generated or recovered for each DS1/E1 port of the MT90528.

The user can select the STiCLK input or the internal PLL clock from any DS1/E1 port to serve as a reference signal for the generation of SToCLK for any other port. The user is able to choose any of the 56 (2 * 28 ports) sources for the primary reference (PRI_REF), and any of the 56 sources as the secondary reference (SEC_REF). PRI_LOS and SEC_LOS are set to their selected port’s LOS. The user selection for PRI_REF is overridden in an LOS condition to always provide the corresponding port’s internal PLL clock as the primary reference. The user selection for SEC_REF is not overridden by an LOS condition.

It is up to the user to select mutually-exclusive sources for the external PLL if redundancy is the goal. Regardless of whether the primary or secondary reference is used, the external PLL output must be programmed to match the desired line rate. The line rate signal which is output from the external PLL is input to the MT90528 device at the TDM_CLK input pin. Alternatively, if the user does not wish to use an external PLL, the PRI_REF signal can be routed directly to the “common clock” multiplexer described previously. This implementation was shown in Figure 34.

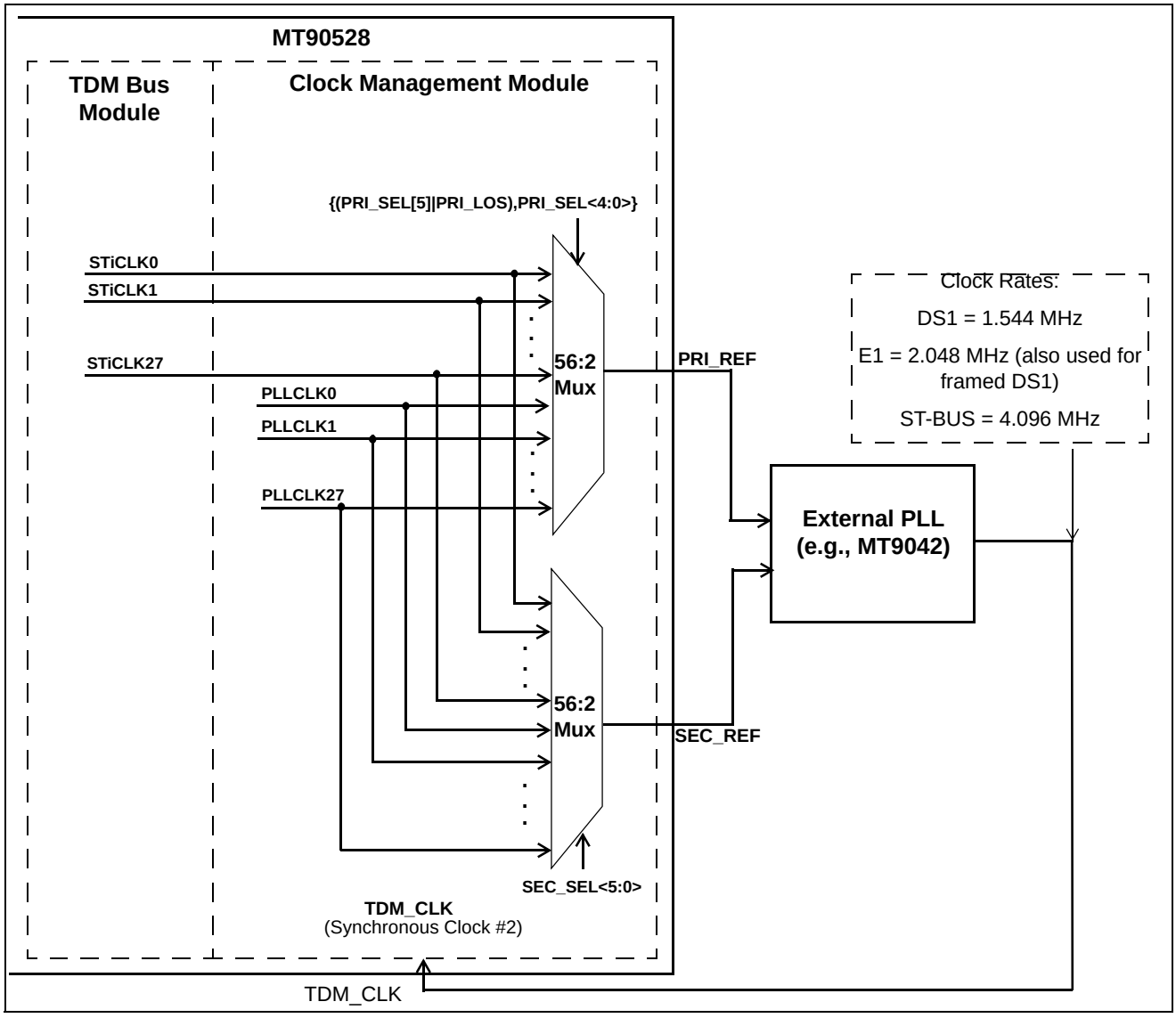


Figure 37 - Synchronous TDM Rate Clock Generated by External PLL User-Selectable References

4.7.2.3 Network Clock Divider Circuit

This sub-module is implemented only once within the MT90528 device and is used by both the Transmit SRTS and Receive SRTS processes. The required circuitry is shown in Figure 38.

The primary function of this sub-module is to create a divided-down network clock, fnxi, from a PHY rate clock (19.44 MHz) which is obtained from an external pin. This sub-module generates a number of different clock rates in accordance with the requirements of the SRTS patent and the CES specification.

When operating in UDT mode, only a single multiplexer is required for RTS generation and SRTS clock recovery. Since all of the VCs contain the same amount of data, only one network clock rate is required. This rate is set out in the CES specification, af-vtoa-0078.000, as 2.430 MHz.

In SDT mode, additional network clock rates are required because the size of the transmitted VCs can differ. The MT90528 permits RTS generation and SRTS clock recovery to be conducted on two different VC sizes (ranging from n = 1 to n = 32) for each device configuration.

A secondary function of the network clock divider circuit is the generation of an internal 8 kHz clock signal from the 19.44 MHz network clock. This 8 kHz signal can then be used as a reference clock to the internal PLLs outlined in Section 4.7.2.7. As an alternative, if the user wishes to provide his own 8 kHz reference for the internal PLL, an 8 kHz signal can be input directly on the PHY_CLK pin, provided that SRTS clock generation/recovery will not be used.

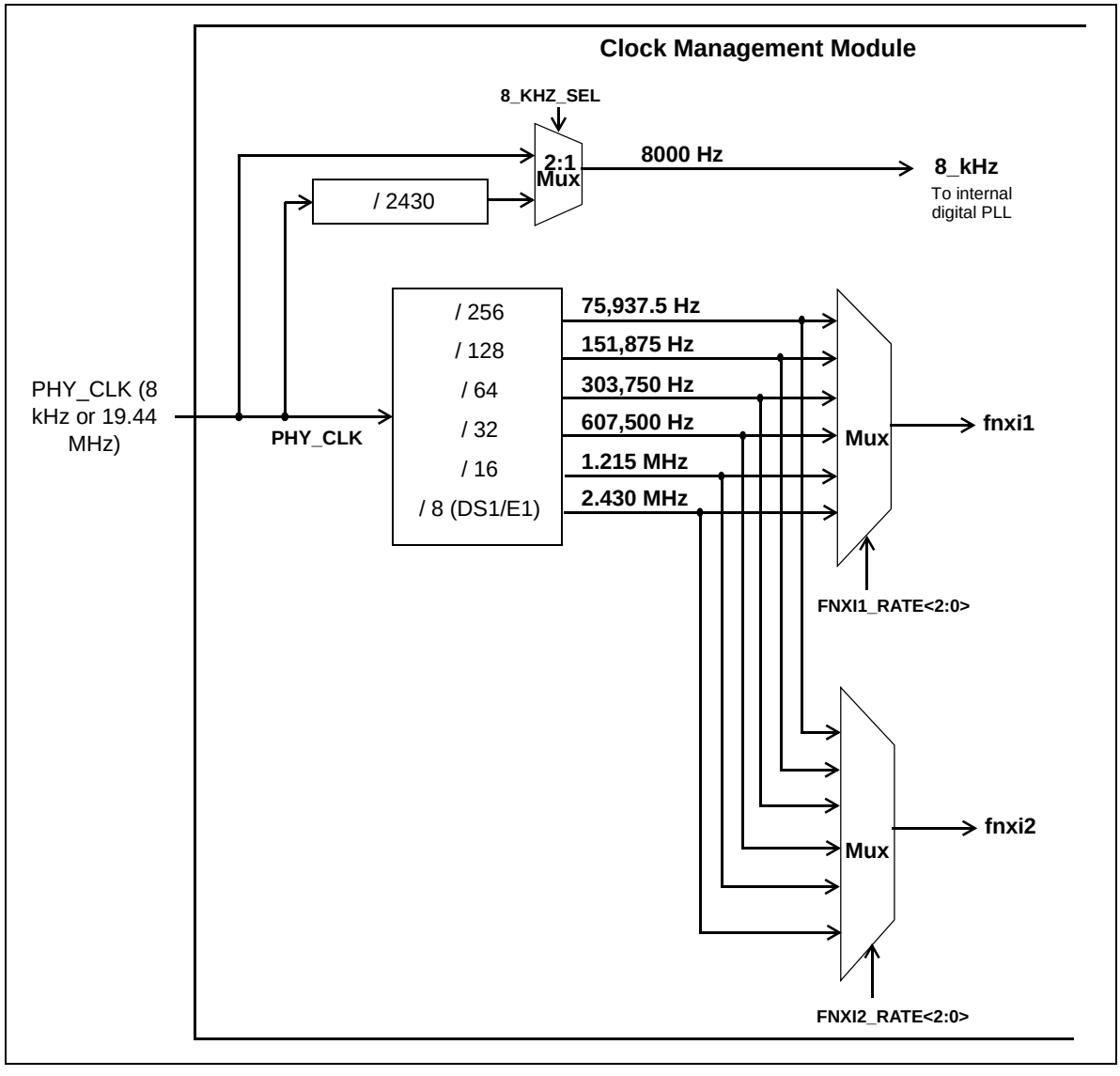


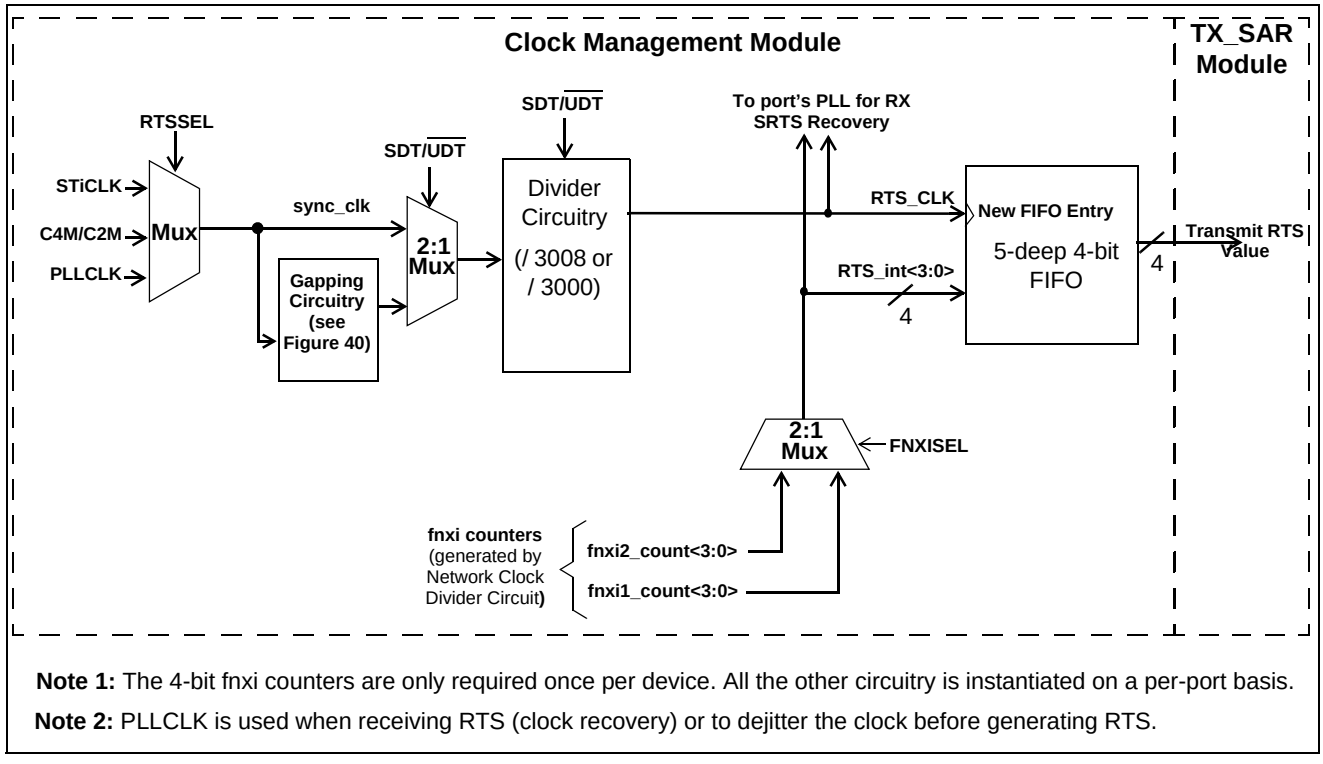
Figure 38 - Network Clock Dividers

4.7.2.4 Transmit SRTS Circuit Sub-module

In the segmentation direction, the purpose of the transmit SRTS circuit sub-module is to generate 4-bit Residual Time Stamps (RTSs) to be inserted within the headers of ATM cells output on the UTOPIA bus. In the reassembly direction, this circuit is used to generate local RTS values which are compared (by an internal PLL) with the RTS values extracted from received cells. Segmentation operation is explained in this section, but the reassembly function is discussed in Section 4.7.2.5, “Receive SRTS Circuit Sub-Module”.

As outlined in U.S. Patent No. 5,260,978, in the segmentation direction, the transmit SRTS circuit compares the local clock rate, determined by STiCLK for a particular port (in independent clocking or ST-BUS backplane mode) or

C4M/C2M (when operating in Generic backplane mode) with the output of an fnxi counter clocked by the Network Clock Divider circuit examined in Section 4.7.2.3 on page 98. The result of the comparison is stored in a FIFO, for eventual transmission of the RTS nibbles to the TX_SAR. Underrun and overflow detection are provided on the Transmit SRTS FIFO via status bits in CPU-accessible registers. The circuit operates in essentially the same way in the reassembly direction, except that the local clock rate is determined by the clock at the output of the port's internal PLL, PLLCLK. As well, in the reassembly direction, data is sent to the Receive SRTS sub-module rather than being sent to the Transmit SRTS FIFO. Figure 39 shows how the circuit is implemented.



Note 1: The 4-bit fnxi counters are only required once per device. All the other circuitry is instantiated on a per-port basis.

Note 2: PLLCLK is used when receiving RTS (clock recovery) or to dejitter the clock before generating RTS.

Figure 39 - Transmit SRTS Sub-module

UDT Operation

The STiCLK or PLLCLK signal for each port (C4M/C2M isn't used, because it is an SDT-mode signal) is divided down to generate a clock, RTS_CLK. This clock has the same frequency as a cycle of RTS. Since one RTS value is transmitted over the course of 8 cells, the division is by 3008, the number of payload bits transmitted within one RTS period (8 cells containing 47 payload bytes). Every time RTS_CLK pulses, the current value of the appropriate fnxi counter is stored in a FIFO. A value from the FIFO is transmitted to the TX_SAR cell header generator circuit once every 8-cell sequence.

SDT Operation

In some cases, the STiCLK/C4M/C2M/PLLCLK input clock requires modification prior to being used in the RTS generator circuit described above. The line rate clock (i.e., 2.048 MHz for DS1/E1/backplane) which is input to the MT90528 represents the rate at which bits are being received on a particular port. In SDT mode, the line rate only represents the bit rate of a VC if the entire stream (e.g., 32 channels in ST-BUS mode) is transmitted in a single VC. For all other cases (i.e., for N-channel VCs, where N is less than the maximum number of channels on a port), the RTS-generating clock must represent the bit rate of a particular VC. This bit rate is determined by the number of channels transmitted within a VC. Figure 40 below shows the line rate clock being passed through the gapping divider circuitry to generate a bit-rate clock.

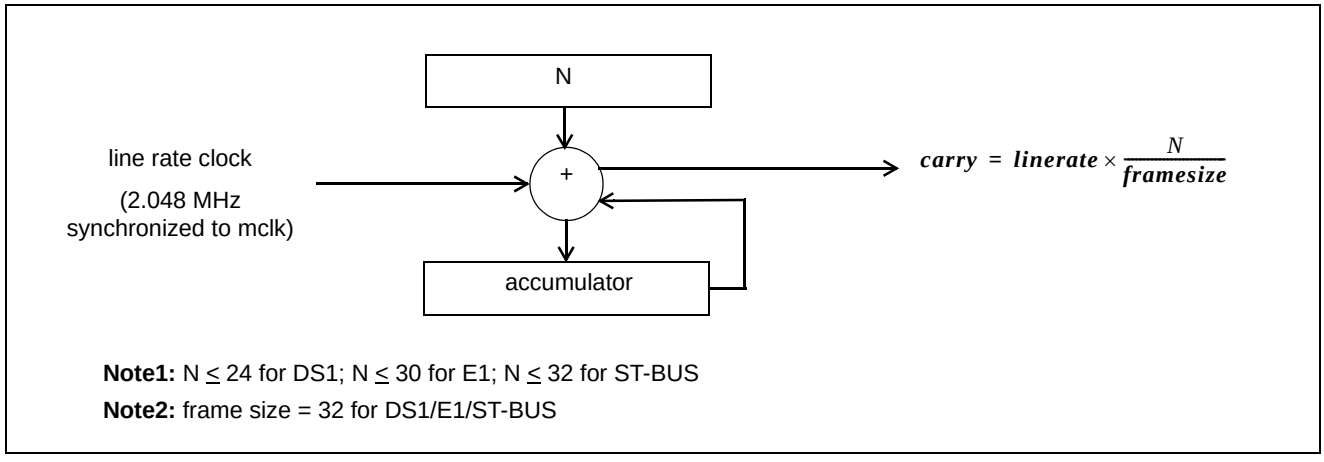


Figure 40 - Gapping Circuitry for SDT Operation

The gapping circuit operates as follows: the line rate clock (STiCLK, C4M/C2M, or PLLCLK) must be equal to a framed clock rate. For DS1, E1, and backplane modes, this rate must be 2.048 MHz. However, the user must provide this clock differently, depending on the mode being employed. If the port is operating in **independent** clock mode, the 2.048 MHz clock is presented on STiCLK and the user should select the port's STiCLK as the source for the RTSSEL mux. When operating in **Generic backplane** mode, the desired 2.048 MHz clock rate is available at C4M/C2M. Therefore, the user should select C4M/C2M as the source for the RTSSEL mux. When operating in **ST-BUS backplane** mode, the C4M/C2M signal has a clock rate of 4.096 MHz. This clock is too high to be the line rate clock for the port. Therefore, the user must provide an appropriate 2.048 MHz clock on the STiCLK input for the port. The user must then select the STiCLK input as the source of the RTSSEL mux. This half-rate STiCLK signal will not be used elsewhere in the port's circuitry, because the TDM module will use the C4M/C2M clock if it is programmed in backplane mode. In any case, the signal which is output from the RTSSEL multiplexer is input to the circuit at "line rate clock". "N" in the above figure represents the number of channels in the VC (N ≤ 24 for DS1; N ≤ 30 for E1; N ≤ 32 for ST-BUS). Adding the number of channels to the accumulator at the rate of the line rate clock, the "carry" of the adder provides the desired clock rate. For example, if using a 2.048 MHz line rate with an 18-channel VC, we want to achieve the following result: carry = 2.048 MHz * (18/32) = 1.152 MHz. Looking at the hardware implementation, we would see the following:

N	accumulator output	accumulator input	carry
18	0	18	0
18	18	4	1
18	4	22	0
18	22	8	1
18	8	26	0
18	26	12	1
18	12	30	0
18	30	16	1
18	16	2	1
18	2	20	0
18	20	6	1
18	6	24	0

Table 20 - Sample Gapping Circuitry Calculation (N = 18)

N	accumulator output	accumulator input	carry
18	24	10	1
18	10	28	0
18	28	14	1
18	14	0	1
18	0	18	0
...	...	...	...

Table 20 - Sample Gapping Circuitry Calculation (N = 18)

Thus, the “carry” signal results in the desired clock rate (in this case, it is slightly greater than 1/2 the line rate clock).

After the gapping circuitry, the resulting clock (carry) is divided by 3000, which represents the number of payload bits transmitted within one RTS period (7 cells containing 47 payload bytes, and one cell containing 46 payload bytes). As with UDT operation, every time RTS_CLK pulses, the current value of the fnxi counter is stored in a FIFO. A value from the FIFO is transmitted to the TX_SAR cell header generator circuit every 8-cell sequence.

Note: Because of the divide-by-3000 circuitry, the TX SRTS circuitry won’t work when a VC is set up for the SDT w/ CAS mode of operation. The problem is caused by the fact that there aren’t necessarily 3000 TDM payload bits in an 8-cell cycle in these operational modes. Therefore, RTS nibble generation and SRTS clock recovery are only supported in “basic” SDT operation.

4.7.2.5 Receive SRTS Circuit Sub-Module

The receive SRTS circuit sub-module generates a bit-rate clock based on RTS values extracted from the headers of ATM cells received on the UTOPIA bus.

As outlined in U.S. Patent No. 5,260,978, the receive SRTS circuit generates a recovered clock based on a comparison between the incoming RTS values and the network clock, fnxi. This comparison provides enough information to re-create the remote (transmit) clock at the local end.

The Receive SRTS circuitry is quite simple, consisting only of a FIFO and a digital PLL, as seen in Figure 41. In addition, the Receive SRTS circuit makes use of signals generated within the Transmit SRTS circuitry, explained in Section 4.7.2.4. These pre-generated signals are also shown in Figure 41.

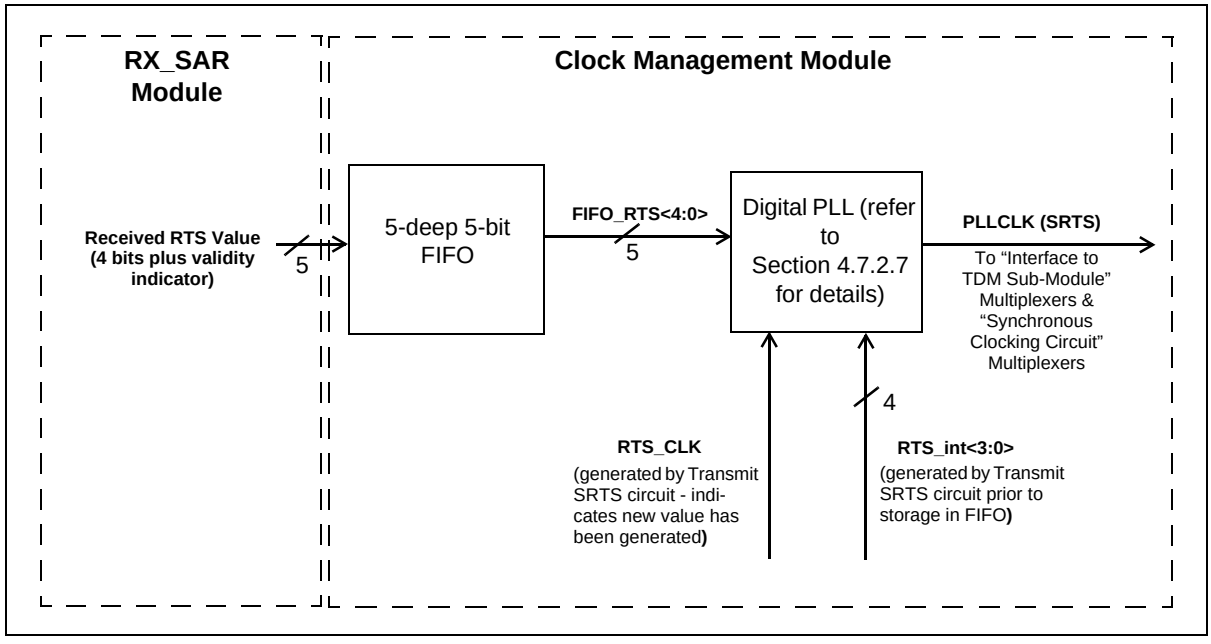


Figure 41 - Receive SRTS Sub-module

In general, the Receive SRTS sub-module simply holds a FIFO of RTS values which were extracted from received cells by either the UDT RX_SAR or the SDT RX_SAR. The RTS value transmitted from the RX_SAR to the Clock Management module is actually 5 bits long, rather than a 4-bit RTS nibble. The extra bit provides error-detection to the internal digital PLL. In the event of a lost cell or unrecoverable error being detected by the RX_SAR, the MSB of the received RTS value is set to 1. The internal digital PLL detects this error and discards the current RTS value from both the RX_SAR and the local Transmit SRTS circuit. More detail about this error protection scheme can be found in Section , “RTS Reception for SRTS Clock Recovery,” on page 88. When the port’s PLL requests a new RTS value, the Receive SRTS sub-module sends the required nibble and validity indicator to the PLL. The actual generation of the output clock based on the RTS nibbles is performed within the digital PLL. Refer to Section 4.7.2.7 on page 104 for a detailed explanation of the digital PLL design.

Note that underrun and overflow detection is provided on the Receive SRTS FIFO. Two register bits are provided to inform the user that underruns or overflows have been detected. If there were not enough RTS values placed into the Receive RTS FIFO by the UDT RX_SAR or the SDT RX_SAR (e.g., because of multiple consecutive sequence number errors, as explained above), the FIFO would eventually underrun. However, the Receive SRTS FIFO underrun protection puts the PLL into holdover mode automatically. Once an entry has been read from the Receive SRTS FIFO by the PLL, the data at that location in the FIFO is overwritten, marking the data as “invalid”. Although during an underrun event, new RTS values are not being placed into the Receive SRTS FIFO, the PLL continues to read RTS values from the FIFO. Eventually, the PLL will read out previously-read data. The reception of these now-invalid RTS values forces the PLL into automatic holdover mode.

4.7.2.6 Adaptive Clock Recovery Circuit

The adaptive clock recovery technique is recommended in ITU-T I.363.1, but not standardized. The general approach is to monitor the fill-level of the received data buffers to determine the clocking rate. If the fill-level is above average, the local clock must be operating at a lower rate than the remote clock. As such, the local clock frequency should be increased so that the buffer is emptied more quickly. On the other hand, if the fill-level measured is below average, the buffer is being emptied too quickly and the local clock rate should be decreased to match the rate of the remote clock.

Within the Clock Management module, the adaptive clock recovery technique is implemented via an internal PLL, as shown in Figure 42. Each port has its own PLL, which is the same as the one outlined for SRTS operation in the

preceding section. There is not any additional circuitry within the Clock Management module since the RX_SAR is responsible for providing the information required by the PLL.

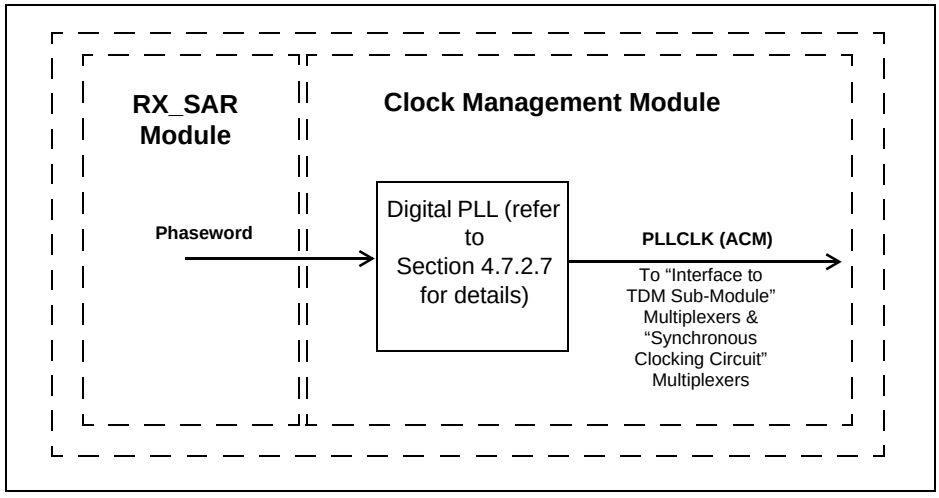


Figure 42 - Adaptive Clock Recovery Sub-module

Explanation of Operation: The UDT RX_SAR or the SDT RX_SAR generates a digital phaseword based on the fill-level of the UDT/SDT Reassembly Circular Buffers of the MT90528. The PLL compares the phaseword with an average value for the buffer fill of the Reassembly Circular Buffer in question. The PLL then adjusts the TDM output clock accordingly. As mentioned previously, the phaseword of the Reassembly Circular Buffer is transmitted to the Clock Management module by the RX_SAR. In the case of a slip, the phaseword is set to a pre-determined value within the RX_SAR module. In such a case, the phaseword indicates to the PLL the type of slip which occurred (i.e., underrun or overflow) so that the PLL can adjust the clock rate appropriately. In the case of a cut VC (i.e., no cells are arriving at the RX_SAR) or upon initialization, the phaseword is set in such a way that the PLL does not adjust the TDM output clock.

More explanation regarding phaseword generation can be found in Section , “Digital Phaseword Generation for Adaptive Clock Recovery,” on page 87.

4.7.2.7 Internal Digital PLL Sub-Module

There is a separate Stratum 4 digital PLL for each of the 28 ports in the MT90528 device. This module takes care of generating several network clocks with the appropriate quality. The same PLL is used for clock recovery from TDM clocks, network clocks, SRTS data, or buffer pointer data in adaptive mode.

In all modes of operation (explained below), the PLL is capable of generating an output clock of 1.544 MHz, 2.048 MHz, or 4.096 MHz. The frequency generated is determined by the PLL_FREQ_SEL bits in the per-port Clocking Configuration Registers.

Architecture

A digital PLL must provide a clock synchronous to some input signal. Since there are several types of incoming signals to synchronize to, the per-port PLLs require dedicated phase detectors for the various types of input. The basic PLL architecture, however, is the same for all situations. It consists of a phase detector, a loop filter, a digital controlled oscillator and a divider (see Figure 43).

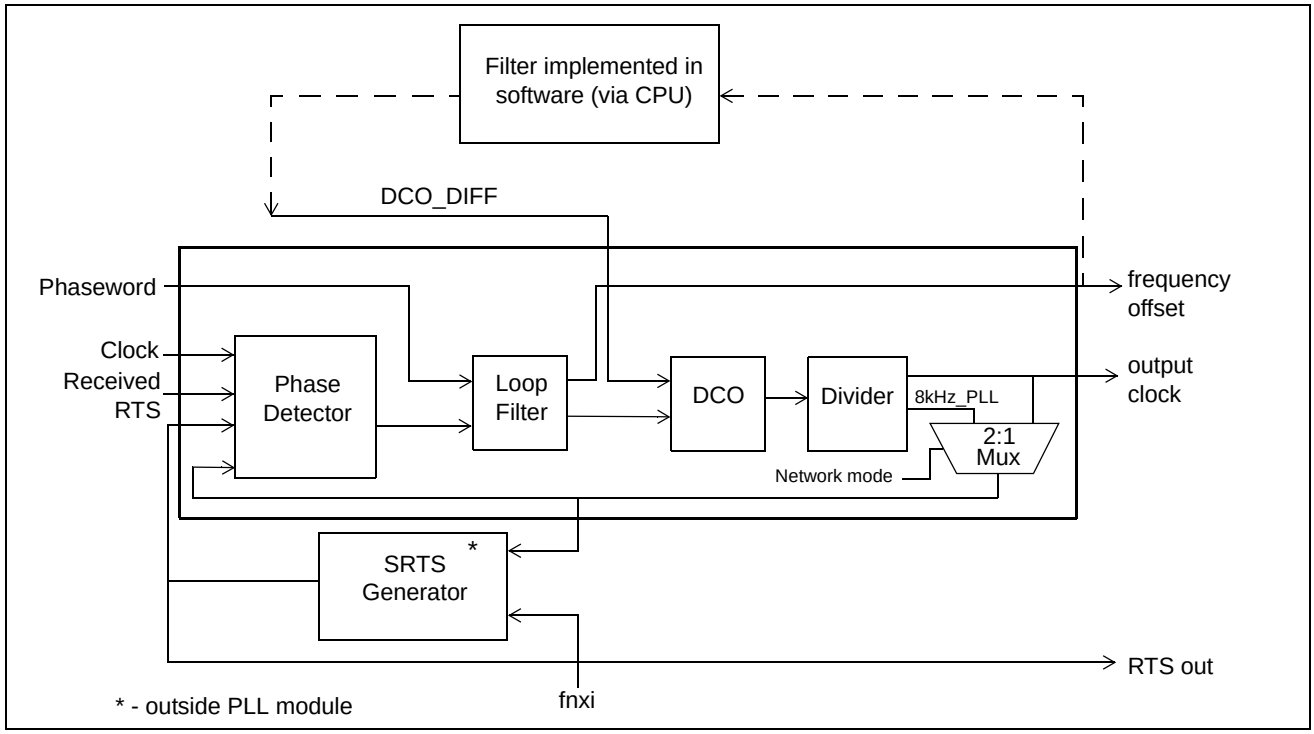


Figure 43 - Block Diagram of the Digital PLL Module

Modes of Operation (PLL_INPUT_SEL bits)

The PLL has four major modes of operation which are configured on a per-port basis via the PLL_INPUT_SEL bits in the Clocking Configuration Registers. The four modes are, briefly, as follows:

- Line-clocking mode: Synchronize to a 1.544 MHz, 2.048 MHz, or 4.096 MHz clock input to the chip on the port's corresponding STiCLK input line. Generate an outgoing clock with the appropriate frequency. The outgoing service clock (1.544 MHz, 2.048 MHz, or 4.096 MHz) is phase-locked to the input clock. This mode of operation may be used to "clean up" a jittery input clock. In line-clocking mode, the maximum locking time is about 15 seconds.
- SRTS mode: Synchronize to the incoming RTS nibbles (time stamps). Generate a 1.544 MHz, 2.048 MHz, or 4.096 MHz clock. The proper service output clock is fed into the per-port SRTS generator (outlined in Section 4.7.2.4, "Transmit SRTS Circuit Sub-module," on page 99) to generate a local RTS value that is compared with subsequent received RTS values. In SRTS mode, the maximum locking time is approximately 100 seconds.
- Network mode: Similar to line-clocking mode, but the input clock is an 8 kHz clock (coming either directly from the PHY_CLK pin or from a divided down version of a 19.44MHz clock input at the PHY_CLK pin). The 8 kHz clock is sourced from the Clock Management module, as explained in Section 4.7.2.3, "Network Clock Divider Circuit," on page 98. The output clock (1.544 MHz, 2.048 MHz, or 4.096 MHz) is synchronous and phase-locked to the 8 kHz input clock. In network mode, the maximum locking time is about 40 seconds.
- Adaptive mode: Synchronize to the incoming cell stream by monitoring the fill level of a VC's Reassembly Circular Buffers. The PLL receives a phaseword from the UDT RX_SAR or SDT RX_SAR. A clock rate of approximately 1.544 MHz, 2.048 MHz, or 4.096 MHz is generated, depending upon the PLL_FREQ_SEL bits.

Note that the UDT RX_SAR and SDT RX_SAR Reassembly Control Structures must be configured appropriately if either Adaptive or SRTS Clock Recovery methods are to be used. For more details, refer to the UDT RX_SAR and SDT RX_SAR module descriptions in Section 4.6.1, "UDT RX_SAR and SDT RX_SAR Modules" earlier in this document.

Sub-modes of Operation (PLL_MODE_SEL bits)

Within each mode described above, the PLL has four sub-modes:

- Normal sub-mode: The input (be it a clock, RTS nibbles, or phasewords) is used to synchronize the PLL output clock to the input.
- Holdover sub-mode: Either when configured as such by the user (via the PLL_MODE_SEL bits) or when a port experiences an LOS condition (while operating in UDT mode), the PLL is switched to holdover sub-mode. When in the holdover state, the PLL ignores the input and holds the output clock at its current deviation from the center frequency.
- Freerun sub-mode: In this sub-mode, a clock rate of 1.544 MHz, 2.048 MHz, or 4.096 MHz is generated. No input is used and the output frequency is fixed to the nominal center frequency.
- CPU sub-mode: In this mode of operation, the offset from the center frequency of the output clocks is determined by the value written to the per-port Clocking DCO Difference Register by an external CPU. The value programmed by the CPU is used to set the PLL output frequency directly, instead of using the PLL's internal filter output. This mode is intended to put an external CPU into the PLL loop. The CPU can read the filter output (from the per-port Clocking Phase Accumulator Register), process it, and write the desired factor to the DCO. This mode of operation might be used if the user wanted to implement a loop filter with a very large time constant.

More detail regarding how to configure the PLL for the various modes of operation can be found in the register descriptions for the Clock Management Module, found in Section 6.2.8 on page 149.

Frequency Behaviour

The PLL must generate frequencies with an accuracy as stated in Table 21. The accuracy defines the freerun accuracy and the locking range of the PLL. The accuracy of the master clock (MCLK), which has to be running at 66 MHz, must be incorporated into these figures. A freerun accuracy of approximately 0.1 ppm and a locking range of approximately 250 ppm has been implemented, thereby allowing 100 ppm MCLK accuracy and a 150 ppm input clock / RTS nibble range.

Clock	Frequency (MHz)	Accuracy (ppm)	1 UI (ns)
C1M5 (DS1)	1.544	-0.13	648
C2M (E1)	2.048	0.05	488
C4M	4.096	0.05	244

Table 21 - Center Frequency and Accuracy

Jitter and Wander

The af-vtoa-0078.000 standard with respect to jitter and wander points to several ANSI and ITU-T standards, as summarized in Table 22. The jitter requirements are met in all clocking modes. The wander requirements may not (nor need they) be met in adaptive mode.

Clock	Jitter	Wander
C1M5 (DS1)	ANSI T1.102 ITU-T G.824	ANSI T1.403 ITU-T G.824
C2M (E1)	ITU-T G.823	ITU-T G.823

Table 22 - Relevant Specifications

The standards from Table 22 specify wander/jitter input tolerance and maximum output jitter. For the input wander/jitter tolerance, the low frequency parts are the largest and are therefore the most important for the PLL requirements (see Table 23). With a corner frequency larger than 1.2 Hz, the PLL will follow wander below 0.1 Hz.

The range of the phase detector is therefore based upon the wander tolerance at 0.1 Hz and will be 32 UI peak-to-peak (+/- 16 UI).

Clock	A0 [UI_{pp}]	A1 [UI_{pp}]	F0 [Hz]	F1 [Hz]	@ 0.1 Hz
C1M5	28	5	1.2E-5	10	6.2
C2M	37	18	1.2E-5	20	23

Table 23 - Minimum Input Wander and Jitter Tolerance

The maximum intrinsic output jitter allowed on the output of the PLL is specified in ITU-T G.823/G.824 and is listed in Table 24. That said, the PLL within the MT90528 has a maximum intrinsic output jitter of one half of an MCLK cycle. However, any jitter on MCLK will be directly transferred to the output clocks.

Clock	A [UI_{pp}]	A [ns]
C1M5	0.1	65
C2M	0.2	98

Table 24 - Maximum Allowed Intrinsic Output Jitter

MTIE (Maximum Time Interval Error)

ANSI T1.403 and T1.101 require that the output phase change at a speed of no more than 81 ns per 1.326 ms, with a maximum phase change of 1 μs. Therefore, the slew rate of the DCO input is no more than 61 ppm of the center frequency setting. The “no more than 81 ns / 1.326 ms” requirement is met in all modes.

Since the period of the 1.544 MHz, 2.048 MHz, and 4.096 MHz signals is less than 1 μs, that requirement is met automatically when the PLL is in synchronous mode. When switching between modes, the 1 μs MTIE is not guaranteed.

Locking Range

When using an 8 kHz, 2.048 MHz, or 4.096 MHz input clock, a locking range of ± 246 ppm is provided. When the input clock is 1.544 MHz, the locking range is ±245 ppm. Note that the locking range is related to the master clock. If the master clock (i.e., MCLK) is 100 ppm too low, the whole locking range also shifts 100 ppm downwards.

4.8 Test Interface

The MT90528 contains an IEEE 1149 standard Test Access Port (TAP), which provides Boundary-Scan test access to aid board-level testing. (IEEE 1149 is often referred to by its older designation: JTAG - Joint Test Action Group.)

4.8.1 Test Access Port

The test port is a standard IEEE 1149 interface, with the optional $\overline{\text{TRST}}$ pin. The Test Access Port consists of 5 pins:

TCK: Boundary-scan Test Clock.

TDI: Test Data In; input pin clocked in on the rising edge of TCK. TDI should be pulled HIGH if boundary-scan is not in use.

TDO: Test Data Out; output pin updated on the falling edge of TCK. The output is in high-impedance except when data is actually being shifted out.

TMS: Test Mode Select; input control line clocked in on the rising edge of TCK. TMS should be pulled HIGH if boundary-scan is not in use.

$\overline{\text{TRST}}$: Test Reset; asynchronous, active-low, input which is used to reset the JTAG interface, and the TAP controller. The $\overline{\text{TRST}}$ pin has an internal pull-down, and should also be pulled LOW externally

whenever boundary-scan is not in use, to ensure normal operation of the MT90528. Figure 44 below shows a typical board-level design, including how $\overline{\text{TRST}}$ can be pulled HIGH by the test connector in cases where the tester does not provide a $\overline{\text{TRST}}$ pin.

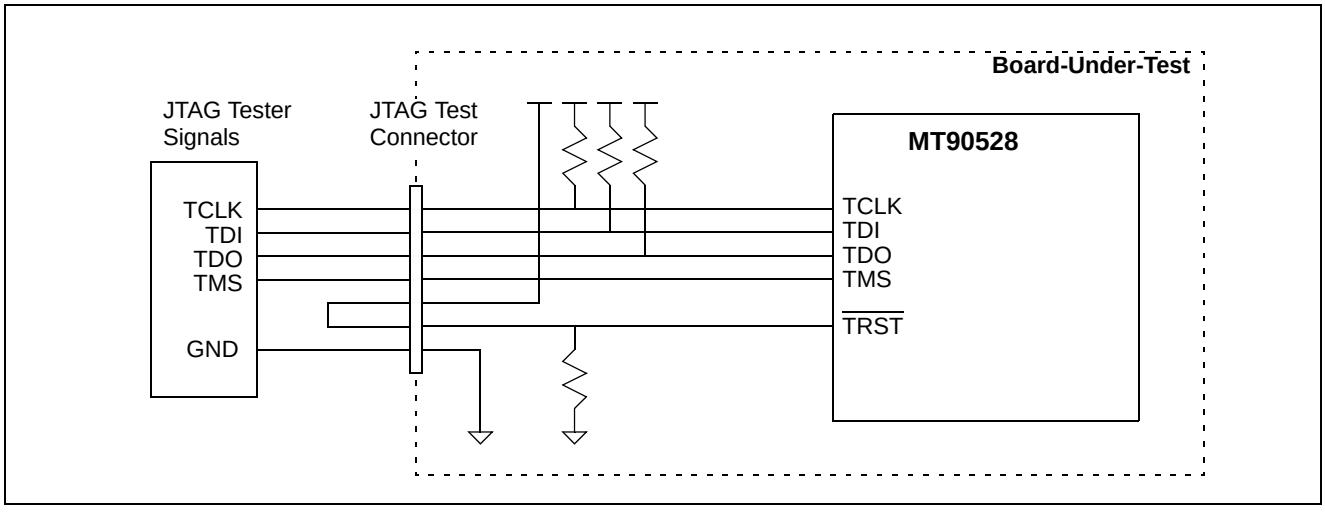


Figure 44 - A Typical JTAG Test Connection

4.8.2 JTAG ID

The JTAG device ID for the MT90528 is 1052814Bh:

Version<31:28>:	0001
Part Number<27:12>:	0000 0101 0010 1000 = 0528h
Manufacturer ID<11:1>:	0001 0100 101
LSB<0>:	1

Note that by mistake, two Zarlink products (MT90520 and MT90528) have been coded with the same Part Number into the JTAG Device ID Register.

4.8.3 Boundary Scan Instructions

The TAP Controller of the MT90528 supports the following instructions: IDCODE, BYPASS, EXTEST, SAMPLE, HIGHZ, CLAMP.

4.8.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Zarlink Semiconductor to aid in the use of the IEEE 1149 test interface.

5.0 Memory

5.1 Internal Memory Map

CPU Byte Address (hex)	Description	Notes
8 xxxx - TX_SAR Control Memory		
80000 - 87FFE	Per-VC UDT and SDT Segmentation Control Structures Segmentation SDT Pointer Tables	Normal CPU access - writes and reads Buffer is 16 Kwords long
9 xxxx - SDT RX_SAR Control Memory		
90000 - 97FFE	Per-VC SDT Reassembly Control Structures	Normal CPU access - writes and reads Buffer is 16 Kwords long
A xxxx - TDM Output Control		
A0000 - A003E	TDM SDT Reassembly CS - port #0	Normal CPU access - writes and reads
A0800 - A083E	TDM SDT Reassembly CS - port #1	Each per-port buffer is 32 words long.
...	...	
AD800- AD83E	TDM SDT Reassembly CS - port #27	
B xxxx - UDT RX_SAR Control Memory		
BE000 - BE01E	UDT RX_SAR CS - port #0	Normal CPU access - writes and reads Each per-port buffer is 16 words long.
BE020 - BE03E	UDT RX_SAR CS - port #1	
...	...	
BE360 - BE37E	UDT RX_SAR CS - port #27	
C xxxx - UTOPIA		
C 0000 - C07FE	UTOPIA RX FIFO	CPU read access for debug 32 cells X 64 bytes/cell = 2048 bytes
C 1000 - C11FE	UTOPIA TX FIFO	CPU read access for debug 8 cells X 64 bytes/cell = 512 bytes

Table 25 - Internal Memory Map

5.2 External Memory

Several buffers and structures are stored in external memory when transmitting and receiving SDT and/or data cells. Since the location of the buffers and structures is not hard-coded in the hardware, the user can program the chip to put these at any location in the external memory. The following list describes the various items located in external memory, if the chip is programmed to support data and SDT cells. Note that the entire external memory space is used (1M word) if the maximum size is chosen for all of these items.

As pointed out previously in this document, note that **no** external memory is required if the device is configured solely for UDT operation, provided that no data cell transmission or reception is required.

- UTOPIA Look-up Table
  - configured based on N, the number of least-significant VCI bits, and M, the number of least-significant VPI bits, (programmed by the user in the UNCB register) used to form the search addresses within the look-up table
  - maximum of **64 K** words

- Data TX_SAR Cell Buffer
  - possible sizes: 16 cells, 32 cells, 64 cells, 128 cells (each cell occupies 64 bytes; 32 words)
  - maximum of **4 K** words
- Data RX_SAR Cell Buffer
  - possible sizes: 16 cells, 32 cells, 64 cells, 128 cells (each cell occupies 64 bytes; 32 words)
  - maximum of **4 K** words
- SDT Segmentation Circular Buffers
  - each channel to be transmitted in ATM cells requires its own Segmentation Circular Buffer. Each buffer occupies 64 words
  - up to 896 channels (28 ports x 32 channels per port) can be transmitted
  - maximum of **56 K** words
- SDT Reassembly Circular Buffers
  - each channel which will be receiving data from ATM cells requires its own Reassembly Circular Buffer. Each buffer has a programmable size, on a per-VC basis.
  - the size selected for a Reassembly Circular Buffer should be based upon the amount of CDV expected on the VC, as well as the number of channels being carried on the VC (more buffering is required on a per-channel basis for VCs with fewer channels, because more data for each channel is received at once upon cell reception). Note that CDV can be accounted for within a larger-than-necessary buffer by programming the Maximum Lead value.

    Circular Buffer Size $\geq$ Maximum Lead + Number of Bytes per Channel per Cell

    Maximum Lead = 2 bytes + ((2*CDV) / (0.125 ms/byte)). CDV is in ms.

    Number of Bytes per Channel per Cell = roundup(N/47). N = # of channels per VC.
  - programmable sizes for Reassembly Circular Buffers are as follows: 64 words, 128 words, 256 words, 512 words, and 1024 words
  - up to 896 channels (28 ports x 32 channels per port) can be received
  - maximum of **896 K** words

Figure 45 shows an example external memory allocation for the structures listed above. The example assumes the maximum memory allocation for each of the structures. The size and location of the structures are programmable and do not necessarily have to be located at the addresses given in the example. The base address in the figure is the base address of external memory.

Figure 46 shows another sample external memory allocation for the structures listed above. The example assumes the minimum memory allocation for each of the structures. The example assumes that no data cell transmission or reception is required, that all channels are transmitted in trunking VCs carrying 128 channels (therefore requiring only 7 VCs), and that minimum-sized Reassembly Circular Buffers are required. The size and location of the structures are programmable and do not necessarily have to be located at the addresses given in the example. The base address in the figure is the base address of external memory.

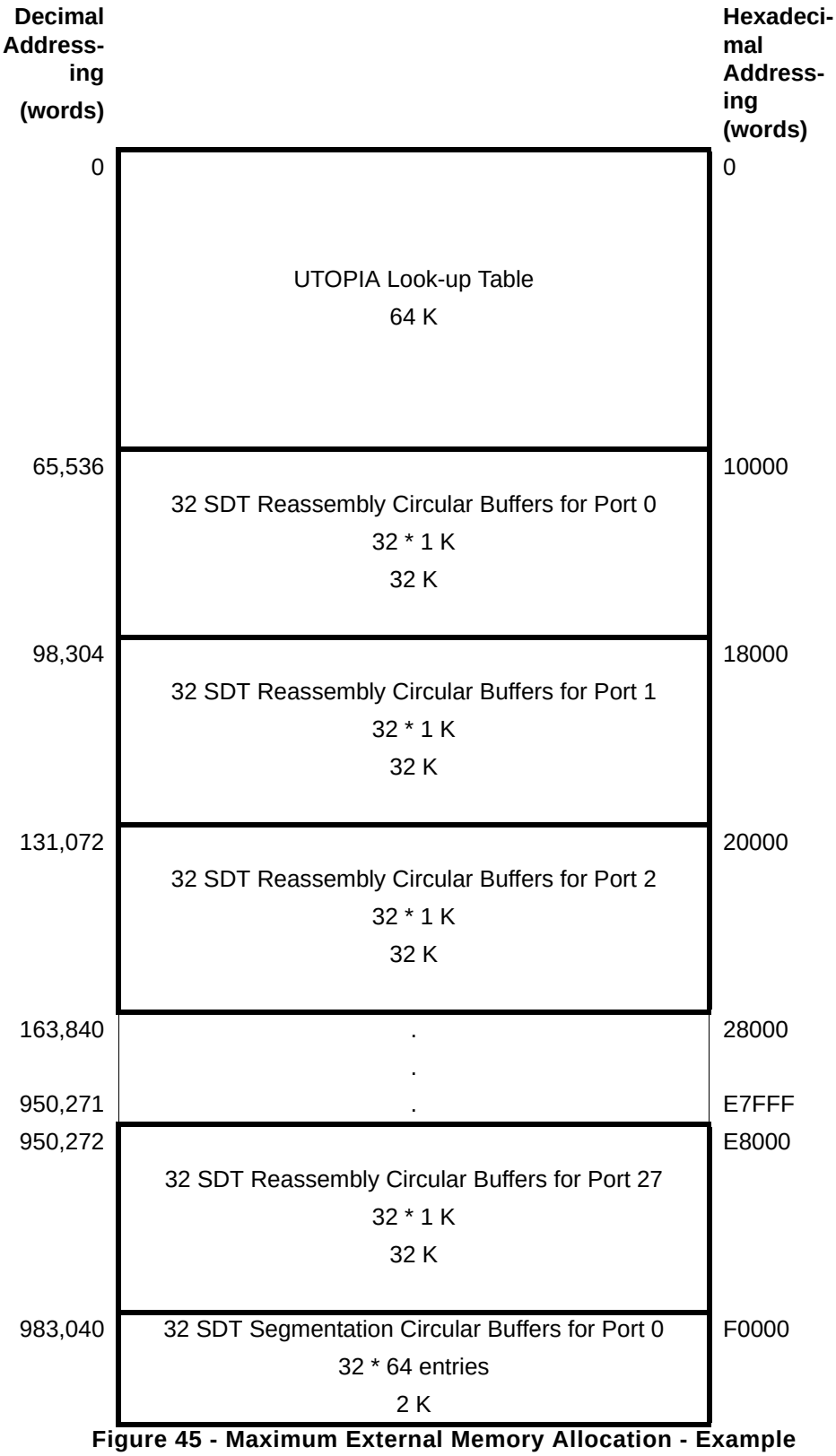


Figure 45 - Maximum External Memory Allocation - Example

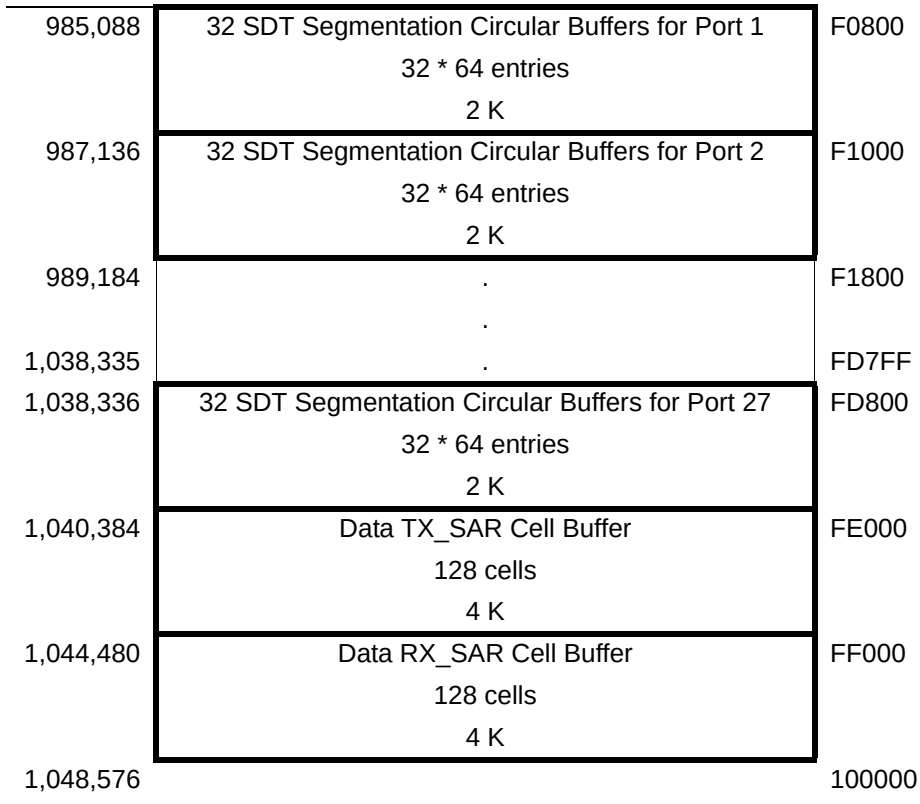


Figure 45 - Maximum External Memory Allocation - Example

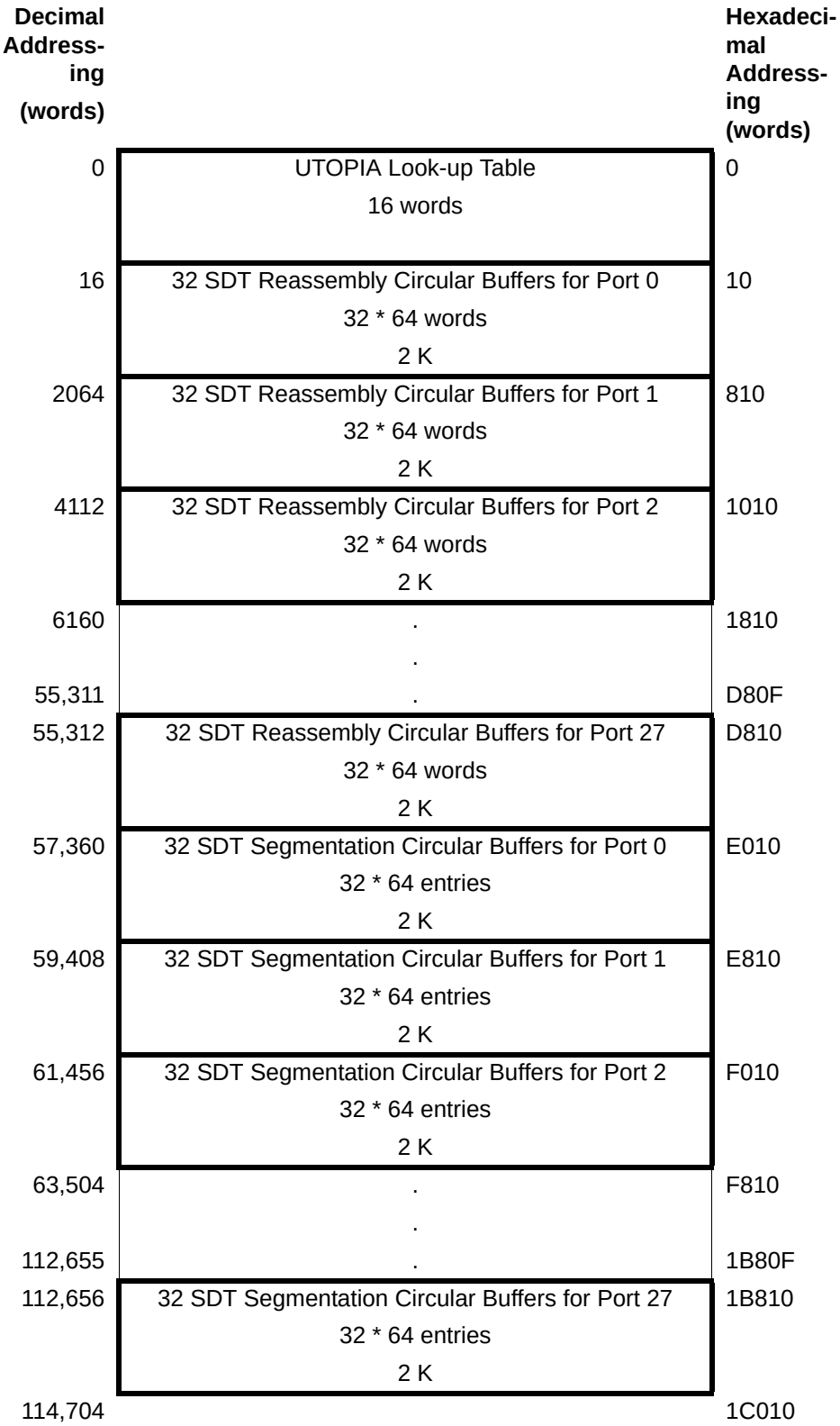


Figure 46 - Minimum External Memory Allocation - Example

6.0 Registers

This section describes the registers contained within the MT90528. The MT90528 is mapped over 1 Mbyte of internal address space. The first 512 Kbytes of address space are allocated for internal register use, while the latter half of address space contains internal memory blocks within the MT90528. As shown in Table 26 on page 115, the device does not implement all of the register space available inside the chip. The unused address space is reserved for future variants of the device.

The internal registers are used by the following modules within the device:

- Microprocessor Interface
- TX_SAR
- RX_SARs (UDT, Data, and SDT)
- Reassembly-Side Timeout
- UTOPIA Interface
- Clock Management
- TDM Interface
- External Memory Interface

All registers are 16 bits long. The device only allows 16-bit (word) microprocessor accesses; byte access is not supported. However, the addresses given in the following tables are given as byte addresses.

All register addresses and reset values are listed in hexadecimal (Hex) format.

The register bit types are:

- **Read / Write (R/W)** - can be read or written via the microprocessor interface.
- **Read Only Latched (R/O/L)** - these bits are set by an activated status source (e.g., counter rollover) within the chip; once set, they remain set even if the status source is deactivated. The microprocessor can read an R/O/L bit and clear it by writing a logic ‘0’ into it (as long as the status source is not active). Writing logic ‘1’ has no effect on this type of register bit.
- **Read Only (R/O)** - can be read via the microprocessor interface. A write to this type of register bit is ignored by the chip. However, these bits should be written with ‘0’ to ensure software compatibility with future versions of the MT90528.

6.1 Register Overview

Byte Address Hex	Reset Value	Label	Description
Microprocessor Interface Module			
0000	0001	CWRR	Chip Wide Reset Register
0002	0000	MSR	Main Status Register
0004	0000	LAWI	Low Address Word Indirection Register
0006	0000	HAIC	High Address Indirection Command Register
0008	0000	IDR	Indirection Data Register
000A	0000	MIER	Main Interrupt Enable Register
000C	0001	MRR	MT90528 Revision Register
TX_SAR Module			
Per-Port TX_SAR Registers			
1000	0000	TXPTB_P0	TX_SAR Pointer Table Base Register Port 0
1002	0000	TXPTB_P1	TX_SAR Pointer Table Base Register Port 1
1004	0000	TXPTB_P2	TX_SAR Pointer Table Base Register Port 2
1006	0000	TXPTB_P3	TX_SAR Pointer Table Base Register Port 3
1008	0000	TXPTB_P4	TX_SAR Pointer Table Base Register Port 4
100A	0000	TXPTB_P5	TX_SAR Pointer Table Base Register Port 5
100C	0000	TXPTB_P6	TX_SAR Pointer Table Base Register Port 6
100E	0000	TXPTB_P7	TX_SAR Pointer Table Base Register Port 7
1010	0000	TXPTB_P8	TX_SAR Pointer Table Base Register Port 8
1012	0000	TXPTB_P9	TX_SAR Pointer Table Base Register Port 9
1014	0000	TXPTB_P10	TX_SAR Pointer Table Base Register Port 10
1016	0000	TXPTB_P11	TX_SAR Pointer Table Base Register Port 11
1018	0000	TXPTB_P12	TX_SAR Pointer Table Base Register Port 12
101A	0000	TXPTB_P13	TX_SAR Pointer Table Base Register Port 13
101C	0000	TXPTB_P14	TX_SAR Pointer Table Base Register Port 14
101E	0000	TXPTB_P15	TX_SAR Pointer Table Base Register Port 15
1020	0000	TXPTB_P16	TX_SAR Pointer Table Base Register Port 16
1022	0000	TXPTB_P17	TX_SAR Pointer Table Base Register Port 17
1024	0000	TXPTB_P18	TX_SAR Pointer Table Base Register Port 18
1026	0000	TXPTB_P19	TX_SAR Pointer Table Base Register Port 19
1028	0000	TXPTB_P20	TX_SAR Pointer Table Base Register Port 20
102A	0000	TXPTB_P21	TX_SAR Pointer Table Base Register Port 21
102C	0000	TXPTB_P22	TX_SAR Pointer Table Base Register Port 22
102E	0000	TXPTB_P23	TX_SAR Pointer Table Base Register Port 23
1030	0000	TXPTB_P24	TX_SAR Pointer Table Base Register Port 24
1032	0000	TXPTB_P25	TX_SAR Pointer Table Base Register Port 25
1034	0000	TXPTB_P26	TX_SAR Pointer Table Base Register Port 26
1036	0000	TXPTB_P27	TX_SAR Pointer Table Base Register Port 27
Main TX_SAR Registers			
1038	0000	DTCON	Data TX_SAR Configuration Register

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
103A	0000	DTWPR	Data TX_SAR Write Pointer Register
103C	0000	DTRPR	Data TX_SAR Read Pointer Register
103E	0000	DTCR	Data TX_SAR Control Register
1040	0001	DCGTOR	Data Cell Generation Time Out Register
1042	0000	DTSR	Data TX_SAR Status Register
1044	0000	TXEN	TX_SAR Master Enable Register
UDT RX_SAR Module			
2000	00FF	URCR	UDT Reassembly Control Register
2002	0000	URSER	UDT Reassembly Service Enable Register
2004	001F	URSR	UDT Reassembly Status Register
2006	0000	URCCR	UDT Reassembly Cell Counter Register
Data RX_SAR Module			
2020	0000	DRCR	Data RX_SAR Control Register
2022	0000	DRSR	Data RX_SAR Status Register
2024	0000	DRCON	Data RX_SAR Configuration Register
2026	0000	DRWPR	Data RX_SAR Write Pointer Register
2028	007F	DRRPR	Data RX_SAR Read Pointer Register
202A	0000	DRCCR	Data RX_SAR Cell Counter Register
SDT RX_SAR Module			
2040	00FF	SRCR	SDT Reassembly Control Register
2042	0000	SRSER	SDT Reassembly Service Enable Register
2044	0000	SRSR	SDT Reassembly Status Register
2046	0000	SRCSR	SDT Reassembly Cell Counter Status Register
2048	0000	SRCCR	SDT Reassembly Cell Counter Register
Reassembly-Side Timeout Module			
Main Timeout Registers			
3000	09C4	MTCR	MIB Timeout Configuration Register
3002	0000	MTSR1	MIB Timeout Status Register 1
3004	0000	MTSR2	MIB Timeout Status Register 2
Per-Port Timeout Registers			
3200	07FF	TCR_P0	Timeout Configuration Register Port 0
3202	07FF	TCR_P1	Timeout Configuration Register Port 1
3204	07FF	TCR_P2	Timeout Configuration Register Port 2
3206	07FF	TCR_P3	Timeout Configuration Register Port 3
3208	07FF	TCR_P4	Timeout Configuration Register Port 4
320A	07FF	TCR_P5	Timeout Configuration Register Port 5
320C	07FF	TCR_P6	Timeout Configuration Register Port 6
320E	07FF	TCR_P7	Timeout Configuration Register Port 7
3210	07FF	TCR_P8	Timeout Configuration Register Port 8
3212	07FF	TCR_P9	Timeout Configuration Register Port 9
3214	07FF	TCR_P10	Timeout Configuration Register Port 10

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
3216	07FF	TCR_P11	Timeout Configuration Register Port 11
3218	07FF	TCR_P12	Timeout Configuration Register Port 12
321A	07FF	TCR_P13	Timeout Configuration Register Port 13
321C	07FF	TCR_P14	Timeout Configuration Register Port 14
321E	07FF	TCR_P15	Timeout Configuration Register Port 15
3220	07FF	TCR_P16	Timeout Configuration Register Port 16
3222	07FF	TCR_P17	Timeout Configuration Register Port 17
3224	07FF	TCR_P18	Timeout Configuration Register Port 18
3226	07FF	TCR_P19	Timeout Configuration Register Port 19
3228	07FF	TCR_P20	Timeout Configuration Register Port 20
322A	07FF	TCR_P21	Timeout Configuration Register Port 21
322C	07FF	TCR_P22	Timeout Configuration Register Port 22
322E	07FF	TCR_P23	Timeout Configuration Register Port 23
3230	07FF	TCR_P24	Timeout Configuration Register Port 24
3232	07FF	TCR_P25	Timeout Configuration Register Port 25
3234	07FF	TCR_P26	Timeout Configuration Register Port 26
3236	07FF	TCR_P27	Timeout Configuration Register Port 27
UTOPIA Interface Module			
Main UTOPIA Registers			
4000	0004	UCR	UTOPIA Configuration Register
4002	0000	UNCB	UTOPIA Number of Concatenated Bits Register
4004	0000	ULBA	LUT Base Address Register
4006	0000	UVCM	VC Match Register
4008	0000	UVCME	VC Match Enable Register
400A	0000	UVPM	VP Match Register
400C	0000	UVPME	VP Match Enable Register
400E	0000	UPM	UTOPIA Parity Mismatches Register
4010	0030	UFS	UTOPIA FIFO Status Register
4012	0000	USR	UTOPIA Status Register
4014	0000	USER	UTOPIA Service Enable Register
4016	0000	UICC	UTOPIA Incoming Cell Counter
Per-Port UTOPIA Registers			
4200	0000	UVC_P0	UDT VCI for Port 0
4202	0000	UVP_P0	UDT VPI for Port 0
4204	0000	UVC_P1	UDT VCI for Port 1
4206	0000	UVP_P1	UDT VPI for Port 1
4208	0000	UVC_P2	UDT VCI for Port 2
420A	0000	UVP_P2	UDT VPI for Port 2
420C	0000	UVC_P3	UDT VCI for Port 3
420E	0000	UVP_P3	UDT VPI for Port 3
4210	0000	UVC_P4	UDT VCI for Port 4

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
4212	0000	UVP_P4	UDT VPI for Port 4
4214	0000	UVC_P5	UDT VCI for Port 5
4216	0000	UVP_P5	UDT VPI for Port 5
4218	0000	UVC_P6	UDT VCI for Port 6
421A	0000	UVP_P6	UDT VPI for Port 6
421C	0000	UVC_P7	UDT VCI for Port 7
421E	0000	UVP_P7	UDT VPI for Port 7
4220	0000	UVC_P8	UDT VCI for Port 8
4222	0000	UVP_P8	UDT VPI for Port 8
4224	0000	UVC_P9	UDT VCI for Port 9
4226	0000	UVP_P9	UDT VPI for Port 9
4228	0000	UVC_P10	UDT VCI for Port 10
422A	0000	UVP_P10	UDT VPI for Port 10
422C	0000	UVC_P11	UDT VCI for Port 11
422E	0000	UVP_P11	UDT VPI for Port 11
4230	0000	UVC_P12	UDT VCI for Port 12
4232	0000	UVP_P12	UDT VPI for Port 12
4234	0000	UVC_P13	UDT VCI for Port 13
4236	0000	UVP_P13	UDT VPI for Port 13
4238	0000	UVC_P14	UDT VCI for Port 14
423A	0000	UVP_P14	UDT VPI for Port 14
423C	0000	UVC_P15	UDT VCI for Port 15
423E	0000	UVP_P15	UDT VPI for Port 15
4240	0000	UVC_P16	UDT VCI for Port 16
4242	0000	UVP_P16	UDT VPI for Port 16
4244	0000	UVC_P17	UDT VCI for Port 17
4246	0000	UVP_P17	UDT VPI for Port 17
4248	0000	UVC_P18	UDT VCI for Port 18
424A	0000	UVP_P18	UDT VPI for Port 18
424C	0000	UVC_P19	UDT VCI for Port 19
424E	0000	UVP_P19	UDT VPI for Port 19
4250	0000	UVC_P20	UDT VCI for Port 20
4252	0000	UVP_P20	UDT VPI for Port 20
4254	0000	UVC_P21	UDT VCI for Port 21
4256	0000	UVP_P21	UDT VPI for Port 21
4258	0000	UVC_P22	UDT VCI for Port 22
425A	0000	UVP_P22	UDT VPI for Port 22
425C	0000	UVC_P23	UDT VCI for Port 23
425E	0000	UVP_P23	UDT VPI for Port 23
4260	0000	UVC_P24	UDT VCI for Port 24
4262	0000	UVP_P24	UDT VPI for Port 24

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
4264	0000	UVC_P25	UDT VCI for Port 25
4266	0000	UVP_P25	UDT VPI for Port 25
4268	0000	UVC_P26	UDT VCI for Port 26
426A	0000	UVP_P26	UDT VPI for Port 26
426C	0000	UVC_P27	UDT VCI for Port 27
426E	0000	UVP_P27	UDT VPI for Port 27
Clock Management Module			
Main Clocking Registers			
5000	0001	CMCR	Clock Management Configuration Register
5002	0000	PLLCS	External PLL Clock Source Register
Per-Port Clocking Registers			
Port 0			
5200	0000	CCR_P0	Clocking Configuration Register
5202	8000	CPAR_P0	Clocking Phase Accumulator Register
5204	0000	CDDR_P0	Clocking DCO Difference Register
5206	0000	CSFSR_P0	SRTS FIFO Status Register
5208	0001	PLLEN_P0	PLL Enable Register
Port 1			
5210	0000	CCR_P1	Clocking Configuration Register
5212	8000	CPAR_P1	Clocking Phase Accumulator Register
5214	0000	CDDR_P1	Clocking DCO Difference Register
5216	0000	CSFSR_P1	SRTS FIFO Status Register
5218	0001	PLLEN_P1	PLL Enable Register
Port 2			
5220	0000	CCR_P2	Clocking Configuration Register
5222	8000	CPAR_P2	Clocking Phase Accumulator Register
5224	0000	CDDR_P2	Clocking DCO Difference Register
5226	0000	CSFSR_P2	SRTS FIFO Status Register
5228	0001	PLLEN_P2	PLL Enable Register
Port 3			
5230	0000	CCR_P3	Clocking Configuration Register
5232	8000	CPAR_P3	Clocking Phase Accumulator Register
5234	0000	CDDR_P3	Clocking DCO Difference Register
5236	0000	CSFSR_P3	SRTS FIFO Status Register
5238	0001	PLLEN_P3	PLL Enable Register
Port 4			
5240	0000	CCR_P4	Clocking Configuration Register
5242	8000	CPAR_P4	Clocking Phase Accumulator Register
5244	0000	CDDR_P4	Clocking DCO Difference Register
5246	0000	CSFSR_P4	SRTS FIFO Status Register
5248	0001	PLLEN_P4	PLL Enable Register

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
Port 5			
5250	0000	CCR_P5	Clocking Configuration Register
5252	8000	CPAR_P5	Clocking Phase Accumulator Register
5254	0000	CDDR_P5	Clocking DCO Difference Register
5256	0000	CSFSR_P5	SRTS FIFO Status Register
5258	0001	PLLEN_P5	PLL Enable Register
Port 6			
5260	0000	CCR_P6	Clocking Configuration Register
5262	8000	CPAR_P6	Clocking Phase Accumulator Register
5264	0000	CDDR_P6	Clocking DCO Difference Register
5266	0000	CSFSR_P6	SRTS FIFO Status Register
5268	0001	PLLEN_P6	PLL Enable Register
Port 7			
5270	0000	CCR_P7	Clocking Configuration Register
5272	8000	CPAR_P7	Clocking Phase Accumulator Register
5274	0000	CDDR_P7	Clocking DCO Difference Register
5276	0000	CSFSR_P7	SRTS FIFO Status Register
5278	0001	PLLEN_P7	PLL Enable Register
Port 8			
5280	0000	CCR_P8	Clocking Configuration Register
5282	8000	CPAR_P8	Clocking Phase Accumulator Register
5284	0000	CDDR_P8	Clocking DCO Difference Register
5286	0000	CSFSR_P8	SRTS FIFO Status Register
5288	0001	PLLEN_P8	PLL Enable Register
Port 9			
5290	0000	CCR_P9	Clocking Configuration Register
5292	8000	CPAR_P9	Clocking Phase Accumulator Register
5294	0000	CDDR_P9	Clocking DCO Difference Register
5296	0000	CSFSR_P9	SRTS FIFO Status Register
5298	0001	PLLEN_P9	PLL Enable Register
Port 10			
52A0	0000	CCR_P10	Clocking Configuration Register
52A2	8000	CPAR_P10	Clocking Phase Accumulator Register
52A4	0000	CDDR_P10	Clocking DCO Difference Register
52A6	0000	CSFSR_P10	SRTS FIFO Status Register
52A8	0001	PLLEN_P10	PLL Enable Register
Port 11			
52B0	0000	CCR_P11	Clocking Configuration Register
52B2	8000	CPAR_P11	Clocking Phase Accumulator Register
52B4	0000	CDDR_P11	Clocking DCO Difference Register
52B6	0000	CSFSR_P11	SRTS FIFO Status Register

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
52B8	0001	PLLEN_P11	PLL Enable Register
Port 12			
52C0	0000	CCR_P12	Clocking Configuration Register
52C2	8000	CPAR_P12	Clocking Phase Accumulator Register
52C4	0000	CDDR_P12	Clocking DCO Difference Register
52C6	0000	CSFSR_P12	SRTS FIFO Status Register
52C8	0001	PLLEN_P12	PLL Enable Register
Port 13			
52D0	0000	CCR_P13	Clocking Configuration Register
52D2	8000	CPAR_P13	Clocking Phase Accumulator Register
52D4	0000	CDDR_P13	Clocking DCO Difference Register
52D6	0000	CSFSR_P13	SRTS FIFO Status Register
52D8	0001	PLLEN_P13	PLL Enable Register
Port 14			
52E0	0000	CCR_P14	Clocking Configuration Register
52E2	8000	CPAR_P14	Clocking Phase Accumulator Register
52E4	0000	CDDR_P14	Clocking DCO Difference Register
52E6	0000	CSFSR_P14	SRTS FIFO Status Register
52E8	0001	PLLEN_P14	PLL Enable Register
Port 15			
52F0	0000	CCR_P15	Clocking Configuration Register
52F2	8000	CPAR_P15	Clocking Phase Accumulator Register
52F4	0000	CDDR_P15	Clocking DCO Difference Register
52F6	0000	CSFSR_P15	SRTS FIFO Status Register
52F8	0001	PLLEN_P15	PLL Enable Register
Port 16			
5300	0000	CCR_P16	Clocking Configuration Register
5302	8000	CPAR_P16	Clocking Phase Accumulator Register
5304	0000	CDDR_P16	Clocking DCO Difference Register
5306	0000	CSFSR_P16	SRTS FIFO Status Register
5308	0001	PLLEN_P16	PLL Enable Register
Port 17			
5310	0000	CCR_P17	Clocking Configuration Register
5312	8000	CPAR_P17	Clocking Phase Accumulator Register
5314	0000	CDDR_P17	Clocking DCO Difference Register
5316	0000	CSFSR_P17	SRTS FIFO Status Register
5318	0001	PLLEN_P17	PLL Enable Register
Port 18			
5320	0000	CCR_P18	Clocking Configuration Register
5322	8000	CPAR_P18	Clocking Phase Accumulator Register
5324	0000	CDDR_P18	Clocking DCO Difference Register

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
5326	0000	CSFSR_P18	SRTS FIFO Status Register
5328	0001	PLLEN_P18	PLL Enable Register
Port 19			
5330	0000	CCR_P19	Clocking Configuration Register
5332	8000	CPAR_P19	Clocking Phase Accumulator Register
5334	0000	CDDR_P19	Clocking DCO Difference Register
5336	0000	CSFSR_P19	SRTS FIFO Status Register
5338	0001	PLLEN_P19	PLL Enable Register
Port 20			
5340	0000	CCR_P20	Clocking Configuration Register
5342	8000	CPAR_P20	Clocking Phase Accumulator Register
5344	0000	CDDR_P20	Clocking DCO Difference Register
5346	0000	CSFSR_P20	SRTS FIFO Status Register
5348	0001	PLLEN_P20	PLL Enable Register
Port 21			
5350	0000	CCR_P21	Clocking Configuration Register
5352	8000	CPAR_P21	Clocking Phase Accumulator Register
5354	0000	CDDR_P21	Clocking DCO Difference Register
5356	0000	CSFSR_P21	SRTS FIFO Status Register
5358	0001	PLLEN_P21	PLL Enable Register
Port 22			
5360	0000	CCR_P22	Clocking Configuration Register
5362	8000	CPAR_P22	Clocking Phase Accumulator Register
5364	0000	CDDR_P22	Clocking DCO Difference Register
5366	0000	CSFSR_P22	SRTS FIFO Status Register
5368	0001	PLLEN_P22	PLL Enable Register
Port 23			
5370	0000	CCR_P23	Clocking Configuration Register
5372	8000	CPAR_P23	Clocking Phase Accumulator Register
5374	0000	CDDR_P23	Clocking DCO Difference Register
5376	0000	CSFSR_P23	SRTS FIFO Status Register
5378	0001	PLLEN_P23	PLL Enable Register
Port 24			
5380	0000	CCR_P24	Clocking Configuration Register
5382	8000	CPAR_P24	Clocking Phase Accumulator Register
5384	0000	CDDR_P24	Clocking DCO Difference Register
5386	0000	CSFSR_P24	SRTS FIFO Status Register
5388	0001	PLLEN_P24	PLL Enable Register
Port 25			
5390	0000	CCR_P25	Clocking Configuration Register
5392	8000	CPAR_P25	Clocking Phase Accumulator Register

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
5394	0000	CDDR_P25	Clocking DCO Difference Register
5396	0000	CSFSR_P25	SRTS FIFO Status Register
5398	0001	PLLEN_P25	PLL Enable Register
Port 26			
53A0	0000	CCR_P26	Clocking Configuration Register
53A2	8000	CPAR_P26	Clocking Phase Accumulator Register
53A4	0000	CDDR_P26	Clocking DCO Difference Register
53A6	0000	CSFSR_P26	SRTS FIFO Status Register
53A8	0001	PLLEN_P26	PLL Enable Register
Port 27			
53B0	0000	CCR_P27	Clocking Configuration Register
53B2	8000	CPAR_P27	Clocking Phase Accumulator Register
53B4	0000	CDDR_P27	Clocking DCO Difference Register
53B6	0000	CSFSR_P27	SRTS FIFO Status Register
53B8	0001	PLLEN_P27	PLL Enable Register
TDM Interface Module			
Main TDM Registers			
6000	FFFF	MAINTDM1	Main TDM Control Register 1
6002	F000	MAINTDM2	Main TDM Control Register 2
Per-Port TDM Registers			
Port 0			
6200	0000	TDM1_P0	TDM Control Register 1
6202	0000	TDM2_P0	TDM Control Register 2
6204	0000	TDM3_P0	TDM Control Register 3
6206	0000	TDM4_P0	TDM Control Register 4
6208	0000	TDM5_P0	TDM Control Register 5
620A	0000	TDM6_P0	TDM Control Register 6
Port 1			
6210	0000	TDM1_P1	TDM Control Register 1
6212	0000	TDM2_P1	TDM Control Register 2
6214	0000	TDM3_P1	TDM Control Register 3
6216	0000	TDM4_P1	TDM Control Register 4
6218	0000	TDM5_P1	TDM Control Register 5
621A	0000	TDM6_P1	TDM Control Register 6
Port 2			
6220	0000	TDM1_P2	TDM Control Register 1
6222	0000	TDM2_P2	TDM Control Register 2
6224	0000	TDM3_P2	TDM Control Register 3
6226	0000	TDM4_P2	TDM Control Register 4
6228	0000	TDM5_P2	TDM Control Register 5
622A	0000	TDM6_P2	TDM Control Register 6

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
Port 3			
6230	0000	TDM1_P3	TDM Control Register 1
6232	0000	TDM2_P3	TDM Control Register 2
6234	0000	TDM3_P3	TDM Control Register 3
6236	0000	TDM4_P3	TDM Control Register 4
6238	0000	TDM5_P3	TDM Control Register 5
623A	0000	TDM6_P3	TDM Control Register 6
Port 4			
6240	0000	TDM1_P4	TDM Control Register 1
6242	0000	TDM2_P4	TDM Control Register 2
6244	0000	TDM3_P4	TDM Control Register 3
6246	0000	TDM4_P4	TDM Control Register 4
6248	0000	TDM5_P4	TDM Control Register 5
624A	0000	TDM6_P4	TDM Control Register 6
Port 5			
6250	0000	TDM1_P5	TDM Control Register 1
6252	0000	TDM2_P5	TDM Control Register 2
6254	0000	TDM3_P5	TDM Control Register 3
6256	0000	TDM4_P5	TDM Control Register 4
6258	0000	TDM5_P5	TDM Control Register 5
625A	0000	TDM6_P5	TDM Control Register 6
Port 6			
6260	0000	TDM1_P6	TDM Control Register 1
6262	0000	TDM2_P6	TDM Control Register 2
6264	0000	TDM3_P6	TDM Control Register 3
6266	0000	TDM4_P6	TDM Control Register 4
6268	0000	TDM5_P6	TDM Control Register 5
626A	0000	TDM6_P6	TDM Control Register 6
Port 7			
6270	0000	TDM1_P7	TDM Control Register 1
6272	0000	TDM2_P7	TDM Control Register 2
6274	0000	TDM3_P7	TDM Control Register 3
6276	0000	TDM4_P7	TDM Control Register 4
6278	0000	TDM5_P7	TDM Control Register 5
627A	0000	TDM6_P7	TDM Control Register 6
Port 8			
6280	0000	TDM1_P8	TDM Control Register 1
6282	0000	TDM2_P8	TDM Control Register 2
6284	0000	TDM3_P8	TDM Control Register 3
6286	0000	TDM4_P8	TDM Control Register 4
6288	0000	TDM5_P8	TDM Control Register 5

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
628A	0000	TDM6_P8	TDM Control Register 6
Port 9			
6290	0000	TDM1_P9	TDM Control Register 1
6292	0000	TDM2_P9	TDM Control Register 2
6294	0000	TDM3_P9	TDM Control Register 3
6296	0000	TDM4_P9	TDM Control Register 4
6298	0000	TDM5_P9	TDM Control Register 5
629A	0000	TDM6_P9	TDM Control Register 6
Port 10			
62A0	0000	TDM1_P10	TDM Control Register 1
62A2	0000	TDM2_P10	TDM Control Register 2
62A4	0000	TDM3_P10	TDM Control Register 3
62A6	0000	TDM4_P10	TDM Control Register 4
62A8	0000	TDM5_P10	TDM Control Register 5
62AA	0000	TDM6_P10	TDM Control Register 6
Port 11			
62B0	0000	TDM1_P11	TDM Control Register 1
62B2	0000	TDM2_P11	TDM Control Register 2
62B4	0000	TDM3_P11	TDM Control Register 3
62B6	0000	TDM4_P11	TDM Control Register 4
62B8	0000	TDM5_P11	TDM Control Register 5
62BA	0000	TDM6_P11	TDM Control Register 6
Port 12			
62C0	0000	TDM1_P12	TDM Control Register 1
62C2	0000	TDM2_P12	TDM Control Register 2
62C4	0000	TDM3_P12	TDM Control Register 3
62C6	0000	TDM4_P12	TDM Control Register 4
62C8	0000	TDM5_P12	TDM Control Register 5
62CA	0000	TDM6_P12	TDM Control Register 6
Port 13			
62D0	0000	TDM1_P13	TDM Control Register 1
62D2	0000	TDM2_P13	TDM Control Register 2
62D4	0000	TDM3_P13	TDM Control Register 3
62D6	0000	TDM4_P13	TDM Control Register 4
62D8	0000	TDM5_P13	TDM Control Register 5
62DA	0000	TDM6_P13	TDM Control Register 6
Port 14			
62E0	0000	TDM1_P14	TDM Control Register 1
62E2	0000	TDM2_P14	TDM Control Register 2
62E4	0000	TDM3_P14	TDM Control Register 3
62E6	0000	TDM4_P14	TDM Control Register 4

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
62E8	0000	TDM5_P14	TDM Control Register 5
62EA	0000	TDM6_P14	TDM Control Register 6
Port 15			
62F0	0000	TDM1_P15	TDM Control Register 1
62F2	0000	TDM2_P15	TDM Control Register 2
62F4	0000	TDM3_P15	TDM Control Register 3
62F6	0000	TDM4_P15	TDM Control Register 4
62F8	0000	TDM5_P15	TDM Control Register 5
62FA	0000	TDM6_P15	TDM Control Register 6
Port 16			
6300	0000	TDM1_P16	TDM Control Register 1
6302	0000	TDM2_P16	TDM Control Register 2
6304	0000	TDM3_P16	TDM Control Register 3
6306	0000	TDM4_P16	TDM Control Register 4
6308	0000	TDM5_P16	TDM Control Register 5
630A	0000	TDM6_P16	TDM Control Register 6
Port 17			
6310	0000	TDM1_P17	TDM Control Register 1
6312	0000	TDM2_P17	TDM Control Register 2
6314	0000	TDM3_P17	TDM Control Register 3
6316	0000	TDM4_P17	TDM Control Register 4
6318	0000	TDM5_P17	TDM Control Register 5
631A	0000	TDM6_P17	TDM Control Register 6
Port 18			
6320	0000	TDM1_P18	TDM Control Register 1
6322	0000	TDM2_P18	TDM Control Register 2
6324	0000	TDM3_P18	TDM Control Register 3
6326	0000	TDM4_P18	TDM Control Register 4
6328	0000	TDM5_P18	TDM Control Register 5
632A	0000	TDM6_P18	TDM Control Register 6
Port 19			
6330	0000	TDM1_P19	TDM Control Register 1
6332	0000	TDM2_P19	TDM Control Register 2
6334	0000	TDM3_P19	TDM Control Register 3
6336	0000	TDM4_P19	TDM Control Register 4
6338	0000	TDM5_P19	TDM Control Register 5
633A	0000	TDM6_P19	TDM Control Register 6
Port 20			
6340	0000	TDM1_P20	TDM Control Register 1
6342	0000	TDM2_P20	TDM Control Register 2
6344	0000	TDM3_P20	TDM Control Register 3

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
6346	0000	TDM4_P20	TDM Control Register 4
6348	0000	TDM5_P20	TDM Control Register 5
634A	0000	TDM6_P20	TDM Control Register 6
Port 21			
6350	0000	TDM1_P21	TDM Control Register 1
6352	0000	TDM2_P21	TDM Control Register 2
6354	0000	TDM3_P21	TDM Control Register 3
6356	0000	TDM4_P21	TDM Control Register 4
6358	0000	TDM5_P21	TDM Control Register 5
635A	0000	TDM6_P21	TDM Control Register 6
Port 22			
6360	0000	TDM1_P22	TDM Control Register 1
6362	0000	TDM2_P22	TDM Control Register 2
6364	0000	TDM3_P22	TDM Control Register 3
6366	0000	TDM4_P22	TDM Control Register 4
6368	0000	TDM5_P22	TDM Control Register 5
636A	0000	TDM6_P22	TDM Control Register 6
Port 23			
6370	0000	TDM1_P23	TDM Control Register 1
6372	0000	TDM2_P23	TDM Control Register 2
6374	0000	TDM3_P23	TDM Control Register 3
6376	0000	TDM4_P23	TDM Control Register 4
6378	0000	TDM5_P23	TDM Control Register 5
637A	0000	TDM6_P23	TDM Control Register 6
Port 24			
6380	0000	TDM1_P24	TDM Control Register 1
6382	0000	TDM2_P24	TDM Control Register 2
6384	0000	TDM3_P24	TDM Control Register 3
6386	0000	TDM4_P24	TDM Control Register 4
6388	0000	TDM5_P24	TDM Control Register 5
638A	0000	TDM6_P24	TDM Control Register 6
Port 25			
6390	0000	TDM1_P25	TDM Control Register 1
6392	0000	TDM2_P25	TDM Control Register 2
6394	0000	TDM3_P25	TDM Control Register 3
6396	0000	TDM4_P25	TDM Control Register 4
6398	0000	TDM5_P25	TDM Control Register 5
639A	0000	TDM6_P25	TDM Control Register 6
Port 26			
63A0	0000	TDM1_P26	TDM Control Register 1
63A2	0000	TDM2_P26	TDM Control Register 2

Table 26 - Register Summary

Byte Address Hex	Reset Value	Label	Description
63A4	0000	TDM3_P26	TDM Control Register 3
63A6	0000	TDM4_P26	TDM Control Register 4
63A8	0000	TDM5_P26	TDM Control Register 5
63AA	0000	TDM6_P26	TDM Control Register 6
Port 27			
63B0	0000	TDM1_P27	TDM Control Register 1
63B2	0000	TDM2_P27	TDM Control Register 2
63B4	0000	TDM3_P27	TDM Control Register 3
63B6	0000	TDM4_P27	TDM Control Register 4
63B8	0000	TDM5_P27	TDM Control Register 5
63BA	0000	TDM6_P27	TDM Control Register 6
External Memory Interface Module			
7000	0000	MACR	Memory Arbiter Configuration Register
7004	0000	PERS	Parity Error Status Register

Table 26 - Register Summary

6.2 Register Description

Note: Unused bits (labeled as “Reserved”) are reserved for future use and although most of them are read-only (R/O) bits, they should be written with ‘0’ to ensure software compatibility with future versions of the MT90528.

6.2.1 Microprocessor Interface Module

Address: 0000 (Hex)
Label: CWRR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
RESET	0	R/W	When set to 1, the chip is put into reset mode.
Reserved	15:1	R/O	Always reads “0000_0000_0000_000”.

Table 27 - Chip Wide Reset Register

Address: 0002 (Hex)
Label: MSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TX_SAR_SRV	0	R/O	TX_SAR Service Request.
SDT_RXSAR_SRV	1	R/O	SDT RX_SAR Service Request.
UDT_RXSAR_SRV	2	R/O	UDT RX_SAR Service Request.
TDM_SRV	3	R/O	TDM Service Request.
UTOPIA_SRV	4	R/O	UTOPIA Service Request.
XMEMA_SRV	5	R/O	External Memory Arbiter Service Request.
DATA_RXSAR_ SRV	6	R/O	Data RX_SAR Service Request.
RX_TIMEOUT_SRV	7	R/O	Reassembly-Side Timeout Service Request.
CPU_SRV	8	R/O	CPU Service Request
Reserved	15:9	R/O	Always reads “0000_000”.

Note: An interrupt will be generated on the $\overline{IRQ}$ pin if any of the above Service Request bits is asserted and the corresponding Interrupt Enable bit is set in the Main Interrupt Enable Register at 000Ah.

Table 28 - Main Status Register

Address: 0004 (Hex)
Label: LAWI
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	0	R/O	Always reads ‘0’.
LAW	15:1	R/W	Low Address Word. These bits represent bits<15:1> of the indirection address (in **bytes**). **This register must be written before the HAIC register at 0006h.**

Table 29 - Low Address Word Indirection Register

Address: 0006 (Hex)
Label: HAIC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
HAB	4:0	R/W	High Address Bits. These bits represent bits<20:16> of the indirection address (in **bytes**).
AEM	5	R/W	Access External Memory. When this bit is set, the indirection access will be to/from external memory. When this bit is cleared, the indirection access will be to/from internal memory.
RD_N_WR	6	R/W	Read/Write. '0' = CPU write. '1' = CPU read.
ACC	7	R/W	Access Cycle Complete. When this bit is set by the CPU, the indirection cycle is initiated. When low, indicates that the last indirection cycle has been completed. While an indirection access is in progress, the Microprocessor Interface Module registers can be accessed. However, the CPU must wait for the ACC bit to be cleared before initiating the next access to another register block, internal memory, or external memory of the MT90528. **Software cannot clear this bit (it can only be cleared by hardware).**
ACC_DONE_SE	8	R/W	Access Cycle Complete Service Enable. When this bit is set and the ACC bit is low, the CPU_SRV status bit is set in the Main Status Register at 0002h.
Reserved	15:9	R/O	Always read "0000_000".

Table 30 - High Address Indirection Command Register

Address: 0008 (Hex)
Label: IDR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
IDV	15:0	R/W	Indirection Data Value. During an indirection write cycle, the value written to this register is placed in the memory location selected in the LAWI and HAIC registers. During an indirection read cycle, the contents of the memory location selected in LAWI and HAIC are transferred to this register. In the case of a write cycle, **this register must be written before the LAWI and HAIC registers**. The CPU must wait for the ACC bit in the HAIC Register to be cleared before initiating the next write cycle. In the case of a read access to memory, the CPU must write the target address to the LAWI and HAIC registers and wait for ACC = 0 before reading this register.

Table 31 - Indirection Data Register

Address: 000A (Hex)
Label: MIER
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TX_SAR_IE	0	R/W	TX_SAR Interrupt Enable.
SDT_RXSAR_IE	1	R/W	SDT RX_SAR Interrupt Enable.
UDT_RXSAR_IE	2	R/W	UDT RX_SAR Interrupt Enable.
TDM_IE	3	R/W	TDM Interrupt Enable.
UTOPIA_IE	4	R/W	UTOPIA Interrupt Enable.
XMEMA_IE	5	R/W	External Memory Arbiter Interrupt Enable.
DATA_RXSAR_IE	6	R/W	Data RX_SAR Interrupt Enable.
RX_TIMEOUT_IE	7	R/W	Reassembly-Side Timeout Interrupt Enable.
CPU_IE	8	R/W	CPU Interrupt Enable.
Reserved	15:9	R/O	Always reads “0000_000”.

Note: An interrupt will be generated on the IRQ pin if any of the above Interrupt Enable bits is set and there is a corresponding module-level Service Request asserted in the Main Status Register at 0002h.

Table 32 - Main Interrupt Enable Register

Address: 000C (Hex)
Label: MRR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
REV	15:0	R/O	MT90528 hardware revision.

Table 33 - MT90528 Revision Register

6.2.2 TX_SAR Module

Address: 1000 + p*2 (Hex)
Label: TXPTB_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXPTB	13:0	R/W	In SDT mode, these bits hold the base **word** address of the port p SDT Segmentation Pointer Table (see Figure 23 on page 63). In UDT mode, these bits form a pointer to the base **word** address of the UDT Segmentation Control Structure associated with port p. The SDT Segmentation Pointer Tables **must** start on 32-word (64-byte) boundaries.
TXCFG	15:14	R/W	Port p Configuration: “00” = Port p is disabled “01” = UDT mode “10” = Reserved “11” = SDT mode.

Table 34 - TX_SAR Pointer Table Base Register (one per port)

Address: 1038 (Hex) Label: DTCON Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
DTSIZE	1:0	R/W	Data TX_SAR Cell Buffer Size. This field indicates the number of non-CBR data cells which can be held in the Data TX_SAR's Cell Buffer: "00" = 16 cells "01" = 32 cells "10" = 64 cells "11" = 128 cells.
DTBASE	9:2	R/W	Data TX_SAR Cell Buffer Base Address. These bits represent address bits<19:12> of the base address (in **words**) of the cell buffer in external memory.
Reserved	15:10	R/O	Always reads "0000_00".

Table 35 - Data TX_SAR Configuration Register

Address: 103A (Hex) Label: DTWPR Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
DTWP	7:0	R/W	Data TX_SAR Write Pointer. Indicates the cell structure number to which the CPU is currently writing (the cell is not yet valid).
Reserved	15:8	R/O	Always reads "0000_0000".

Table 36 - Data TX_SAR Write Pointer Register

Address: 103C (Hex) Label: DTRPR Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
DTRP	6:0	R/O	Data TX_SAR Read Pointer. Indicates the cell structure number from which the Data TX_SAR is currently reading. This pointer is cleared when the TDSENB bit in the Data TX_SAR Control Register at 103Eh is cleared.
Reserved	15:7	R/O	Always reads "0000_0000_0".

Table 37 - Data TX_SAR Read Pointer Register

Address: 103E (Hex)
Label: DTCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDSENB	0	R/W	Data TX_SAR Enable. When cleared, the Data TX_SAR Read Pointer (register at 103Ch) is reset to “000_0000” and no data cells are transmitted. When set, the Data TX_SAR sends the cells stored in the Data TX_SAR Cell Buffer.
AUTO	1	R/W	When set, the Data TX_SAR transmits cells when the CBR TX_SAR is not busy. When cleared, data cell transmission is controlled by the DCGTOR register at 1040h.
TCBE_SE	2	R/W	Transmit Cell Buffer Empty Service Request Enable. When set, a service request to the CPU is asserted when the cell buffer is empty, as indicated by the assertion of the TCBE bit in the Data TX_SAR Status Register at 1042h. When cleared, this service request is masked.
Reserved	15:3	R/O	Always reads “0000_0000_0000_0”.

Table 38 - Data TX_SAR Control Register

Address: 1040 (Hex)
Label: DCGTOR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
DCGP	9:0	R/W	These bits control the time between data cell transmissions when the Data TX_SAR is in timer mode (i.e., AUTO=0 in Data TX_SAR Control Register at 103Eh). A value of all zeros disables data cell transmission. The time between cells is determined as follows: $\Delta(\text{Seconds}) = \frac{65535}{mclk(Hz)} \times DCGP$
Reserved	15:10	R/O	Always reads “0000_00”.

Table 39 - Data Cell Generation Time Out Register

Address: 1042 (Hex)
Label: DTSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TCBE	0	R/O	Transmit Cell Buffer Empty. This bit is set when the read pointer is equal to the write pointer and indicates that all of the cells in the buffer have been sent. This bit is cleared when the TDSENB bit in the DTCR register at 103Eh is cleared.
Reserved	15:1	R/O	Always reads “0000_0000_0000_000”.

Table 40 - Data TX_SAR Status Register

Address: 1044 (Hex)
Label: TXEN
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXENB	0	R/W	When cleared, the TX_SAR will not produce UDT or SDT cells for any port.
Reserved	15:1	R/O	Always reads “0000_0000_0000_000”.

Table 41 - TX_SAR Master Enable Register

6.2.3 UDT RX_SAR Module

Address: 2000 (Hex)
Label: URCR
Reset Value: 00FF (Hex)

Label	Bit Position	Type	Description
UDT_DUMMY	7:0	R/W	UDT RX_SAR Dummy Cell Octet. This octet is inserted into a port’s UDT Reassembly Circular Buffer 47 times when dummy cell insertion is required. **Defaults to FFh, to represent silence**.
UDT_INSERT_ LOST	8	R/W	UDT Insert Number of Lost Cells Flag. When set, the number of dummy cells inserted into the UDT Reassembly Circular Buffer in the case of a multi-cell loss equals the number of lost cells (up to 7). When this bit is cleared (**default**), a maximum of 2 dummy cells are inserted in a multi-cell loss case.
CHECK_ LATE_ARRIVALS	9	R/W	Check for Late Cell Arrivals in UDT mode. When set, this bit causes a dummy cell to be inserted into the UDT Reassembly Circular Buffer for the corresponding port, if the late cell timeout period for this port is passed while the port is in “sync”. The late cell timeout period for the port is configured in the port’s Timeout Configuration Register at 3200h + p*2h. **Default value: disabled.**
Reserved	15:10	R/O	Always reads “0000_00”.

Table 42 - UDT Reassembly Control Register

Address: 2002 (Hex)
Label: URSER
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
UDT_REASS_ ROLL_SE	0	R/W	When set, the assertion of the Reassembled Cells Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_HDR_ROLL _SE	1	R/W	When set, the assertion of the AAL1 Header Byte Error Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_SEQ_ROLL _SE	2	R/W	When set, the assertion of the AAL1 Sequence Error Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_LOST_ ROLL_SE	3	R/W	When set, the assertion of the Lost Cells Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.

Table 43 - UDT Reassembly Service Enable Register

Address: 2002 (Hex)
Label: URSER
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
UDT_MIS_ROLL_SE	4	R/W	When set, the assertion of the Misinserted Cells Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_UNDER_ROLL_SE	5	R/W	When set, the assertion of the Buffer Underrun Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_OVER_ROLL_SE	6	R/W	When set, the assertion of the Buffer Overrun Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
UDT_LATE_ROLL_SE	7	R/W	When set, the assertion of the Late Cells Counter Rollover status bit in a UDT Reassembly Control Structure will cause the UDT_RXSAR_STATUS bit to be set in the UDT Reassembly Status Register at 2004h.
Reserved	15:8	R/O	Always reads “0000_0000”.

Table 43 - UDT Reassembly Service Enable Register

Address: 2004 (Hex)
Label: URSR
Reset Value: 001F (Hex)

Label	Bit Position	Type	Description
SERVICE_PORT	4:0	R/O	TDM port associated with the last UDT Reassembly Control Structure to generate a serviceable event (i.e., a control structure status field rollover). **Defaults to 1Fh (illegal port) and returns to 1Fh when the UDT_RXSAR_STATUS bit in this register is cleared.**
Reserved	11:5	R/O	Always reads “0000_000”.
CELL_COUNTER_RO_SE	12	R/W	UDT RX_SAR Cell Counter Rollover Service Enable When set, a ‘1’ on CELL_COUNTER_RO_STATUS in this register will cause the UDT_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
CELL_COUNTER_RO_STATUS	13	R/O/L	If set, indicates that the UDT RX_SAR Cell Counter located in register 2006h has overflowed.
UDT_RXSAR_SE	14	R/W	UDT RX_SAR Service Enable. When set, a ‘1’ on UDT_RXSAR_STATUS in this register will cause the UDT_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
UDT_RXSAR_STATUS	15	R/O/L	If set, indicates that an unmasked (due to settings of the Service Enable bits in the UDT Reassembly Service Enable Register at 2002h) UDT RX_SAR serviceable event has occurred. Writing a ‘0’ to this bit clears it and sets SERVICE_PORT to 1Fh.

Table 44 - UDT Reassembly Status Register

Address: 2006 (Hex)
Label: URCCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_COUNTER	15:0	R/O	Number of cells received by the UDT RX_SAR.

Table 45 - UDT Reassembly Cell Counter Register

6.2.4 Data RX_SAR Module

Address: 2020 (Hex)
Label: DRCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
DRENB	0	R/W	Data RX_SAR Enable. When cleared, the Data RX_SAR Write Pointer (DRWP at 2026h) is reset to 00h and all received data cells are ignored. When set, received data cells are processed normally. **Default of '0' means that the Data RX_SAR is usually disabled.**
DROR_SE	1	R/W	Data RX_SAR Cell Buffer Overrun Service Enable. When set, a '1' on DROR in Register 2022h will cause the DATA_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
DRCA_SE	2	R/W	Data RX_SAR Cell Arrival Service Enable. When set, a '1' on DRCA in Register 2022h will cause the DATA_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
DRBHF_SE	3	R/W	Data RX_SAR Buffer Half Full Service Enable. When set, a '1' on DRBHF in Register 2022h will cause the DATA_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
DRCCR_SE	4	R/W	Data RX_SAR Cell Counter Rollover Service Enable. When set, a '1' on DRCCR in Register 2022h will cause the DATA_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
Reserved	15:5	R/O	Always reads "0000_0000_000".

Table 46 - Data RX_SAR Control Register

Address: 2022 (Hex)
Label: DRSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	0	R/O	Always reads '0'.
DROR	1	R/O/L	Data RX_SAR Cell Buffer Overrun Error. If this bit is set, the DRWP (Register 2026h) = DRRP (Register 2028h). This signifies that either a non-CBR cell has been overwritten or is about to be overwritten. Software must take appropriate actions to adjust the read pointer so that further overruns do not occur. Writing a '0' to this bit clears it.
DRCA	2	R/O/L	Data RX_SAR Cell Arrival. This bit is set each time a data cell is written to the Data RX_SAR Cell Buffer. Writing a '0' to this bit clears it.
DRBHF	3	R/O/L	Data RX_SAR Buffer Half Full This bit is set when the buffer is determined to be half full by comparing the read and write pointers. Writing a '0' to this bit clears it.
DRCCR	4	R/O/L	Data RX_SAR Cell Counter Rollover. This bit is set when the Data RX_SAR Cell Counter, located in register 202Ah, overflows. Writing a '0' to this bit clears it.
Reserved	15:5	R/O	Always reads "0000_0000_000".

Table 47 - Data RX_SAR Status Register

Address: 2024 (Hex)
Label: DRCON
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
DRSIZE	1:0	R/W	Data RX_SAR Cell Buffer Size. This field indicates the number of non-CBR data cells which can be held in the Data RX_SAR's Cell Buffer: "00" = 16 cells "01" = 32 cells "10" = 64 cells "11" = 128 cells.
DRBASE	12:2	R/W	Data RX_SAR Cell Buffer Base Address. Represents address bits <19:9> that point to the **word** address of the first structure in the cell buffer in external memory. The lower address bits <8:0> of the pointer are preset to "0_0000_0000". **Cell buffers must start on boundaries corresponding to the size of the buffer (e.g., 32-cell buffers must start on boundaries which are integer multiples of 32 cells * 32 words/cell)**. As a result, in some cases, DRBASE<2:0> (bits<11:9> of the actual address) must to be set to '0', depending on the number of cells allocated in the cell buffer: **16**-cell buffer: **no restrictions** **32**-cell buffer: **DRBASE<0> must equal '0'** (buffers start on 1024-word boundaries) **64**-cell buffer: **DRBASE<1:0> must equal "00"** (buffers start on 2048-word boundaries) **128**-cell buffer: **DRBASE<2:0> must equal "000"** (buffers start on 4096-word boundaries).
Reserved	15:13	R/O	Always reads "000".

Table 48 - Data RX_SAR Configuration Register

Address: 2026 (Hex)
Label: DRWPR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
DRWP	6:0	R/O	Data RX_SAR Cell Buffer Write Pointer. Indicates the cell structure number which is currently being written by the Data RX_SAR (the cell is not yet valid). This value is incremented at the end of each cell-write procedure (indicates the **next** cell location to be written). Allowable values: 0h -> Fh (16-cell buffer) 0h -> 1Fh (32-cell buffer) 0h -> 3Fh (64-cell buffer) 0h -> 7Fh (128-cell buffer).
Reserved	15:7	R/O	Always reads "0000_0000_0".

Note: The write pointer value is cleared to "00h" upon start-up and each time that the DRENB bit is cleared (i.e., when the Data RX_SAR is disabled, the write pointer is automatically cleared to "00h").

Table 49 - Data RX_SAR Write Pointer Register

Address: 2028 (Hex)
Label: DRRPR
Reset Value: 007F (Hex)

Label	Bit Position	Type	Description
DRRP	6:0	R/W	Data RX_SAR Cell Buffer Read Pointer. Indicates the cell structure number which is currently being read by the CPU. This value **should not** be incremented by the CPU at the end of a cell-read; therefore, if a read operation is not in progress, the pointer indicates the cell location which was **last** read by the microprocessor.
Reserved	15:7	R/O	Always reads “0000_0000_0”.

Note: The read pointer value is set to “7Fh” upon start-up, pointing to the final location within the cell buffer. Upon the start of the first read operation, software should increment the pointer to point to the first cell location.

Table 50 - Data RX_SAR Read Pointer Register

Address: 202A (Hex)
Label: DRCCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_COUNTER	15:0	R/O	Number of cells received by the Data RX_SAR.

Table 51 - Data RX_SAR Cell Counter Register

6.2.5 SDT RX_SAR Module

Address: 2040 (Hex)
Label: SRCR
Reset Value: 00FF (Hex)

Label	Bit Position	Type	Description
SDT_DUMMY	7:0	R/W	SDT RX_SAR Dummy Cell Octet. A 47-byte cell filled with this octet is inserted into the appropriate SDT Reassembly Circular Buffer(s) when dummy cell insertion is required. **Defaults to FFh, but should be set to appropriate silence value for the TDM type.**
SDT_INSERT_LOST	8	R/W	SDT Insert Number of Lost Cells Flag. When set, the number of dummy cells inserted into the SDT Reassembly Circular Buffer(s) in the case of a multi-cell loss equals the number of lost cells (up to 6). When this bit is cleared (**default**), a maximum of 2 dummy cells are inserted in a multi-cell loss case.
CB_BASE_ADD	10:9	R/W	Reassembly Circular Buffer Base Address. These bits form the 2 MSBs (bits<19:18>) of the external memory base addresses (in **words**) of the SDT Reassembly Circular Buffers.
Reserved	15:11	R/O	Always reads “0000_0”.

Table 52 - SDT Reassembly Control Register

Address: 2042 (Hex)
Label: SRSER
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SDT_REASS_ ROLL_SE	0	R/W	When set, the assertion of the Reassembled Cells Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_HDR_ROLL _SE	1	R/W	When set, the assertion of the AAL1 Header Byte Error Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_SEQ_ROLL _SE	2	R/W	When set, the assertion of the AAL1 Sequence Error Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_LOST_ ROLL_SE	3	R/W	When set, the assertion of the Lost Cells Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_MIS_ROLL_ SE	4	R/W	When set, the assertion of the Misinserted Cells Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
REFRAME_ROLL _SE	5	R/W	When set, the assertion of the Pointer Reframes Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
PARITY_ROLL_ SE	6	R/W	When set, the assertion of the Pointer Parity Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_UNDER_ ROLL_SE	7	R/W	When set, the assertion of the Buffer Underrun Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
SDT_OVER_ ROLL_SE	8	R/W	When set, the assertion of the Buffer Overrun Counter Rollover status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
POINTER_OUT_ OF_RANGE_SE	9	R/W	When set, the assertion of the Pointer Out-of-Range status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
CAS_CHANGE_ SE	10	R/W	When set, the assertion of the CAS Changed status bit in an SDT Reassembly Control Structure will cause the SDT_RXSAR_STATUS bit to be set in the SDT Reassembly Status Register at 2044h.
Reserved	15:11	R/O	Always reads “0000_0”.

Table 53 - SDT Reassembly Service Enable Register

Address: 2044 (Hex)
Label: SRSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SERVICE_ADD	13:0	R/O	Base **word** address of the last SDT Reassembly Control Structure to generate a serviceable event (i.e., a status field rollover or bit setting). **This field is cleared when the SDT_RXSAR_STATUS bit in this register is cleared.**
SDT_RXSAR_SE	14	R/W	SDT RX_SAR Service Enable. When set, a '1' on SDT_RXSAR_STATUS in this register will cause the SDT_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
SDT_RXSAR_STATUS	15	R/O/L	If set, indicates that an unmasked (due to the settings of the Service Enable bits in the SDT Reassembly Service Enable Register at 2042h) SDT RX_SAR serviceable event has occurred. Writing a '0' to this bit clears it and clears the SERVICE_ADD field.

Table 54 - SDT Reassembly Status Register

Address: 2046 (Hex)
Label: SRCSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_COUNTER_RO_SE	0	R/W	SDT RX_SAR Cell Counter Rollover Service Enable. When set, a '1' on CELL_COUNTER_RO_STATUS in this register will cause the SDT_RXSAR_SRV bit to be set in the Main Status Register at 0002h.
CELL_COUNTER_RO_STATUS	1	R/O/L	If set, indicates that the SDT Reassembly Cell Counter Register in register 2048h has overflowed. Writing a '0' to this bit clears it.
Reserved	15:2	R/O	Always reads "0000_0000_0000_00".

Table 55 - SDT Reassembly Cell Counter Status Register

Address: 2048 (Hex)
Label: SRCCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_COUNTER	15:0	R/O	Number of cells received by the SDT RX_SAR.

Table 56 - SDT Reassembly Cell Counter Register

6.2.6 Reassembly-Side Timeout Module

Address: 3000 (Hex)
Label: MTCR
Reset Value: 09C4 (Hex)

Label	Bit Position	Type	Description
CUT_VC _PERIOD	15:0	R/W	Reassembly Cell Loss Integration Period. If cells on a VC are continuously lost for this period of time (given in ms), the CUT_VC_STATUS bit is set in the Timeout Configuration Register (3200h + p*2h) corresponding to the VC's "VC TDM Port". **Default value = 2.5 s.**

Table 57 - MIB Timeout Configuration Register

Address: 3002 (Hex)
Label: MTSR1
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
STATUS_0	0	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 0.
STATUS_1	1	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 1.
STATUS_2	2	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 2.
STATUS_3	3	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 3.
STATUS_4	4	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 4.
STATUS_5	5	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 5.
STATUS_6	6	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 6.
STATUS_7	7	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 7.
STATUS_8	8	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 8.
STATUS_9	9	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 9.
STATUS_10	10	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 10.
STATUS_11	11	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 11.
STATUS_12	12	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 12.
STATUS_13	13	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 13.
STATUS_14	14	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 14.
STATUS_15	15	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 15.

Table 58 - MIB Timeout Status Register 1

Address: 3004 (Hex)
Label: MTSR2
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
STATUS_16	0	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 16.
STATUS_17	1	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 17.
STATUS_18	2	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 18.
STATUS_19	3	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 19.
STATUS_20	4	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 20.
STATUS_21	5	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 21.
STATUS_22	6	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 22.
STATUS_23	7	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 23.
STATUS_24	8	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 24.
STATUS_25	9	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 25.
STATUS_26	10	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 26.
STATUS_27	11	R/O	If set, indicates that either an unmasked late cell event or an unmasked cut VC event has occurred on port 27.
Reserved	15:12	R/O	Always reads “0000”.

Table 59 - MIB Timeout Status Register 2

Address: 3200 + p*2 (Hex)
Label: TCR_Pp (where p represents the port number)
Reset Value: 07FF (Hex)

Label	Bit Position	Type	Description
LATE_CELL_ PERIOD	10:0	R/W	Late Cell Timeout. If a cell has not been received prior to this timeout (measured in 125µs increments), an internal flag is set, indicating a late cell arrival. This timer should generally be set to a value equal to the cell assembly time, plus the expected CDV. **Default: 256 ms** In UDT mode, if this timeout period is passed, the LATE_CELL_STATUS bit in this per-port register will be set. Additionally, if the CHECK_LATE_ARRIVALS bit is set in the UDT Reassembly Control Register at 2000h, a dummy cell will also be inserted into the UDT Reassembly Circular Buffer for the port.
LATE_CELL_ SE	11	R/W	Late Cell Status Service Enable. When set, a '1' on LATE_CELL_STATUS in this register will cause the RX_TIMEOUT_SRV bit to be set in the Main Status Register at 0002h. As well, the per-port status bit for the corresponding port will be set in one of the MIB Timeout Status Registers at 3002h or 3004h.
LATE_CELL_ STATUS	12	R/O/L	If set, indicates that a late cell event has occurred on this port. This bit can be cleared by writing with '0'. **Note: This bit will only be set if a port is operating in UDT mode.**
CUT_VC_SE	13	R/W	Cut VC Status Service Enable. When set, a '1' on CUT_VC_STATUS in this register will cause the RX_TIMEOUT_SRV bit to be set in the Main Status Register at 0002h. As well, the per-port status bit for the corresponding port will be set in one of the MIB Timeout Status Registers at 3002h or 3004h.
CUT_VC_ STATUS	14	R/O/L	If set, indicates that a cut VC event has occurred on this port (i.e, the CUT_VC_PERIOD set in the MIB Timeout Configuration Register at 3000h has been passed without a cell arrival). This bit can be cleared by writing with '0'.
Reserved	15	R/O	Always reads '0'.

Table 60 - Timeout Configuration Register (one per port)

6.2.7 UTOPIA Interface Module

Address: 4000 (Hex)
Label: UCR
Reset Value: 0004 (Hex)

Label	Bit Position	Type	Description
SDT_N_UDT	0	R/W	SDT/$\overline{\text{UDT}}$. Selects between SDT mode (when set) and UDT mode (when cleared). To operate in both modes simultaneously, this bit must be cleared. When operating in UDT mode, the UDT VCI/VPI comparison is performed followed by the LUT (if necessary). In SDT mode, the look-up is performed first (the UDT VPI/VCI comparison is skipped).
UNI_N_NNI	1	R/W	UNI/$\overline{\text{NNI}}$. Selects between UNI (when set) and NNI mode (when cleared). If NNI mode is enabled, the GFC field of the cell header will be used in the UDT VPI/VCI comparison.

Table 61 - UTOPIA Configuration Register

Address: 4000 (Hex)
Label: UCR
Reset Value: 0004 (Hex)

Label	Bit Position	Type	Description
UTO_CLK_SEL	2	R/W	Selects between an external clock (when set) and an internal clock (when cleared). If an internal clock is selected, UTO_IN_CLK and UTO_OUT_CLK are outputs, and the frequency of the generated clock is equivalent to MCLK/2. If an external clock is selected, UTO_IN_CLK and UTO_OUT_CLK are inputs.
GLOBAL_OAM_SEL	3	R/W	Global OAM Select. When this bit is set, received OAM cells are kept for further processing. When this bit is low, OAM cells are discarded.
EIGHT_N_SIXTEEN	4	R/W	8-bit mode/16-bit mode. Selects between UTOPIA eight-bit (when set) and sixteen-bit (when cleared) operation.
LEVEL1_N_LEVEL2	5	R/W	Level1/Level2. Selects between UTOPIA Level 1 (when set) and UTOPIA Level 2 (when cleared) operation.
UKSEL	6	R/W	When this bit is set, cells which have unknown routing according to the look-up table are placed in the Receive Data Cell Buffer; otherwise these cells are discarded.
CLAV_TRI_OVERRIDE	7	R/W	When set, this bit forces the CLAV signals to always drive a defined value. When this bit is cleared, the CLAV signals become high impedance following a clock cycle in which the MT90528 is not polled.
DATA_TRI_OVERRIDE	8	R/W	When set, this bit forces UTO_OUT_SOC and UTO_OUT_DATA to always drive defined values. When this bit is low, the UTO_OUT_SOC and the UTO_OUT_DATA signals become high impedance, as defined in the ATM Forum UTOPIA Level 2 specification.
PHY_N_ATM	9	R/W	PHY/ATM. When set, the MT90528's UTOPIA interface will operate in PHY mode; when the bit is cleared, the MT90528's UTOPIA interface will operate in ATM mode.
DEVICE_ADDRESS	14:10	R/W	Defines the address of the MT90528 device used to compare to the UTO_IN_ADD and UTO_OUT_ADD buses when operating in MPHY mode. **Note:** Only addresses 00h to 1Eh are valid.
UTO_CLK_ CONFIGURED	15	R/W	The user must set this bit at least one clock cycle after the UTO_CLK_SEL bit has been programmed. **For normal operation of the UTOPIA port, this bit must be set and must not be cleared.** This bit should be set only once the UTOPIA is fully programmed (including the LUT, which should be cleared (all the entries set to 0003h) even if not used).

Table 61 - UTOPIA Configuration Register

Address: 4002 (Hex)
Label: UNCB
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
M	3:0	R/W	M least-significant bits of the VPI used for external memory look-ups. **The valid range for this value is 0 to 12.**
N	8:4	R/W	N least-significant bits of the VCI used for external memory look-ups. **The valid range for this value is 4 to 16.**
BACK_TO_BACK _DISABLED	9	R/W	When asserted this bit will force the RX UTOPIA ATM state machine to pause after each cell reception by driving the UTO_IN_ENBATM_ CLAVPHY signal to '1'

Table 62 - UTOPIA Number of Concatenated Bits Register

Address: 4002 (Hex)
Label: UNCB
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	15:10	R/O	Always reads “0000_00”.

Note: The contents of this register are used to determine how many bits of the cell header are used to form the look-up table addresses. The user selects up to 16 of the bits of the GFC/VPI and VCI fields to be used for the look-up table search. A minimum of 4 bits (from the VCI) and a maximum of 16 bits (all from the VCI or from a combination of both the VCI and VPI) of the header must be used for searches.

Table 62 - UTOPIA Number of Concatenated Bits Register

Address: 4004 (Hex)
Label: ULBA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
LUT_BASE_ADD	15:0	R/W	Contains the 16 most significant bits of the Look-Up Table base address. These bits represent **byte** address bits<20:5> of the external memory. **If N+M is greater than 4, bits<(N+M):5> of the Look-Up Table base address should be set to 0. (For example, if N+M=7, bits<7:5> should be set to “000”)**

Table 63 - LUT Base Address Register

Address: 4006 (Hex)
Label: UVCM
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VC_MATCH	15:0	R/W	Contains match values for each of the bits in the VCI.

Table 64 - VC Match Register

Address: 4008 (Hex)
Label: UVCME
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VC_MATCH_ENB	15:0	R/W	Each bit, when set, enables the comparison of a cell’s VCI and the corresponding VC_MATCH bit. If a bit in this register is not set, the corresponding bit in the received cell VCI is considered valid, regardless of the setting in the VC_MATCH field.

Table 65 - VC Match Enable Register

Address: 400A (Hex)
Label: UVPM
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VP_MATCH	11:0	R/W	Contains match values for each of the twelve bits in the VPI (including the GFC field).
Reserved	15:12	R/O	Always reads “0000”.

Table 66 - VP Match Register

Address: 400C (Hex)
Label: UVPME
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VP_MATCH_ENB	11:0	R/W	Each bit, when set, enables the comparison of a cell’s VPI and the corresponding VP_MATCH bit. If a bit in this register is not set, the corresponding bit in the received cell VPI is considered valid, regardless of the setting in the VP_MATCH field. In UNI mode, bits<11:8> should be cleared to avoid the comparison of the GFC.
Reserved	15:12	R/O	Always reads “0000”.

Table 67 - VP Match Enable Register

Address: 400E (Hex)
Label: UPM
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
PARITY_ MISMATCHES	15:0	R/O	Contains a count of the mismatches between UTO_IN_DATA and UTO_IN_PARITY. If this counter rolls over, the PARITY_ROLL_STATUS bit in the UTOPIA Status Register at 4012h will be set.

Table 68 - UTOPIA Parity Mismatches Register

Address: 4010 (Hex)
Label: UFS
Reset Value: 0030 (Hex)

Label	Bit Position	Type	Description
UTOPIA_ LOOPBACK	0	R/W	When set, this bit forces the UTOPIA port into loopback mode. Data is looped from the incoming UTOPIA bus to the outgoing UTOPIA bus, through the incoming UTOPIA FIFO and the outgoing UTOPIA FIFO. The incoming data is filtered by the Match and Match Enable filters before being re-transmitted.
UTO_OUT_FIFO_ RESET	1	R/W	When set, empties the outgoing UTOPIA FIFO.
UTO_IN_FIFO_ RESET	2	R/W	When set, empties the incoming UTOPIA FIFO.

Table 69 - UTOPIA FIFO Status Register

Address: 4010 (Hex)
Label: UFS
Reset Value: 0030 (Hex)

Label	Bit Position	Type	Description
UTO_OUT_FIFO_ FULL	3	R/O	If set, this bit indicates that the outgoing UTOPIA FIFO is full.
UTO_OUT_FIFO EMPTY	4	R/O	If set, this bit indicates that the outgoing UTOPIA FIFO is empty.
UTO_IN_FIFO_ EMPTY	5	R/O	If set, this bit indicates that the incoming UTOPIA FIFO is empty.
UTO_IN_FIFO_ FULL	6	R/O	If set, this bit indicates that the incoming UTOPIA FIFO is full.
Reserved	15:7	R/O	Always reads “0000_0000_0”.

Table 69 - UTOPIA FIFO Status Register

Address: 4012 (Hex)
Label: USR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_CNT_ROLL _STATUS	0	R/O/L	If set, this status bit indicates that the UTOPIA interface has received 2^{16} cells, as counted by the UTOPIA Incoming Cell Counter at 4016h.
PARITY_ROLL_ STATUS	1	R/O/L	If set, this status bit indicates that the UTOPIA interface has received 2^{16} data words containing parity errors, as counted by the UTOPIA Parity Mismatches Register at 400Eh.
Reserved	15:2	R/O	Always reads “0000_0000_0000_00”.

Table 70 - UTOPIA Status Register

Address: 4014 (Hex)
Label: USER
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_CNT_ROLL _SE	0	R/W	When set, a ‘1’ on CELL_CNT_ROLL_STATUS will cause the UTOPIA_SRV bit to be set in the Main Status Register at 0002h.
PARITY_ROLL_ SE	1	R/W	When set, a ‘1’ on PARITY_ROLL_STATUS will cause the UTOPIA_SRV bit to be set in the Main Status Register at 0002h.
Reserved	15:2	R/O	Always reads “0000_0000_0000_00”.

Table 71 - UTOPIA Service Enable Register

Address: 4016 (Hex)
Label: UICC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CELL_CNT	15:0	R/O	Counter indicating the number of cells received by the UTOPIA interface. If this counter rolls over, the CELL_CNT_ROLL_STATUS status bit in the UTOPIA Status Register at 4012h will be set. **Note:** This counter counts the number of SOC signals detected at the incoming UTOPIA interface. Therefore, both “good” and errored cells are counted.

Table 72 - UTOPIA Incoming Cell Counter

Address: 4200 + p*4 (Hex)
Label: UVC_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
UDT_VCI	15:0	R/W	UDT VCI for TDM port p. The VCI value of the incoming cell is compared to this value to determine if the cell is destined for port p.

Table 73 - UDT VCI for Port p (one per port)

Address: 4202 + p*4 (Hex)
Label: UVP_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
UDT_VPI	11:0	R/W	UDT VPI for TDM port p. The VPI value of the incoming cell is compared to this value to determine if the cell is destined for port p. In UNI mode, only the 8 least significant bits of this field are used for the comparison. In NNI mode, all 12 bits are used.
OAM_SEL	12	R/W	OAM select for port p. When set, OAM cells with matching VPI/VCI are sent to the Receive Data Cell Buffer. When cleared, OAM cells arriving on this VC are discarded.
Reserved	15:13	R/O	Always reads “000”.

Table 74 - UDT VPI for Port p (one per port)

6.2.8 Clock Management Module

Address: 5000 (Hex)
Label: CMCR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
SLV_N_MSTR	0	R/W	Slave/Master. When set, the signals F0 and C4M_C2M are sourced from the TDM backplane (inputs). When cleared, the MT90528 generates these signals (outputs). **When the MT90528 is not operating in backplane mode, this bit should be set to 1 (i.e., slave mode). Furthermore, if operating in backplane mode, this bit should only be cleared if the user wishes the MT90528 to control the F0 and C4M_C2M backplane signals.**
EXT_N_INT	1	R/W	External/Internal. When set, the common clock and the “master” C4M_C2M and F0 signals are generated from the clock input to the MT90528 at TDM_CLK (this is usually sourced from an external PLL). When cleared and if in master mode, the C4M_C2M and F0 signals are generated from an internal version of the output signal PRI_REF.
F0_MODE	4:2	R/W	Frame Pulse Format Selector. F0_MODE<0> - Frame Pulse Polarity (used only in Generic mode): ‘0’ = Negative polarity ‘1’ = Positive polarity. F0_MODE<1> - Frame Pulse Trigger Edge (used only in Generic mode): ‘0’ = Negative-edge trigger ‘1’ = Positive-edge trigger. F0_MODE<2> - Frame Pulse Format: ‘0’ = Generic ‘1’ = ST-BUS.
8_KHZ_SEL	5	R/W	Internal 8 kHz clock source. Used to select the origin of the 8 kHz clock source used by the internal PLLs. When set, the 8 kHz clock is generated as a divided-down version of the 19.44 MHz clock input to the MT90528 at PHY_CLK. When cleared, an 8 kHz clock is expected to be input directly at PHY_CLK.
FNXI1_RATE	8:6	R/W	FNXI Rate Selector 1. (See Notes 1 and 2) These bits are used to select the rate of the FNXI clock (#1) from which outgoing RTS values will be generated, and to which incoming RTS values will be compared: “000” = 75,937.5 Hz “001” = 151,875 Hz “010” = 303,750 Hz “011” = 607,500 Hz “100” = 1.215 MHz “101” = 2.43 MHz (UDT rate) “110” = 4.86 MHz “111” = 9.72 MHz.

Table 75 - Clock Management Configuration Register

Address: 5000 (Hex)
Label: CMCR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
FNXI2_RATE	11:9	R/W	FNXI Rate Selector 2. (See Notes 1 and 2) These bits are used to select the rate of the FNXI clock (#2) from which outgoing RTS values will be generated, and to which incoming RTS values will be compared: “000” = 75,937.5 Hz “001” = 151,875 Hz “010” = 303,750 Hz “011” = 607,500 Hz “100” = 1.215 MHz “101” = 2.43 MHz (UDT rate) “110” = 4.86 MHz “111” = 9.72 MHz.
BACKPLANE_CLK _CONFIGURED	12	R/W	TDM Backplane Clock Configured Must be set once the C4M_C2M and F0 signals are stable. This bit needs to be high in order to ensure the synchronization of the TDM ports programmed in backplane mode. A toggle of this bit resets the synchronization of all the TDM ports programmed in backplane mode.
Reserved	15:13	R/O	Always reads “000”.

Note 1: Two rates for the FNXI clocks are provided in case different ports of the device are programmed to have SDT timing VCs carrying different numbers of channels.
Note 2: Since RTS support is only provided in SDT mode for VCs carrying up to 32 channels, FNXI rates of 4.86 MHz and 9.72 MHz should not be used.

Table 75 - Clock Management Configuration Register

Address: 5002 (Hex) Label: PLLCS Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
PRI_SEL	5:0	R/W	Primary Clock Source for External PLL. Used to select the primary clock source for the external PLL (signals output on PRI_REF and PRI_LOS). Bits<4:0> indicate which port should provide the clock source (only “00000”:“11011” are valid choices). Bit<5> indicates whether the port’s TDM input clock (STiCLK) or the port’s internally-generated PLL clock should be used as the clock source. ‘0’ = STiCLK; ‘1’ = PLLCLK. **Note:** If the port selected to provide the primary reference experiences an LOS condition, that port’s PLLCLK will be used as PRI_REF, even if the port’s STiCLK is selected via PRI_SEL<5>.
SEC_SEL	11:6	R/W	Secondary Clock Source for External PLL. Used to select the secondary clock source for the external PLL (signals output on SEC_REF and SEC_LOS). Bits<4:0> indicate which port should provide the clock source (only “00000”: “11011” are valid choices). Bit<5> indicates whether the port’s TDM input clock (STiCLK) or the port’s internally-generated PLL clock should be used as the clock source. ‘0’ = STiCLK; ‘1’ = PLLCLK. **Note:** An LOS condition on the port selected to provide the secondary reference clock will have no effect on the selection of the clock source for SEC_REF.
Reserved	15:12	R/O	Always reads “0000”.

Table 76 - External PLL Clock Source Register

Address: 5200 + p*10 (Hex)
Label: CCR_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CLKSEL	1:0	R/W	SToCLK Selector. These bits are used to select the source for the port's SToCLK output signal: "00" = MCLK/2 "01" = STiCLK "10" = PLLCLK (generated by the port's internal PLL) "11" = common clock; sourced from either the TDM_CLK input pin (if the EXT_N_INT bit is set in the Clock Management Configuration Register at 5000h) or from an internal version of the output signal PRI_REF (if the EXT_N_INT bit is cleared). **Note:** If there is an LOS signal received on this port and the user has selected to source SToCLK from STiCLK, the user's configuration will be overridden and SToCLK will be sourced from PLLCLK.
RTSSEL	3:2	R/W	RTS Clock Selector. These bits are used to select the source for the internal RTS clock: "00" = STiCLK (used when transmitting RTS in independent mode or in **ST-BUS backplane** mode) "01" = C4M_C2M (used when transmitting RTS in **Generic backplane** mode) "10" = PLLCLK (used when receiving RTS & performing clock recovery) "11" = Reserved. **Note:** When transmitting RTS from a TDM port that is operating in ST-BUS backplane mode, it is necessary to present a bit-rate clock to the Tx SRTS circuitry. The user must provide this clock by **presenting a 2.048 MHz clock on the STiCLK input of the transmitting port. Due to this restriction, the C4M_C2M backplane clock must be either an input ("slave" mode), or it must be generated from a reference source other than this port's STiCLK input.**
FNXISEL	4	R/W	FNXI Source Selector. This bit is used to select either the FNXI1 or the FNXI2 clock rate for RTS generation or comparison: '0' = FNXI1_RATE '1' = FNXI2_RATE.
PLL_FREQ_SEL	6:5	R/W	Output Frequency Selector for Internal PLL. "00" = 1.544 MHz "01" = 2.048 MHz "10" = 4.096 MHz "11" = Reserved.
PLL_MODE_SEL	8:7	R/W	Operating Mode for Internal PLL. These bits define the operating mode of the PLL. "00" = Normal mode; output synchronized to the input. "01" = Holdover mode; output no longer follows the input, but holds last frequency setting. "10" = Freerun mode; output is fixed to the nominal frequency. "11" = CPU mode; the output frequency is directly controlled by the programmable DCO_DIFF_p value, regardless of PLL_INPUT_SEL.

Table 77 - Clocking Configuration Register (one per port)

Address: 5200 + p*10 (Hex)
Label: CCR_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
PLL_INPUT_SEL	10:9	R/W	PLL input mode. These bits define the input used to generate the PLL's output clock. "00" = Line Clocking mode; input is from the port's STiCLK (can also be used to dejitter the clock for timestamp generation; see Figure 39 on page 100 for an illustration). "01" = SRTS mode; input is a digital Synchronous Residual Time Stamp stream from the RX_SAR. "10" = Network mode; input is the 8 kHz network reference (derived from PHY_CLK pin; see bit<5> of the Clock Management Configuration Register at 5000h). "11" = Adaptive mode; input is determined by the buffer-fill-level from the RX_SAR.
VC_CHANNELS	15:11	R/W	Number of Channels in VC. This field is used when generating or receiving RTS nibbles in SDT mode. It indicates the number of channels in the VC which is carrying timing information for the port. The field must be programmed by the user to be one less than the actual number of channels in the VC (possible values = 00h to 1Fh).

Table 77 - Clocking Configuration Register (one per port)

Address: 5202 + p*10 (Hex)
Label: CPAR_Pp (where p represents the port number)
Reset Value: 8000 (Hex)

Label	Bit Position	Type	Description
PHASE_ACCUM	10:0	R/O	Internal PLL Phase Accumulator. This 2's complement value represents the long-term frequency offset of the output clock from the PLL's centre frequency. This value translates to the frequency offset as follows: freq_offset = (phase_accum/3139881) * 1,544,000 Hz for DS1 mode freq_offset = (phase_accum/4164817) * 2,048,000 Hz for E1 mode freq_offset = (phase_accum/4164817) * 4,096,000 Hz for C4 mode.
Reserved	14:11	R/O	Always reads "0000".
PHASE_LIMITER	15	R/O	Internal PLL Phase Limiter. When cleared, indicates that the PLL is limiting its phase detector output so that the PLL output phase changes no more than 6 ns / 125 µs. A change of more than 6 ns / 125 µs typically occurs when the PLL is **not** locked or when there is large jitter on the input signal of the PLL. When PHASE_LIMITER is high for approximately 30 seconds, one can assume that the PLL is in lock; contrarily, when PHASE_LIMITER is low for approximately 30 seconds, the PLL is out of lock.

Note: The reset value of this register can only be read as 8000h if the corresponding PLL is disabled (bit<0> cleared in the PLL Enable Register, located at address 5208h+p*10h).

Table 78 - Clocking Phase Accumulator Register (one per port)

Address: 5204 + p*10 (Hex)
Label: CDDR_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
DCO_DIFF	11:0	R/W	Frequency offset value. When PLL_MODE_SEL (in register 5200h + p*10h) is set to CPU mode, the value in this field is used to set the PLL output frequency directly, instead of using the filter output. In CPU mode, the PLL input selected by PLL_INPUT_SEL (in register 5200h + p*10h) is no longer used. Data read from this field is interpreted as 2's complement format.
Reserved	15:12	R/O	Always reads "0000".

Table 79 - Clocking DCO Difference Register (one per port)

Address: 5206 + p*10 (Hex)
Label: CSFSR_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RX_OVERFLOW_ERROR	0	R/O/L	Receive SRTS FIFO Overflow Error. If set, the Receive SRTS FIFO has overflowed. Writing a '0' to this bit clears it.
RX_UNDERFLOW_ERROR	1	R/O/L	Receive SRTS FIFO Underflow Error. If set, the Receive SRTS FIFO has underrun. Writing a '0' to this bit clears it.
TX_OVERFLOW_ERROR	2	R/O/L	Transmit SRTS FIFO Overflow Error. If set, the Transmit SRTS FIFO has overflowed. Writing a '0' to this bit clears it.
TX_UNDERFLOW_ERROR	3	R/O/L	Transmit SRTS FIFO Underflow Error. If set, the Transmit SRTS FIFO has underrun. Writing a '0' to this bit clears it.
Reserved	15:4	R/O	Always reads "0000_0000_0000".

Table 80 - SRTS FIFO Status Register (one per port)

Address: 5208 + p*10 (Hex)
Label: PLLEN_Pp (where p represents the port number)
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
PLL_ENABLE	0	R/W	When cleared, the PLL for this port is held in reset.
Reserved	15:1	R/O	Always reads "0000_0000_0000_000".

Table 81 - PLL Enable Register (one per port)

6.2.9 TDM Interface Module

Address: 6000 (Hex)
Label: MAINTDM1
Reset Value: FFFF (Hex)

Label	Bit Position	Type	Description
IDLE_DATA	7:0	R/W	User-programmable idle data. (Applies only to SDT mode.) When a channel is idle (I bit is set in the corresponding TDM SDT Reassembly Control Structure), idle data is output on DSTo.
SILENCE_DATA	15:8	R/W	User-programmable silence data. (Applies only to SDT mode.) When a channel is experiencing a TDM underrun, this silence data is output on DSTo if REPLAY_N_SILENCE is cleared in the TDM Control Register 3 for that port.

Table 82 - Main TDM Control Register 1

Address: 6002 (Hex)
Label: MAINTDM2
Reset Value: F000(Hex)

Label	Bit Position	Type	Description
Reserved	11:0	R/O	Always reads “0000_0000_0000”.
IDLE_CAS	15:12	R/W	User-programmable idle CAS. (Applies only to SDT mode.) When a channel is idle (I bit is set in the corresponding TDM SDT Reassembly Control Structure), idle CAS nibbles are output on CSTo.

Table 83 - Main TDM Control Register 2

Address: 6200 + p*10 (Hex)
Label: TDM1_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM_CIR_BUF_LPBK	0	R/W	TDM Circular Buffer Loopback. (Applies only to SDT mode.) ‘0’ = Normal operation. ‘1’ = Data input on DSTi is output on DSTo, after routing through the SDT circular buffers in external memory.
TDM_LOS_CLK	1	R/W	Incoming Loss of Signal. (Applies only to UDT mode.) ‘0’ = Normal operation (continue to use STiCLK during an LOS condition). ‘1’ = Switch to MT90528’s internal clock source if loss of signal is detected on CSTi/LOSi.
TDM_LOS_POL	2	R/W	Incoming TDM LOS Polarity. (Applies only to UDT mode; must be set in SDT mode.) ‘0’ = Negative polarity (i.e., zero on CSTi/LOSi means loss of signal). ‘1’ = Positive polarity (i.e., one on CSTi/LOSi means loss of signal).
TDM_CAS_LOCATION	3	R/W	TDM Signalling. (Applies only to SDT mode.) ‘0’ = Signalling nibbles are located in the LS four bits of each channel. ‘1’ = Signalling nibbles are located in the MS four bits of each channel.

Table 84 - TDM Control Register 1 (one per port)

Address: 6200 + p*10 (Hex)
Label: TDM1_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM_MAPPING_SCH	4	R/W	TDM Mapping Scheme. (Applies only to an incoming DS1 link in SDT mode.) In Generic mode: ‘0’ = Use first 24 channels. ‘1’ = Use 3 channels out of every 4. In ST-BUS mode, this bit must be cleared.
TDM_PULSE_SEL	5	R/W	TDM Frame Pulse Selection. (Applies only to SDT mode.) ‘0’ = STiMF pin is a frame pulse. ‘1’ = STiMF pin is a multiframe pulse. In Backplane SDT mode, this bit must cleared.
TDM_PULSE_POL	6	R/W	TDM Frame Pulse Polarity. (Applies only to SDT mode.) In Generic mode: ‘0’ = Negative polarity. ‘1’ = Positive polarity. In ST-BUS mode, this bit must be cleared.
TDM_CLK_POL	7	R/W	Segmentation TDM Input Clock Polarity. ‘0’ = TDM data is sampled on the rising edge. ‘1’ = TDM data is sampled on the falling edge. In ST-BUS SDT mode, this bit must be set.
TDM_CLK_RATE	8	R/W	TDM Clock Rate. ‘0’ = TDM clock is 1.544 MHz. ‘1’ = TDM clock is 2.048 MHz or 4.096 MHz.
TDM_LINK_TYPE	9	R/W	TDM Link Type. ‘0’ = E1 link. ‘1’ = DS1 link.
INT_LOS_ENABLE	10	R/W	Internal LOS Enable (Applies only to UDT mode). ‘0’ = Internal version of LOS disabled. ‘1’ = Internal version of LOS enabled. If this bit is set, the occurrence of an LOS event on the port will be propagated throughout the device, possibly influencing the signals output on PRI_REF, PRI_LOS, and the port’s SToCLK. This bit must be set if TDM_LOS_CLK (bit<1>) is set.
TDM_CLK_MODE	11	R/W	TDM Clocking Mode. (Applies only to SDT mode; must be cleared in UDT mode.) ‘0’ = Independent mode (Independent clocks and frame pulses) ‘1’ = Backplane mode (Common clock and frame pulse)
TDM_BUS_MODE	12	R/W	TDM Bus Mode (Applies only to SDT mode; must be cleared in UDT mode.) ‘0’ = Generic. ‘1’ = ST-BUS. (The clock is 4.096 MHz.)

Table 84 - TDM Control Register 1 (one per port)

Address: 6200 + p*10 (Hex)
Label: TDM1_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM_DATA_ FORMAT	14:13	R/W	TDM Data Mode. “00” = No cells generated from this port. “01” = UDT mode “10” = SDT mode. “11” = SDT mode with N>46. This mode should be used when any VC associated with this port has more than 46 channels.
TDM_LOW_ LATENCY_LPBK	15	R/W	Low latency loopback. ‘0’ = Normal operation. ‘1’ = Loopback data from DSTi to DSTo. **Note 1:** If this bit is set, data from DSTi is output on DSTo, regardless of the value of the TDM_REASS_PORT_CONTROL bit in TDM Control Register 3 (i.e., even if the port is apparently inactive, loopback data will be output on DSTo). **Note 2:** To use low-latency loopback, the clock edge used to sample the incoming TDM data (determined by TDM_CLK_POL in this register) must be opposite to the clock edge used to drive the outgoing TDM data (determined by TDM_REASS_CLK_POL, set at 6204h). **Note 3:** The delay through the device in low latency loopback mode is approximately 2 TDM clock cycles.

Table 84 - TDM Control Register 1 (one per port)

Address: 6202 + p*10 (Hex)
Label: TDM2_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM_SEGMEN_ BASE_ADD	8:0	R/W	Segmentation Circular Buffer Base Address. (Applies only to SDT mode.) Represents bits<19:11> of the SDT Segmentation Circular Buffer **word** address in external memory.
Reserved	12:9	R/O	Always reads “0000”.
TDM_SEGMEN_ PORT_CONTROL	13	R/W	Segmentation TDM Port Control. ‘0’ = Port is not active (data is not transferred from the TDM module to the rest of the MT90528). ‘1’ = Port is active.
TDM_SEGMEN_ INT_ENB	14	R/W	Segmentation Internal Enable Process. ‘0’ = Process is disabled. ‘1’ = Process that writes data/CAS to the TDM input buffer is enabled.
TDM_SEGMEN_ EXT_ENB	15	R/W	Segmentation External Enable Process. (Applies only to SDT mode.) ‘0’ = Process is disabled. ‘1’ = Process that transfers data from the input buffer to external memory is enabled.

Table 85 - TDM Control Register 2 (one per port)

Address: 6204 + p*10 (Hex)
Label: TDM3_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM_REASS_ BASE_ADD	4:0	R/W	SDT Reassembly Circular Buffer Base Address. (Applies only to SDT mode.) Represents bits<19:15> of the SDT Reassembly Circular Buffer **word** address in external memory.
Reserved	9:5	R/O	Always reads “00_000”.
REPLAY_ N_SILENCE	10	R/W	Play old data or silence byte on underrun. (Applies only to SDT mode.) ‘0’ = During a TDM underrun, the reassembly process outputs silence bytes (programmed in the MAINTDM1 register at 6000h) on DSTo. ‘1’ = During a TDM underrun, the reassembly process replays the reassembly circular buffer.
TDM_REASS_ CLK_POL	11	R/W	Reassembly TDM Output Clock Polarity. ‘0’ = TDM data is driven out on the falling edge of SToCLK or C4M_C2M ‘1’ = TDM data is driven out on the rising edge of SToCLK or C4M_C2M. In ST-BUS, this bit must be set to “0”
TDM_REASS_ LOS	12	R/W	Outgoing Loss of Signal. (Applies only to UDT mode.) CSTo/LOSo pin drives out the value programmed in this field.
TDM_REASS_ PORT_CONTROL	13	R/W	Reassembly TDM port control. ‘0’ = Port is not active (output data pins are held in high impedance). ‘1’ = Port is active.
TDM_REASS_ INT_ENB	14	R/W	Reassembly Internal Enable Process. ‘0’ = Process is disabled. ‘1’ = Process that transfers data/CAS from the TDM output buffer to the output pins is enabled.
TDM_REASS_ EXT_ENB	15	R/W	Reassembly External Enable Process. (Applies only to SDT mode.) ‘0’ = Process is disabled. ‘1’ = Process that transfers data/CAS from external memory to the TDM output buffer is enabled.

Table 86 - TDM Control Register 3 (one per port)

Address: 6206 + p*10 (Hex)
Label: TDM4_Pp (where p represents the port number)
Reset Value: 0040 (Hex)

Label	Bit Position	Type	Description
Reserved	0	R/O	Always reads ‘0’.
UDT_LOS_SE	1	R/W	UDT Loss of Signal (LOS) Service Enable. When this bit is set and UDT_LOS_STATUS is asserted, TDM_SRV is set in the Main Status Register at 0002h.
UDT_TDM_OUT_ BUF_ERROR_SE	2	R/W	UDT TDM Output Buffer Error Service Enable. When this bit is set and UDT_TDM_OUT_BUF_STATUS is asserted, TDM_SRV is set in the Main Status Register at 0002h.
SDT_TDM_OUT_ BUF_ERROR_SE	3	R/W	SDT TDM Output Buffer Error Service Enable. When this bit is set and SDT_TDM_OUT_BUF_STATUS is asserted, TDM_SRV is set in the Main Status Register at 0002h.

Table 87 - TDM Control Register 4 (one per port)

Address: 6206 + p*10 (Hex)
Label: TDM4_Pp (where p represents the port number)
Reset Value: 0040 (Hex)

Label	Bit Position	Type	Description
SDT_PERM_ UNDER_SE	4	R/W	SDT Permanent Underrun Service Enable. When this bit is set and SDT_PERM_UNDER_STATUS is asserted, TDM_SRV is set in the Main Status Register at 0002h.
SDT_SIMPLE_ UNDER_SE	5	R/W	SDT Simple Underrun Service Enable. When this bit is set and SDT_SIMPLE_UNDER_STATUS is asserted, TDM_SRV is set in the Main Status Register at 0002h.
UDT_LOS_ STATUS	6	R/O/L	UDT Loss of Signal (LOS) Status. This bit is set when a loss of signal is detected on CSTi/LOSi. Writing a ‘0’ to this bit clears it. This bit cannot be cleared until the TDM Control Register 1 is programmed.
UDT_TDM_OUT_ BUF_STATUS	7	R/O/L	UDT TDM Output Buffer Error Status. This bit is set when there is an error in the UDT TDM output buffer. Writing a ‘0’ to this bit clears it.
SDT_TDM_OUT_ BUF_STATUS	8	R/O/L	SDT TDM Output Buffer Error Status. This bit is set when there is an error in the SDT TDM output buffer. Writing a ‘0’ to this bit clears it.
SDT_PERM_ UNDER_STATUS	9	R/O/L	SDT Permanent Underrun Status. This bit is set when a permanent underrun service enable bit is set in the TDM SDT Reassembly Control Structure for the port and the corresponding permanent underrun condition occurs. Writing a ‘0’ to this bit clears it.
SDT_SIMPLE_ UNDER_STATUS	10	R/O/L	SDT Simple Underrun Status. This bit is set when a simple underrun service enable bit is set in the TDM SDT Reassembly Control Structure for the port and the corresponding simple underrun condition occurs. Writing a ‘0’ to this bit clears it.
SIMPLE_UNDER RUN_REPORT	15:11	R/O	SDT Simple Underrun Report. Indicates the TDM channel on which a “simple underrun” occurred last.

Table 87 - TDM Control Register 4 (one per port)

Address: 6208 + p*10 (Hex)
Label: TDM5_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
PERM_ UNDERRUN_ REPORT	15:0	R/O/L	Permanent Underrun Report. (Applies only to SDT mode.) This register represents bits<31:16> of the 32-bit permanent underrun report. Bit<31> corresponds to channel 31, bit<30> corresponds to channel 30, etc. When an underrun occurs on a certain channel, the corresponding bit is set high; the microprocessor can clear these bits by writing them to ‘0’.

Table 88 - TDM Control Register 5 (one per port)

Address: 620A + p*10 (Hex)
Label: TDM6_Pp (where p represents the port number)
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
PERM_ UNDERRUN_ REPORT	15:0	R/O/L	Permanent Underrun Report. (Applies only to SDT mode.) This register represents bits<15:0> of the 32-bit permanent underrun reports. Bit<15> corresponds to channel 15, bit<14> corresponds to channel 14, etc. When an underrun occurs on a certain channel, the corresponding bit is set high; the microprocessor can clear these bits by writing them to '0'.

Table 89 - TDM Control Register 6 (one per port)

6.2.10 External Memory Interface Module

Address: 7000 (Hex)
Label: MACR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
MCFG	2:0	R/W	Memory Configuration: "000" = No external memory "100" = Bank of 1 M words (max. 1 bank) "101" = Banks of 512 K words (max. 2 banks) "110" = Banks of 256 K words (max. 4 banks) "111" = Banks of 128 K words (max. 4 banks) All others = Reserved.
MTYP	3	R/W	Memory Type: '0' = Flow-through '1' = Pipelined.
PESE	4	R/W	Parity Error Service Enable. When this bit is set and either the LPPRTY_E bit or the HBPRTY_E bit is asserted at 7004h, the XMEMA_SRV bit is set in the Main Status Register at 0002h.
Reserved	15:5	R/O	Always reads "0000_0000_000".

Table 90 - Memory Arbiter Configuration Register

Address: 7004 (Hex) Label: PERS Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
LBPRTY_E	0	R/O/L	Low Byte Parity Error. If set, this bit indicates that a parity error has occurred in the lower 8 bits of the data word being read from external memory. A parity error may occur if a location in memory is read before being written. Writing ‘0’ to this bit clears it.
HBPRTY_E	1	R/O/L	High Byte Parity Error. If set, this bit indicates that a parity error has occurred in the high 8 bits of the data word being read from external memory. A parity error may occur if a location in memory is read before being written. Writing ‘0’ to this bit clears it.
Reserved	15:2	R/O	Always reads “0000_0000_0000_00”.

Table 91 - Parity Error Status Register

7.0 Electrical Specification

7.1 DC Characteristics

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage - 2.5 Volt Rail	V_{DD2}	V_{SS}	3.5	V
2	Supply Voltage - 3.3 Volt Rail	V_{DD3}	V_{SS}	4.5	V
3	Voltage on 3.3 V Input pins	V_{I3}	- 0.5	6	V
4	Voltage on 3.3 V Output pins	V_{O3}	- 0.5	4.6	V
5	Continuous current at digital inputs	I_I		±10	mA
6	Continuous current at digital outputs	I_O		± 24	mA
7	Storage Temperature	T_S	- 40	+125	°C

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed.
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated. Long-term exposure to absolute maximum ratings may affect device reliability, and exceeding the maximum ratings may cause permanent damage. The device should be operated under recommended operating conditions.

Recommended Operating Conditions

	Characteristics	Sym.	Min.	Typ.[a]	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	- 40	25	+ 85	°C	
2	Supply Voltage, 2.5 Volt Rail	V_{DD2}	2.37	2.5	2.63	V	
3	Supply Voltage, 3.3 Volt Rail	V_{DD3}	3.13	3.3	3.46	V	
4	Input Voltage, 3.3 V inputs	V_{I3}	- 0.5		5.5	V	

a. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

DC Characteristics

	Characteristics	Sym.	Min.	Typ.[a]	Max.	Units	Test Conditions [b]
1	Supply Current - 2.5 V supply	I_{DD2}		400	620	mA	66.0 MHz, UDT mode
2	Supply Current - 2.5 V supply	I_{DD2}		420	650	mA	66.0 MHz, SDT mode
3	Supply Current - 3.3 V supply	I_{DD3}		22	53	mA	66.0 MHz, UDT mode, Notes 1, 2
4	Supply Current - 3.3 V supply	I_{DD3}		46	95	mA	66.0 MHz, SDT mode, Notes 1, 3
5	Device Power Dissipation (2.5V and 3.3V supplies)	P_{DDU}		1.1	1.8	W	66.0 MHz, UDT mode, Notes 1, 2
6	Device Power Dissipation (2.5 V and 3.3 V supplies)	P_{DDS}		1.2	2.0	W	66.0 MHz, SDT mode, Notes 1, 3
7	Input High Voltage (3.3 V CMOS)	V_{IH3}	2.3		5.5	V	
8	Input Low Voltage (3.3 V CMOS)	V_{IL3}	-0.5		1.0	V	
9	Switching Threshold (3.3 V CMOS)	V_{TC3}	1.24	1.36	1.59	V	
10	Schmitt Trigger Positive Threshold	V_{t+}		1.57	1.72	V	

DC Characteristics

	Characteristics	Sym.	Min.	Typ.[a]	Max.	Units	Test Conditions [b]
11	Schmitt Trigger Negative Threshold	V_{t-}	0.825	1.18		V	
12	Input Leakage Current	I_I		± 0.01	± 1	µA	$V_{IN} = V_{DDx}$ or V_{ss}
	Inputs with pull-down resistors	I_{IH}	16	35	70	µA	$V_{IN} = V_{DD3}$
	Inputs with pull-up resistors	I_{IL}	-18	-35	- 70	µA	$V_{IN} = V_{ss}$
13	Input Pin Capacitance	C_I			10	pF	
14	Output Pin Capacitance	C_O			10	pF	
15	Output High Impedance Leakage	I_{OZ}		± 0.01	±1	µA	$V_O = V_{SS}$ or V_{DDx}
16	Output HIGH Voltage (3.3 V CMOS)	V_{OH3}	2.4			V	I_{OH} = rated current
17	Output LOW Voltage (3.3 V CMOS)	V_{OL3}			0.4	V	I_{OL} = rated current
18	3.3 V output HIGH current (4 mA buffer)	I_{OH3}	- 5.9	- 12.7		mA	V_{OH} = 2.4 V
19	3.3 V output LOW current (4 mA buffer)	I_{OL3}	4.1	6.9		mA	V_{OL} = 0.4 V
20	3.3 V output HIGH current (24 mA buffer)	I_{OH3}	- 24.1	- 50.5		mA	V_{OH} = 2.4 V
21	3.3 V output LOW current (24 mA buffer)	I_{OL3}	24.6	41.3		mA	V_{OL} = 0.4 V
22	Junction-to-Ambient Thermal Resistance	θ_{J-A}		19.4		°C/W	0 lfm air flow (natural convection airflow only)

a. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
b. T_{OP} = -40°C to 85°C; V_{DD2} = 2.5 V ± 5%; V_{DD3} = 3.3 V ± 5%
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

Note 1: Supply current and device power is for 28 ports in E1 mode. Typical values are with V_{DD3} and V_{DD2} at nominal, with all output pins loaded with half the rated capacitance (as given in the AC Characteristics section) and with the two UTOPIA clocks as inputs. Maximum values are with V_{DD3} and V_{DD2} at + 5% (2.625 V and 3.465 V), with all output pins loaded with the full rated capacitance, and the two UTOPIA clocks as outputs.
Note 2: UDT mode supply current and device power includes 1800 cells of CPU/OAM traffic in both directions, and no discards of non-AAL1 cells, giving Look-Up Table reads of 1 800 reads/second.
Note 3: SDT mode supply current and device power includes 1800 cells of CPU/OAM traffic in both directions, and sufficient discards of non-AAL1 cells to bring Look-Up Table reads to 1 000 000 reads/second.

7.2 AC Characteristics

MCLK - Master Clock Input Parameters

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
MCLK Frequency	t_{MF}		66.0	66.0	MHz	30 ppm clock required for proper operation of the TDM PLLs
MCLK Period	t_{MP}		15.2		ns	
MCLK Pulse Width (HIGH / LOW)	$t_{MH/L}$	6.8	7.6		ns	

PHY_CLK - Clock Input Parameters

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
PHY_CLK Frequency	t_{PF}		19.44 8		MHz kHz	PHY_CLK frequency determined by 8_KHZ_SEL bit in CMCR register
PHY_CLK Period 19.44 MHz 8 kHz	t_{PP}		 51.44 125		 ns µs	
PHY_CLK Pulse Width (HIGH / LOW) 19.44 MHz 8 kHz	$t_{PH/L}$	 20 0.1	 25.72 62.5		 ns µs	

7.2.1 CPU Interface

Intel Microprocessor Interface Timing - Read Cycle Parameters

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Address Setup - (AEM and CPU_ADD[20:1] VALID) to ($\overline{CS}$ and $\overline{RD}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{RD}$ de-asserted) to (AEM and CPU_ADD[20:1] INVALID)	t_{ADDH}	0			ns	
RDY Low - $\overline{CS}$ asserted to RDY driven low	t_{RRDYL}	0		10	ns	C_L = 75 pF
RDY Delay - ($\overline{CS}$ and $\overline{RD}$ asserted) to RDY asserted Register access Memory access	t_{RACC}	 197 213	 228	 243 2021	 ns ns	C_L = 100 pF 13 MCLK < t_{RACC} < 16 MCLK 14 MCLK < t_{RACC} < 133 MCLK
RDY High-Impedance - $\overline{CS}$ de-asserted to RDY high-impedance	t_{RRDYZ}	0		10	ns	C_L = 75 pF
Data Output Setup - CPU_DATA[15:0] VALID to RDY asserted	t_{DS}		16		ns	C_L = 75 pF ~ 1 MCLK cycle
Data Output Hold - ($\overline{CS}$ or $\overline{RD}$ de-asserted) to CPU_DATA[15:0] INVALID	t_{DH}	0			ns	C_L = 75 pF

Note 1: MCLK = 66 MHz (15.2 ns)
Note 2: Both $\overline{CS}$ and $\overline{RD}$ must be asserted for a read cycle to occur. A read cycle is completed when either $\overline{CS}$ or $\overline{RD}$ is de-asserted.
Note 3: There should be a minimum of 3 MCLK periods between CPU accesses, to allow the MT90528 to recognize the accesses as separate (i.e., $\overline{CS}$ must be de-asserted for 3 MCLK cycles between CPU accesses).

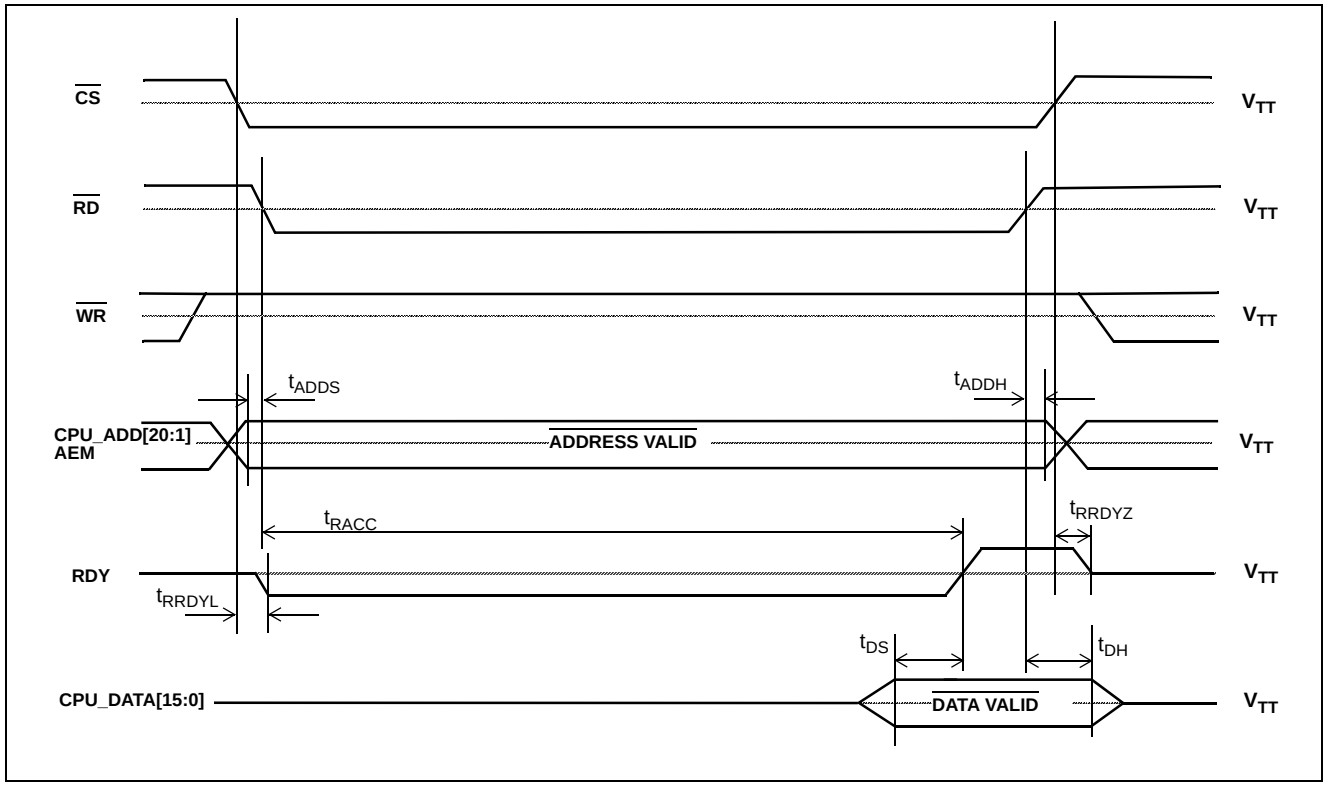


Figure 47 - Intel CPU Interface Timing - Read Access

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Address Setup - (AEM and CPU_ADD[20:1] VALID) to ($\overline{CS}$ and $\overline{WR}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{WR}$ de-asserted) to (AEM and CPU_ADD[20:1] INVALID)	t_{ADDH}	0			ns	
RDY Low - $\overline{CS}$ asserted to RDY driven low	t_{WRDYL}	0		10	ns	C_L = 75 pF
RDY Delay - ($\overline{CS}$ and $\overline{WR}$ asserted) to RDY asserted	t_{WACC}					C_L = 75 pF
Register access		167	197	213	ns	11 MCLK < t_{WACC} < 14 MCLK
Memory access		182		2021	ns	12 MCLK < t_{WACC} < 133 MCLK
RDY High-Impedance - $\overline{CS}$ de-asserted to RDY high-impedance	t_{WRDYZ}	0		10	ns	C_L = 75 pF
Write Cycle Hold Time - RDY asserted to ($\overline{CS}$ or $\overline{WR}$ de-asserted)	t_{WRH}	0			ns	
Data Input Setup - CPU_DATA[15:0] VALID to ($\overline{CS}$ and $\overline{WR}$ asserted)	t_{DS}	0			ns	
Data Input Hold - ($\overline{CS}$ or $\overline{WR}$ de-asserted) to CPU_DATA[15:0] INVALID	t_{DH}	0			ns	

Note 1: MCLK = 66 MHz (15.2 ns)
Note 2: Both $\overline{CS}$ and $\overline{WR}$ must be asserted for a write cycle to occur. A write cycle is completed when either $\overline{CS}$ or $\overline{WR}$ is de-asserted.
Note 3: There should be a minimum of 3 MCLK periods between CPU accesses, to allow the MT90528 to recognize the accesses as separate (i.e., $\overline{CS}$ must be de-asserted for 3 MCLK cycles between CPU accesses).

Table 92 - Intel Microprocessor Interface Timing - Write Cycle Parameters

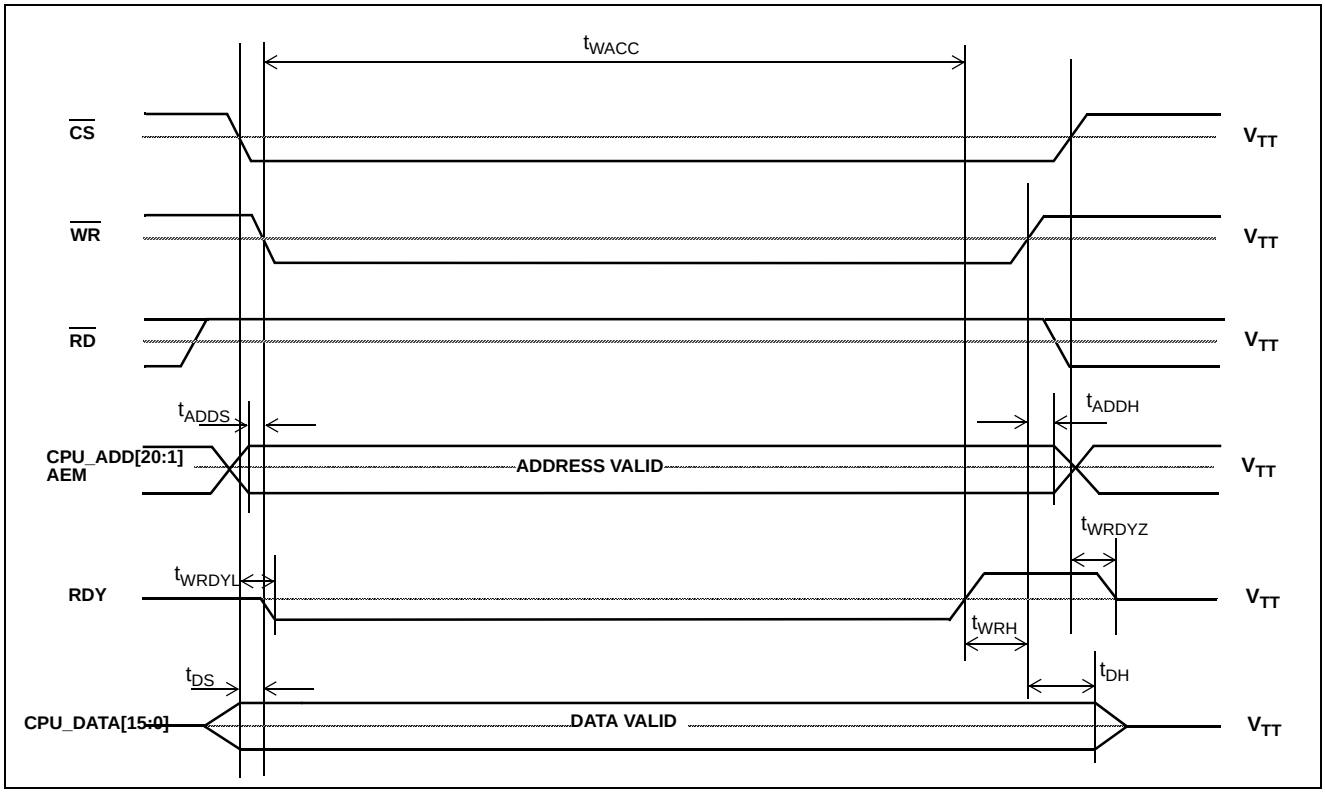


Figure 48 - Intel CPU Interface Timing - Write Access

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Address Setup - (R/$\overline{W}$, AEM and CPU_ADD[20:1] VALID) to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to (AEM, CPU_ADD[20:1] and R/$\overline{W}$ INVALID)	t_{ADDH}	0			ns	
$\overline{DTACK}$ High - $\overline{CS}$ asserted to $\overline{DTACK}$ driven high	t_{RDTKH}	0		10	ns	C_L = 75 pF
$\overline{DTACK}$ Delay - ($\overline{CS}$ and $\overline{DS}$ asserted) to $\overline{DTACK}$ asserted Register access Memory access	t_{RACC}	 197 213	 228	 243 2021	ns	C_L = 75 pF 13 MCLK < t_{RACC} < 16 MCLK 14 MCLK < t_{RACC} < 133 MCLK
$\overline{DTACK}$ High-Impedance - $\overline{CS}$ de-asserted to $\overline{DTACK}$ high-impedance	t_{RDTKZ}	0		10	ns	C_L = 75 pF
Data Output Setup - CPU_DATA[15:0] VALID to $\overline{DTACK}$ asserted	t_{DS}		16		ns	C_L = 75 pF ~ 1 MCLK cycle
Data Output Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to CPU_DATA[15:0] INVALID	t_{DH}	0			ns	C_L = 75 pF

Note 1: MCLK = 66 MHz (15.2 ns)
Note 2: Both $\overline{CS}$ and $\overline{DS}$ must be asserted for a read cycle to occur. A read cycle is completed when either $\overline{CS}$ or $\overline{DS}$ is de-asserted.
Note 3: There should be a minimum of 3 MCLK periods between CPU accesses, to allow the MT90528 to recognize the accesses as separate (i.e., $\overline{CS}$ must be de-asserted for 3 MCLK cycles between CPU accesses).

Table 93 - Motorola Microprocessor Interface Timing - Read Cycle Parameters

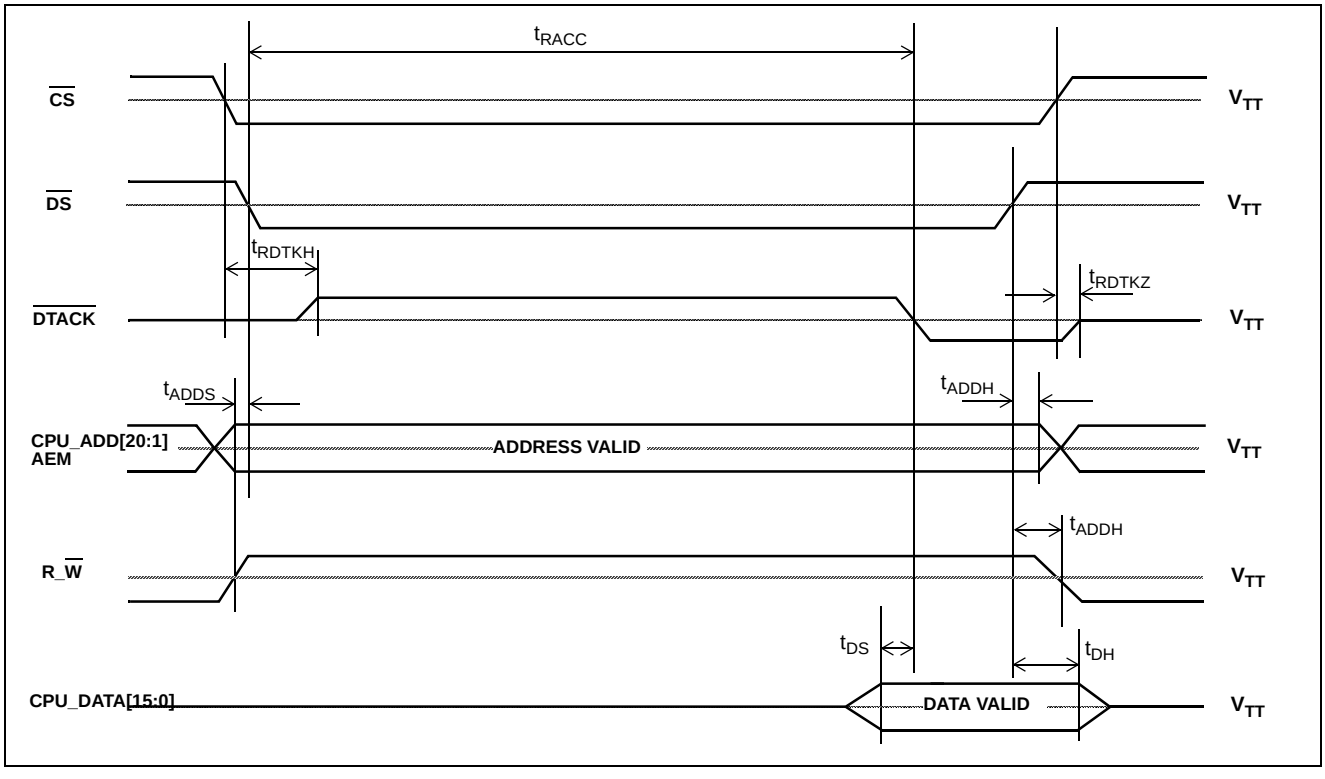


Figure 49 - Motorola CPU Interface Timing - Read Access

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Address Setup - (R/$\overline{W}$, AEM and CPU_ADD[20:1] VALID) to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to (AEM, CPU_ADD[20:1] and R/$\overline{W}$ INVALID)	t_{ADDH}	0			ns	
$\overline{DTACK}$ High - $\overline{CS}$ asserted to $\overline{DTACK}$ driven high	t_{WDTKH}	0		10	ns	C_L = 75 pF
$\overline{DTACK}$ Delay - ($\overline{CS}$ and $\overline{DS}$ asserted) to DTACK asserted Register access Memory access	t_{WACC}	 167 182	 197	 213 2021	 ns ns	C_L = 75 pF 11 MCLK < t_{WACC} < 14 MCLK 12 MCLK < t_{WACC} < 133 MCLK
$\overline{DTACK}$ High-Impedance - $\overline{CS}$ de-asserted to DTACK high-impedance	t_{WDTKZ}	0		10	ns	C_L = 75 pF
Data Input Setup - CPU_DATA[15:0] VALID to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{DS}	0			ns	
Data Input Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to CPU_DATA[15:0] INVALID	t_{DH}	0			ns	

Note 1: MCLK = 66 MHz (15.2 ns)
Note 2: Both $\overline{CS}$ and $\overline{DS}$ must be asserted for a write cycle to occur. A write cycle is completed when either $\overline{CS}$ or $\overline{DS}$ is de-asserted.
Note 3: There should be a minimum of 3 MCLK periods between CPU accesses ($\overline{CS}$ de-asserted), to allow the MT90528 to recognize the accesses as separate (i.e., $\overline{CS}$ must be de-asserted for 3 MCLK cycles between CPU accesses).

Table 94 - Motorola Microprocessor Interface Timing - Write Cycle Parameters

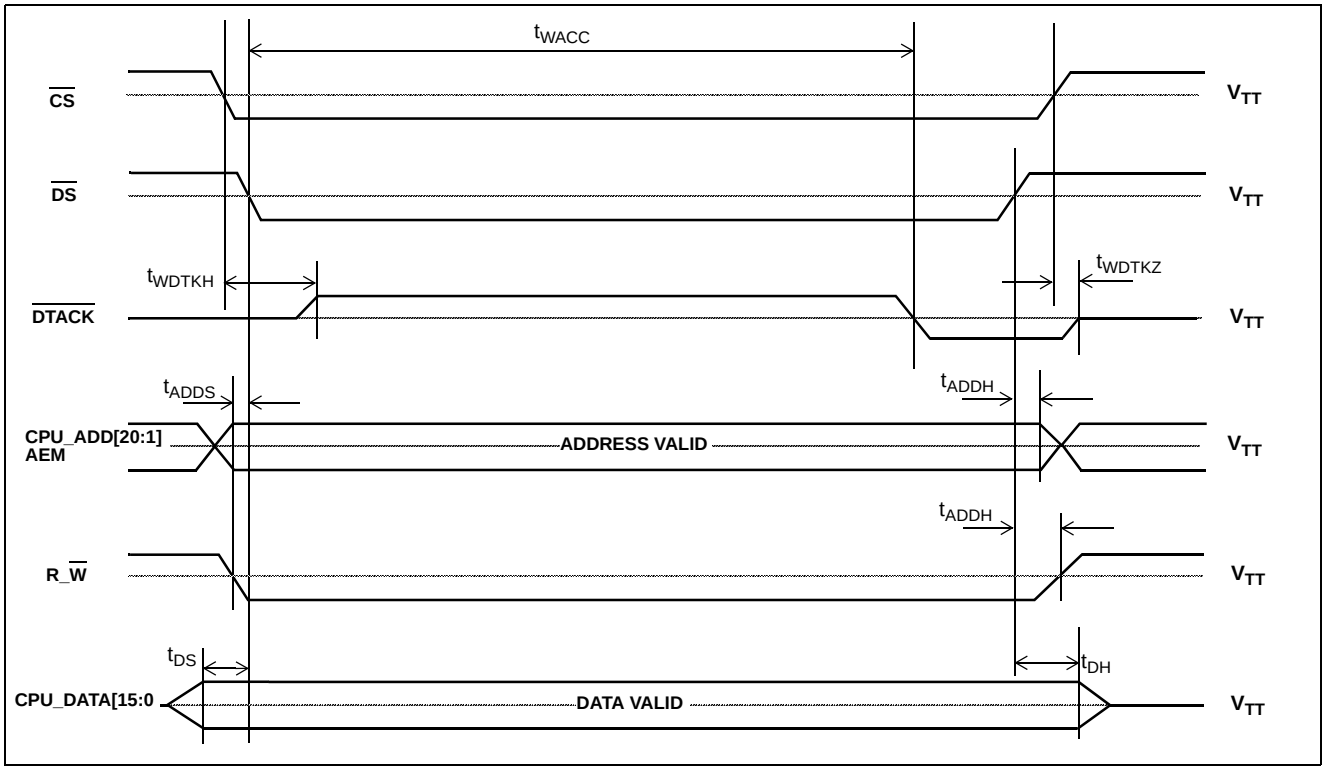


Figure 50 - Motorola CPU Interface Timing - Write Access

7.2.2 External Memory Interface

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Data Input Setup - MEM_DATA[17:0] VALID to MCLK rising	t_{DIS}	5			ns	C_L = 35 pF
Data Input Hold Time - MCLK rising to MEM_DATA[17:0] INVALID	t_{DIH}	2			ns	C_L = 35 pF
Clock to Change - MCLK rising to (MEM_ADD[19:0], MEM_CS_X and MEM_WR) change	t_{OC}	1			ns	C_L = 35 pF
Output Delay - MCLK rising to (MEM_ADD[19:0] VALID and (MEM_CS_X and MEM_WR) asserted)	t_{OD}			12.5	ns	C_L = 35 pF

Table 95 - External Memory Interface Timing - Read Cycle Parameters

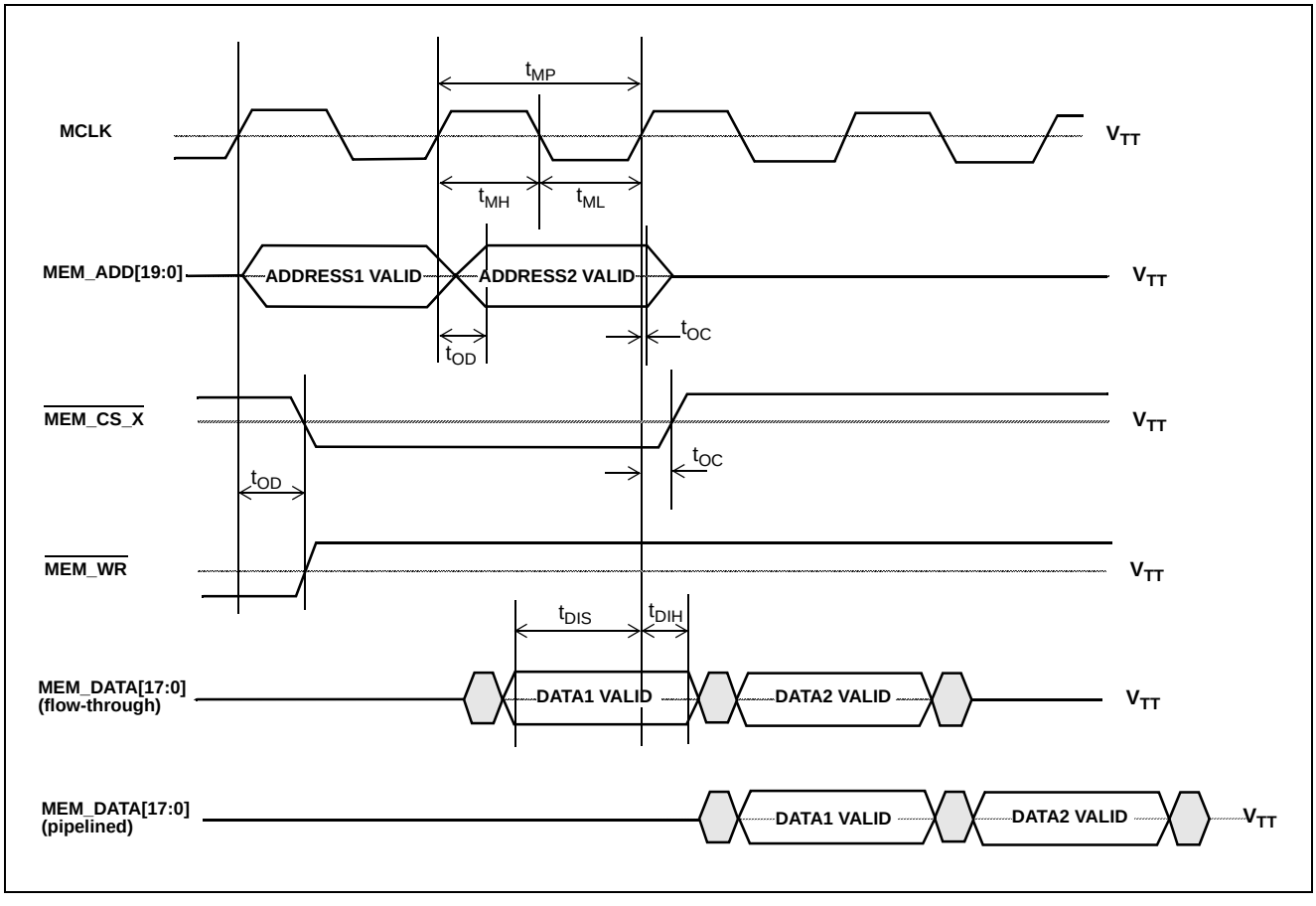


Figure 51 - External Memory Interface Timing - Read Cycle

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Output Delay - MCLK rising to (MEM_ADD[19:0], MEM_DATA[17:0]) VALID and (MEM_CS_X and MEM_WR) asserted	t_{OD}			12.5	ns	C_L = 35 pF
Output Hold Time - MCLK rising MEM_DATA[17:0] INVALID	t_{OH}	1			ns	C_L = 35 pF
High-Z to Drive Time - MCLK rising to MEM_DATA[17:0] driven	t_{ZD}	3			ns	C_L = 35 pF
Clock to Change - MCLK rising to (MEM_ADD[19:0], MEM_CS_X and MEM_WR) change	t_{OC}	1			ns	C_L = 35 pF
Drive to High-Z Time - MCLK rising to MEM_DATA[17:0] High-Z	t_{DZ}	1		6.5	ns	C_L = 35 pF

Table 96 - External Memory Interface Timing - Write Cycle Parameters

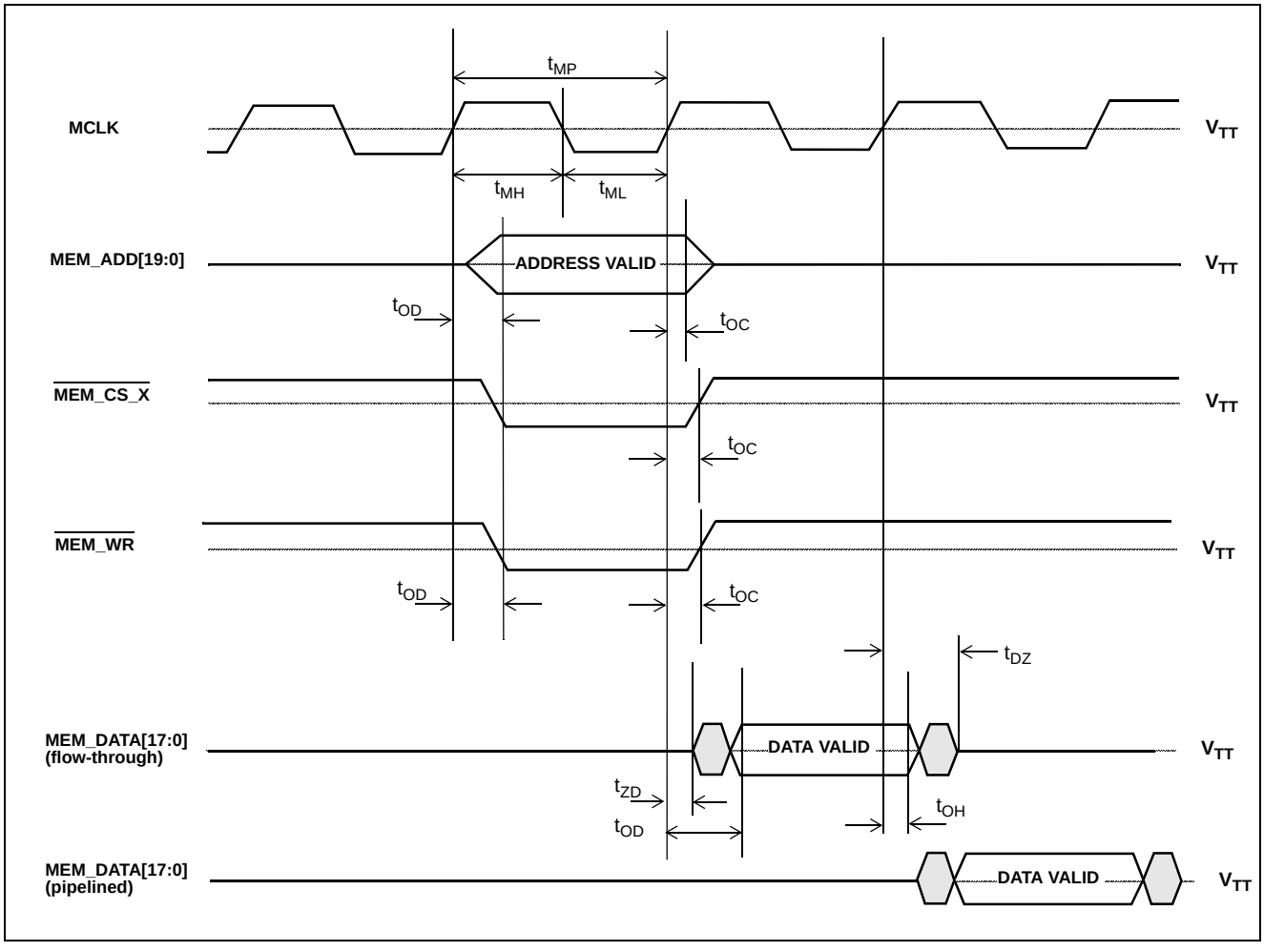
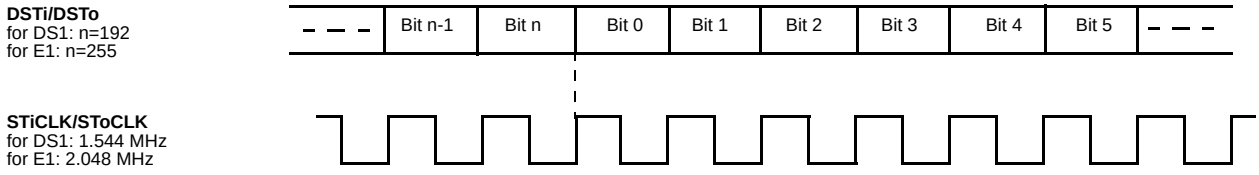


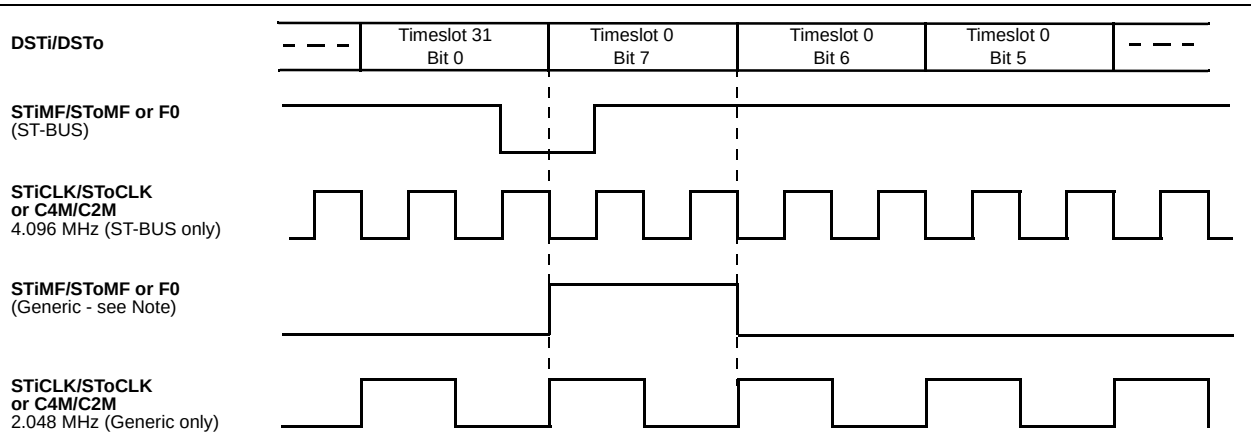
Figure 52 - External Memory Interface Timing - Write Cycle

7.2.3 TDM Interface



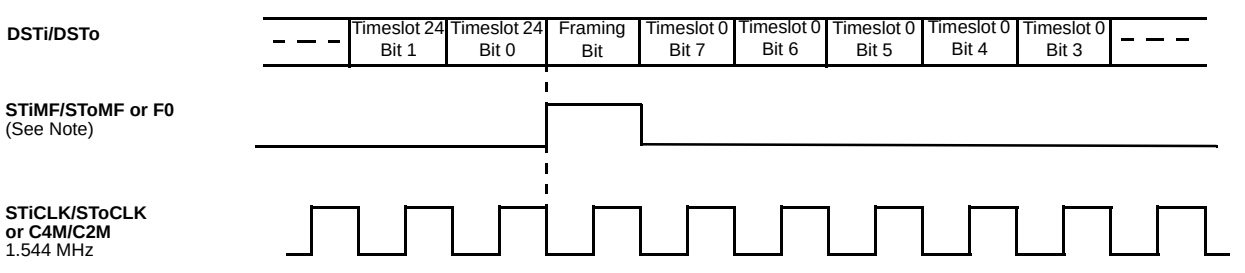
Note: Clock polarity is programmable. Data can be sampled/driven out either on the falling edge or the rising edge of the clock.

Figure 53 - Nominal UDT Mode Timing Diagram - DS1 (1.544 Mbps) and E1 (2.048 Mbps)



Note: In Generic format, both clock polarity and frame pulse polarity are programmable. Data can be sampled/driven out either on the falling edge or the rising edge of the clock. The frame pulse can have either positive or negative polarity.

Figure 54 - Nominal SDT Mode Timing Diagram - Generic and ST-BUS DS1 or E1 (2.048 Mbps)



Note: Due to the use of Generic mode, clock and frame pulse polarity are programmable. Data can be sampled/driven out either on the falling edge or the rising edge of the clock. The frame pulse can have either positive or negative polarity.

Figure 55 - Nominal SDT Mode Timing Diagram - Generic DS1 (1.544 Mbps)

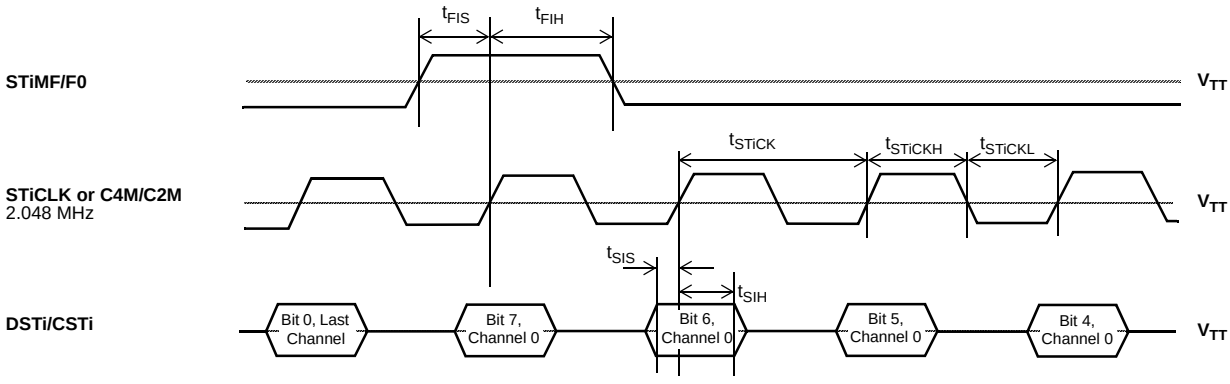
Table 97 and Table 98 refer to input clock parameters which are displayed in Figure 56 and Figure 57, which follow the tables.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
STiCLK/C4M/C2M Clock Period	t_{STiCK}					
1.544 Mbps bus (1.544 MHz clock)			648		ns	
1.544 or 2.048 Mbps bus (2.048 MHz clock)			488		ns	
2.048 Mbps bus (4.096 MHz clock)			244		ns	
STiCLK/C4M/C2M Pulse Width (HIGH / LOW)	$t_{STiCKH/L}$					
1.544 Mbps bus (1.544 MHz clock)			324		ns	
1.544 or 2.048 Mbps bus (2.048 MHz clock)			244		ns	
2.048 Mbps bus (4.096 MHz clock)			122		ns	
Frame Pulse Width	t_{FPW}					
1.544 Mbps (Generic)		100	648	900	ns	
2.048 Mbps (Generic)		100	488	600	ns	
2.048 Mbps (ST-BUS)		100	244	300	ns	
Frame Pulse Setup Time	t_{FIS}					
STiMF/F0 valid to STiCLK/C4M/C2M rising		15			ns	
STiMF/F0 valid to STiCLK/C4M/C2M falling		15			ns	
Frame Pulse Hold Time	t_{FIH}					
STiCLK/C4M/C2M rising to STiMF/F0 invalid		10			ns	
STiCLK/C4M/C2M falling to STiMF/F0 invalid		10			ns	

Table 97 - TDM Bus Input Clock Parameters

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Data Setup Time - DSTi/CSTi VALID to STiCLK/C4M/C2M falling Sampling on falling edge	t_{SIS}	15			ns	
Data Hold Time - STiCLK/C4M/C2M falling to DSTi/CSTi INVALID Sampling on falling edge	t_{SIH}	10			ns	
Data Setup Time - DSTi/CSTi VALID to STiCLK/C4M/C2M rising Sampling on rising edge	t_{SIS}	15			ns	
Data Hold Time - STiCLK/C4M/C2M rising to DSTi/CSTi INVALID Sampling on rising edge	t_{SIH}	10			ns	

Table 98 - TDM Bus Input Data Parameters



Note: In Generic format, both clock polarity and frame pulse polarity are programmable. Data can be sampled either on the falling edge or the rising edge of the clock. The frame pulse can have either positive or negative polarity.

Figure 56 - TDM Bus Inputs - Generic Bus Sampling

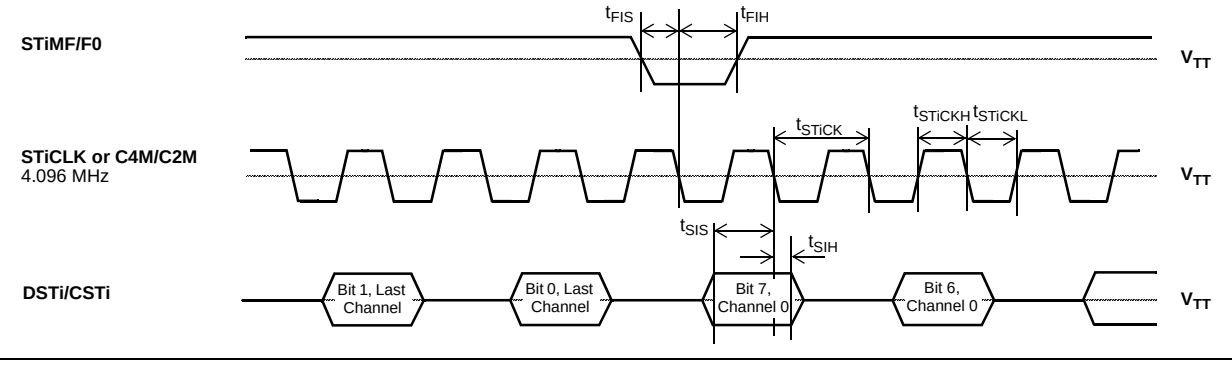


Figure 57 - TDM Bus Inputs - ST-BUS Sampling

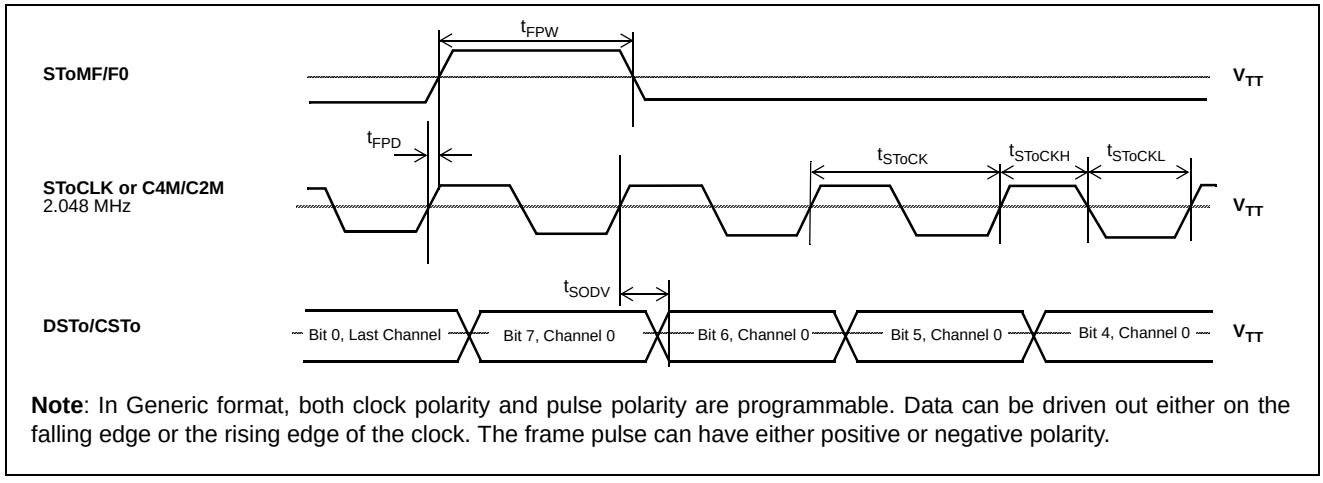
Table 99 and Table 100 refer to output clock parameters which are displayed below in Figure 58, Figure 59, and Figure 60.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
SToCLK/C4M/C2M Clock Period	t_{SToCK}					
1.544 Mbps bus (1.544 MHz clock)			648		ns	
1.544 or 2.048 Mbps bus (2.048 MHz clock)			488		ns	
2.048 Mbps bus (4.096 MHz clock)			244		ns	
SToCLK/C4M/C2M Pulse Width (HIGH / LOW)	$t_{SToCKH/L}$					
1.544 Mbps bus (1.544 MHz clock)			324		ns	
1.544 or 2.048 Mbps bus (2.048 MHz clock)			244		ns	
2.048 Mbps bus (4.096 MHz clock)			122		ns	
Frame Pulse Width	t_{FPW}					
1.544 Mbps (Generic)			648		ns	
2.048 Mbps (Generic)			488		ns	
2.048 Mbps (ST-BUS)			244		ns	
Frame Pulse Delay	t_{FPD}					
SToCLK rising to SToMF change (Generic)		0		40	ns	C_L = 30 pF
SToCLK falling to SToMF change (ST-BUS or Generic)		0		40	ns	C_L = 30 pF
C4M/C2M rising to F0 change (Generic)		4		40	ns	C_L = 200 pF
C4M/C2M falling to F0 change (ST-BUS or Generic)		4		40	ns	C_L = 200 pF

Table 99 - TDM Bus Output Clock Parameters

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Data Delay - Clock to Data Change	t_{SODX}					
SToCLK/C4M/C2M rising to DSTo or CSTo change (Generic)		5			ns	C_L = 30 pF
SToCLK/C4M/C2M falling to DSTo or CSTo change (ST-BUS or Generic)		5			ns	C_L = 30 pF
Data Delay - Clock to Data Valid	t_{SODV}					
SToCLK/C4M/C2M rising to DSTo or CSTo valid (Generic)				40	ns	C_L = 30 pF
SToCLK/C4M/C2M falling to DSTo or CSTo valid (ST-BUS or Generic)				40	ns	C_L = 30 pF
Drive to High-Z	t_{SODZ}					
SToCLK/C4M/C2M rising to DSTo or CSTo HIGH-Z (Generic)		5		10	ns	C_L = 30 pF
SToCLK/C4M/C2M falling to DSTo or CSTo HIGH-Z (ST-BUS or Generic)		5		10	ns	C_L = 30 pF
High-Z to Drive	t_{SOZX}					
SToCLK/C4M/C2M rising and DSTo or CSTo HIGH-Z to DSTo or CSTo change (Generic)		5		40	ns	C_L = 30 pF
SToCLK/C4M/C2M falling and DSTo or CSTo HIGH-Z to DSTo or CSTo change (ST-BUS or Generic)		5		40	ns	C_L = 30 pF

Table 100 - TDM Bus Data Output Parameters



Note: In Generic format, both clock polarity and pulse polarity are programmable. Data can be driven out either on the falling edge or the rising edge of the clock. The frame pulse can have either positive or negative polarity.

Figure 58 - TDM Bus Output Clocking Parameters - Generic

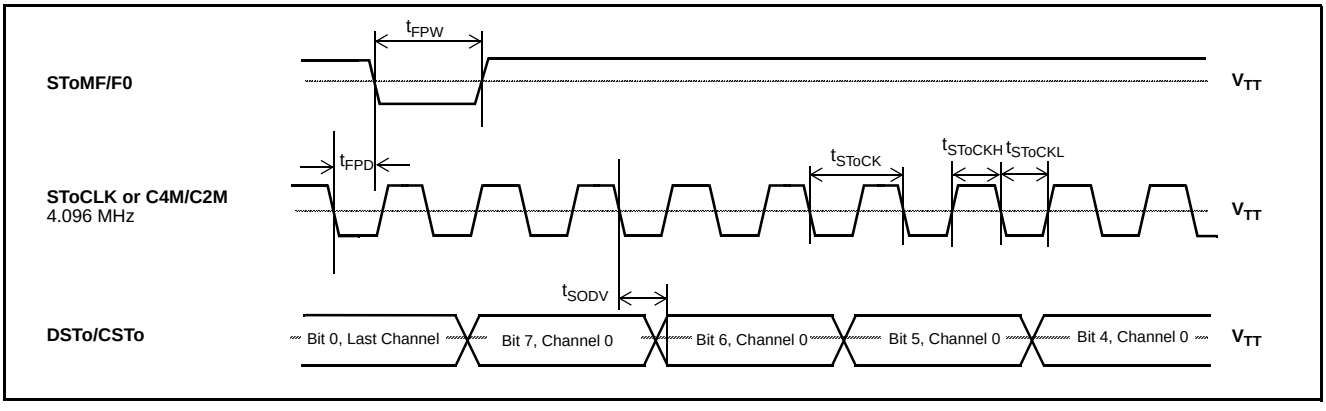


Figure 59 - TDM Bus Output Clocking Parameters - ST-BUS

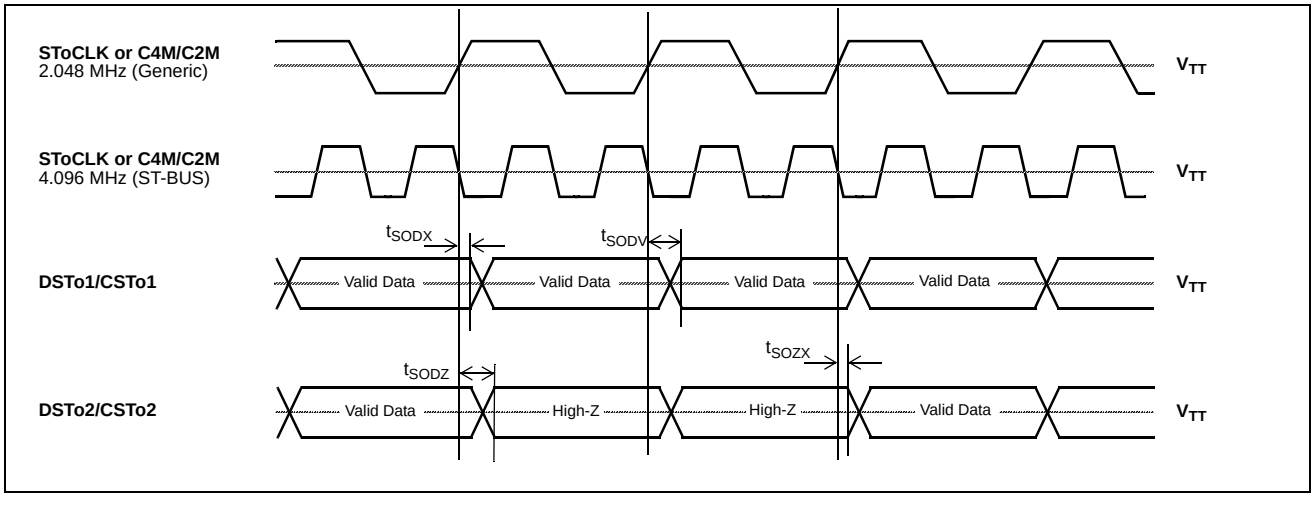


Figure 60 - TDM Bus Outputs - Serial Output Timing

7.2.3.1 UTOPIA Interface

7.2.3.2 UTOPIA Level 1

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
UTO_IN_CLK Period	t_{URX1P}	19.23			ns	UTO_IN_CLK = 52 MHz
UTO_IN_CLK Pulse Width (HIGH / LOW)	$t_{URX1H/L}$	7.7	$t_{URX1P}/2$		ns	
Input Setup Time - (UTO_IN_CLAVATM_ENBPHY, UTO_IN_SOC asserted and UTO_IN_DATA[7:0] VALID) to UTO_IN_CLK rising	t_{URXIS}	4			ns	
Input Hold Time - UTO_IN_CLK rising to (UTO_IN_DATA[7:0] INVALID and UTO_IN_SOC and UTO_IN_CLAVATM_ENBPHY de-asserted)	t_{URXIH}	1			ns	
Output Delay - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY asserted	t_{URXD}			13.8	ns	C_L=20 pF; UTO_IN_CLK ≤ 52 MHz
Output Hold Time - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY de-asserted	t_{URXH}	1			ns	C_L=20 pF; UTO_IN_CLK ≤ 52 MHz
Note: The MT90528 operates with the UTOPIA cell-level handshake.						

Table 101 - UTOPIA Level 1 Interface Timing - ATM mode - Incoming Data (UTOPIA RX Bus)

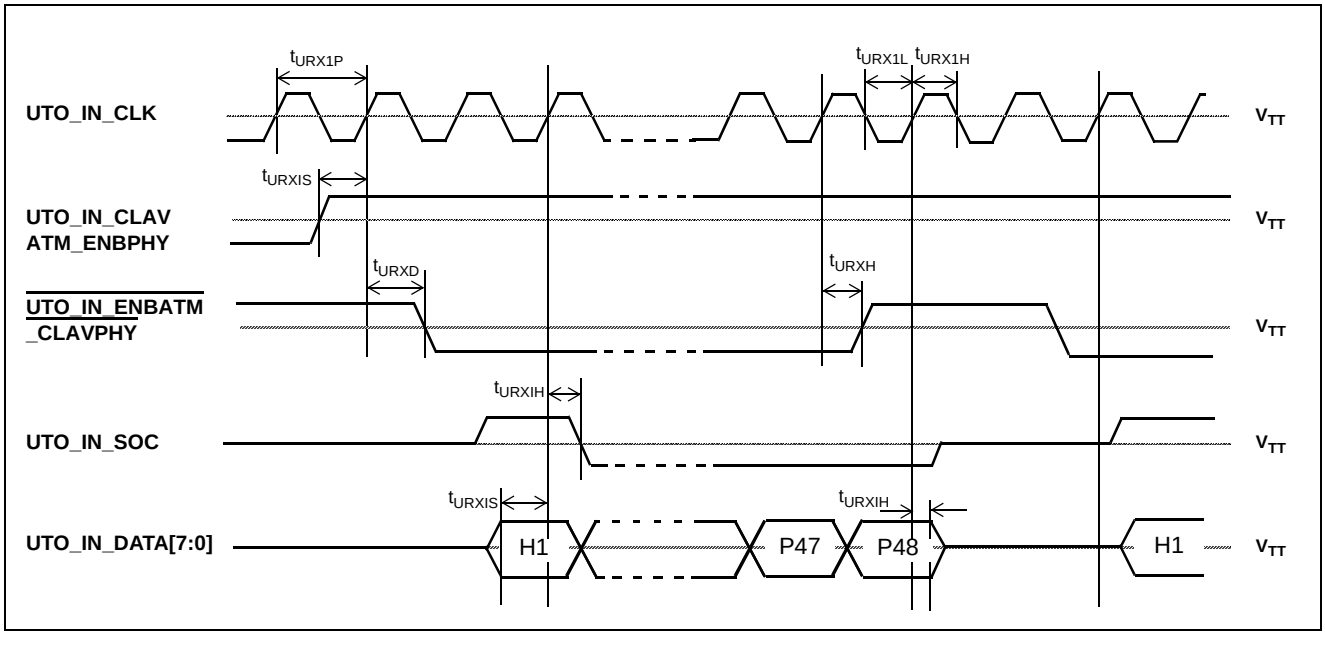


Figure 61 - UTOPIA Level 1 Interface Timing - ATM Mode - Incoming Data (UTOPIA RX Bus)

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
UTO_OUT_CLK Period	t_{UTX1P}	19.23			ns	UTO_OUT_CLK = 52 MHz
UTO_OUT_CLK Pulse Width (HIGH / LOW)	$t_{UTX1H/L}$	7.7	$t_{UTX1P}/2$		s	
Input Setup Time - UTO_OUT_CLAVATM_ENBPHY VALID to UTO_OUT_CLK rising	t_{UTXIS}	4			ns	
Input Hold Time - UTO_OUT_CLK rising to UTO_OUT_CLAVATM_ENBPHY de-asserted	t_{UTXIH}	1			ns	
Output Delay - UTO_OUT_CLK rising to (UTO_OUT_DATA[7:0] VALID and UTO_OUT_ENBATM_CLAVPHY and UTO_OUT_SOC asserted)	t_{UTXD}			13.8	ns	C_L = 20 pF; UTO_OUT_CLK ≤ 52 MHz
Output Hold Time - UTO_OUT_CLK rising to (UTO_OUT_DATA[7:0] INVALID and UTO_OUT_ENBATM_CLAVPHY and UTO_OUT_SOC de-asserted)	t_{UTXH}	1			ns	C_L = 20 pF; UTO_OUT_CLK ≤ 52 MHz

Table 102 - UTOPIA Level 1 Interface Timing - ATM mode - Outgoing Data (UTOPIA TX Bus)

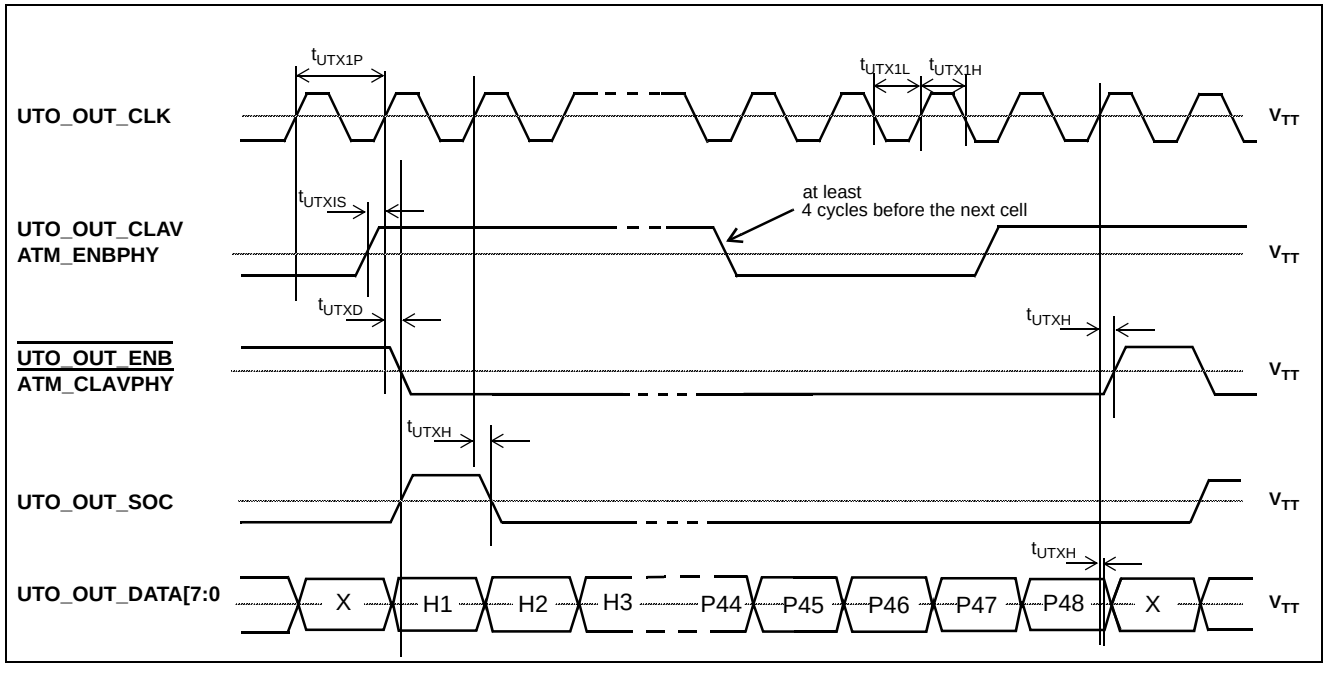


Figure 62 - UTOPIA Level 1 Interface Timing - ATM Mode - Outgoing Data (UTOPIA TX Bus)

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
UTO_IN_CLK Period	t_{UTX1P}	19.23			ns	UTO_IN_CLK = 52 MHz
UTO_IN_CLK Pulse Width (HIGH / LOW)	$t_{UTX1H/L}$	7.7	$t_{UTX1P}/2$		ns	
Input Setup Time - ($\overline{\text{UTO_IN_CLAVATM_ENBPHY}}$, UTO_IN_SOC asserted and UTO_IN_DATA[7:0] VALID) to UTO_IN_CLK rising	t_{UTXIS}	4			ns	
Input Hold Time - UTO_IN_CLK rising to (UTO_IN_DATA[7:0] INVALID and $\overline{\text{UTO_IN_CLAVATM_ENBPHY}}$ de-asserted)	t_{UTXIH}	1			ns	
Output Delay - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY asserted	t_{UTXD}			13.8	ns	C_L=20 pF; UTO_IN_CLK ≤ 52 MHz
Output Hold Time - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY de-asserted	t_{UTXH}	1			ns	C_L=20 pF; UTO_IN_CLK ≤ 52 MHz

Table 103 - UTOPIA Level 1 Interface Timing - PHY mode - Incoming Data (UTOPIA TX Bus)

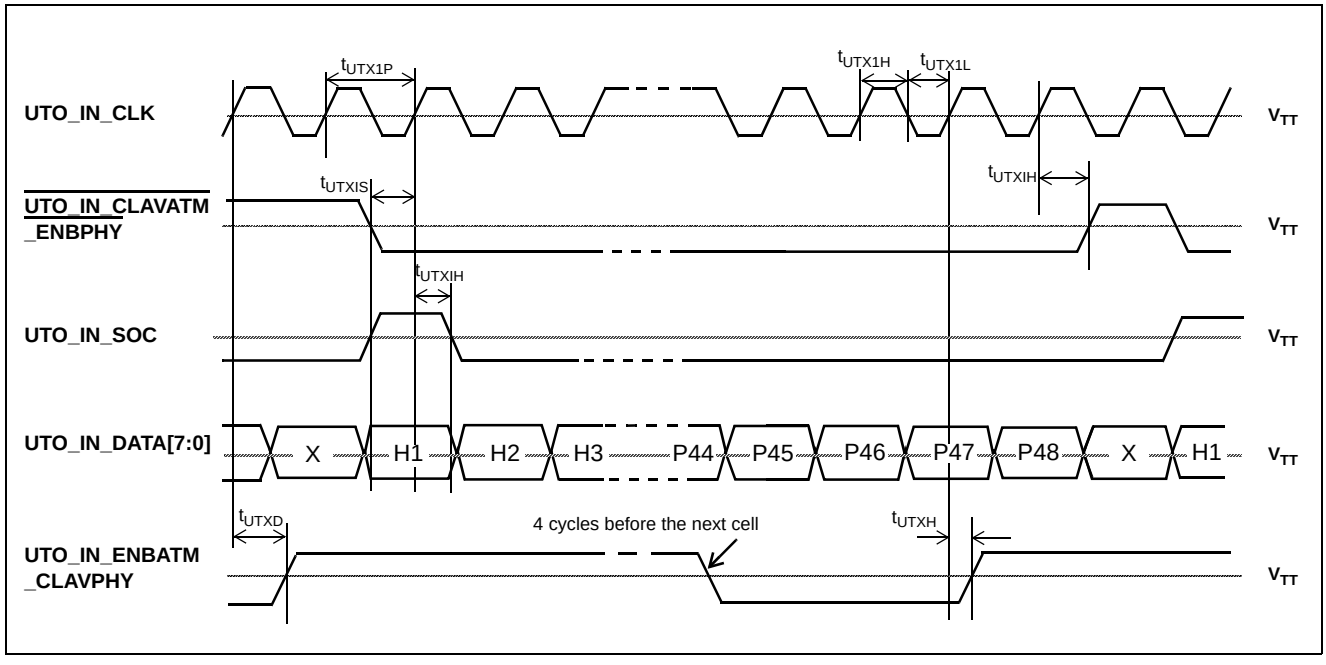


Figure 63 - UTOPIA Level 1 Interface Timing - PHY Mode - Incoming Data (UTOPIA TX Bus)

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
UTO_OUT_CLK Period	t_{URX1P}	19.23			ns	UTO_OUT_CLK = 52 MHz
UTO_OUT_CLK Pulse Width (HIGH / LOW)	$t_{URX1H/L}$	7.7	$t_{URX1P}/2$		ns	
Input Setup Time - UTO_OUT_CLAVATM_ENBPHY asserted to UTO_OUT_CLK rising	t_{URXIS}	4			ns	
Input Hold Time - UTO_OUT_CLK rising to UTO_OUT_CLAVATM_ENBPHY de-asserted	t_{URXIH}	1			ns	
Output Delay - UTO_OUT_CLK rising to (UTO_OUT_DATA[7:0] VALID and UTO_OUT_ENBATM_CLAVPHY and UTO_OUT_SOC asserted)	t_{URXD}			13.8	ns	C_L = 20 pF; UTO_OUT_CLK ≤ 52 MHz
Output Hold Time - UTO_OUT_CLK rising to (UTO_OUT_DATA[7:0] INVALID and UTO_OUT_ENBATM_CLAVPHY and UTO_OUT_SOC de-asserted)	t_{URXH}	1			ns	C_L = 20 pF; UTO_OUT_CLK ≤ 52 MHz

Table 104 - UTOPIA Level 1 Interface Timing - PHY mode - Outgoing Data (UTOPIA RX Bus)

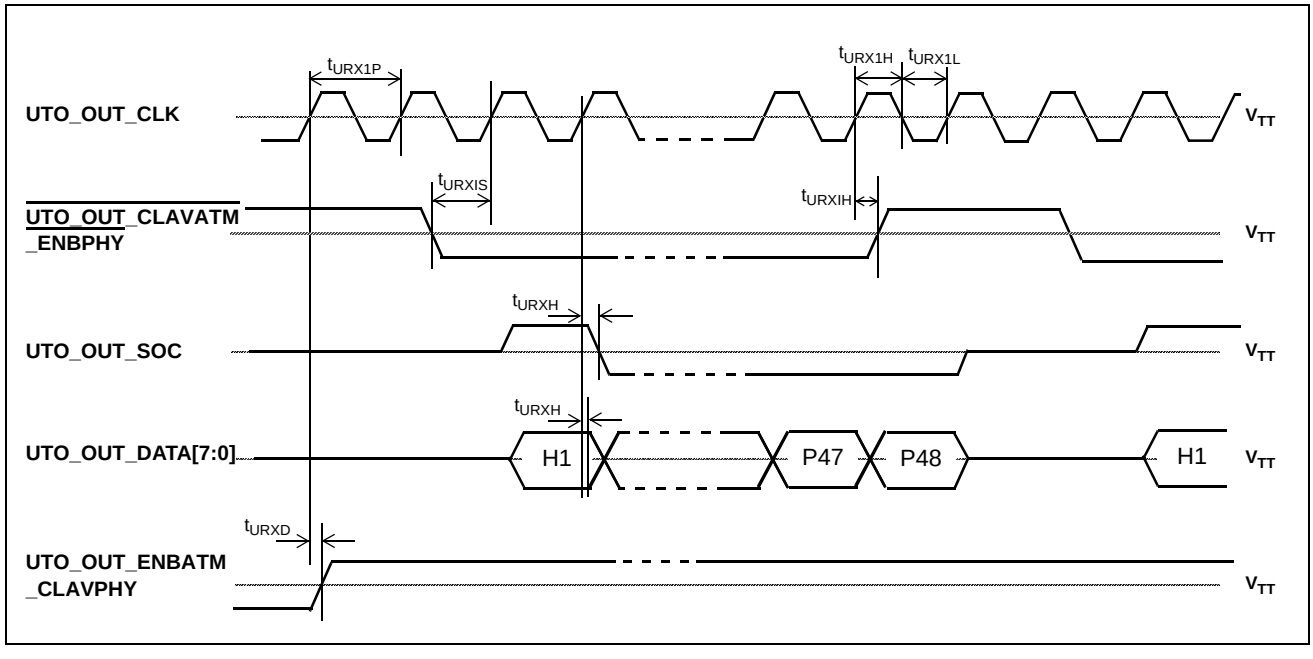


Figure 64 - UTOPIA Level 1 Interface Timing - PHY Mode - Outgoing Data (UTOPIA RX Bus)

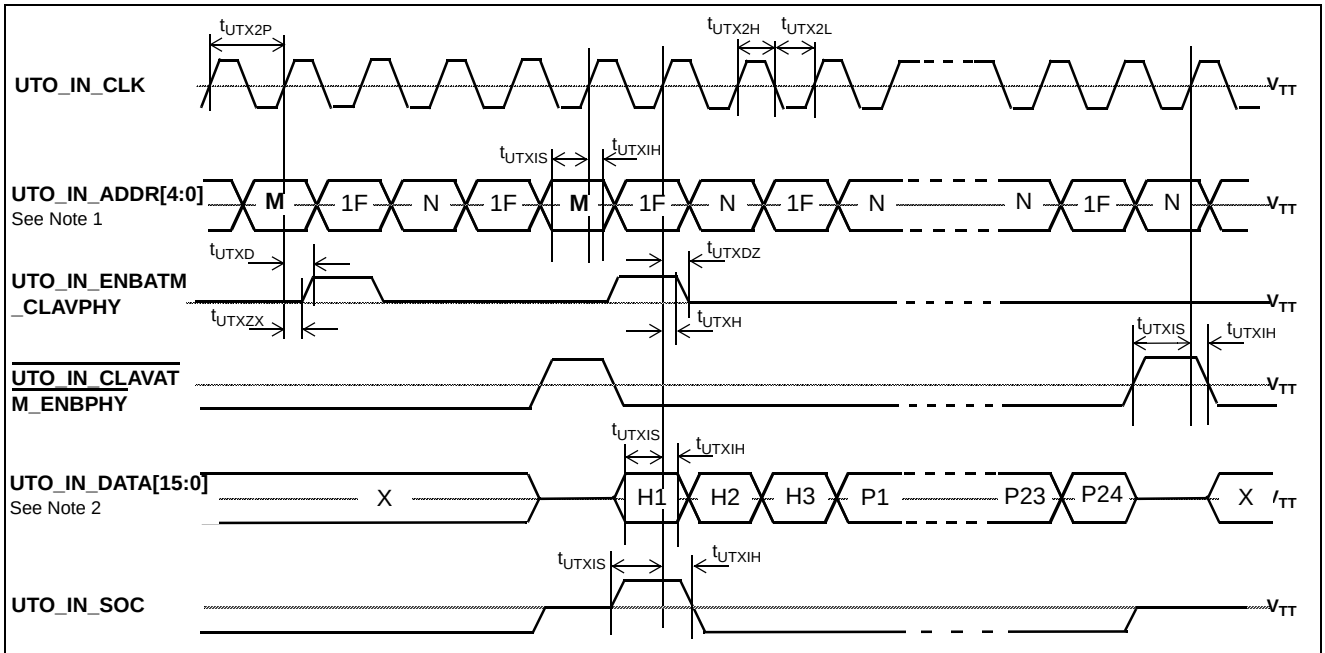
7.2.3.3 UTOPIA Level 2

This section contains the timing diagrams for the MT90528 setup in UTOPIA Level 2 as a PHY device. For functional timing diagrams, refer to the ATM Forum Level 2 specification (af-phy-0039.000).

Since the MT90528 does not support multi-PHY (MPHY) operation in ATM mode, the Level 2 ATM timing diagrams are identical to the ones for Level 1 operation, except that in Level 2, the MT90528 features a 16-bit data bus in both the TX and RX directions and it supports up to 80pF of load at 33 MHz and 40 pF at 52 MHz. Note that the address bus is only used when in PHY mode.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
UTO_IN_CLK Period	t_{UTX2P}	19.23			ns	UTO_IN_CLK = 52 MHz
UTO_IN_CLK Pulse Width (HIGH / LOW)	$t_{UTX2H/L}$	7.7	$t_{UTX2P}/2$		ns	
Input Setup Time - ($\overline{\text{UTO_IN_CLAVATM_ENBPHY}}$, UTO_IN_SOC asserted and UTO_IN_DATA[15:0], UTO_IN_ADDR[4:0] VALID) to UTO_IN_CLK rising	t_{UTXIS}	4			ns	
Input Hold Time - UTO_IN_CLK rising to (UTO_IN_DATA[15:0], UTO_IN_ADDR[4:0] $\overline{\text{INVALID and UTO_IN_SOC,}}$ $\overline{\text{UTO_IN_CLAVATM_ENBPHY}}$ de-asserted)	t_{UTXIH}	1			ns	
Output Delay - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY asserted	t_{UTXD}			13.8 20.5	ns ns	C_L=40 pF; UTO_IN_CLK ≤ 52 MHz C_L=80 pF; UTO_IN_CLK ≤ 33 MHz
Output Hold Time - UTO_IN_CLK rising to (UTO_IN_ENBATM_CLAVPHY change)	t_{UTXH}	1 1			ns ns	C_L=40 pF; UTO_IN_CLK ≤ 52 MHz C_L=80 pF; UTO_IN_CLK ≤ 33 MHz
Drive to High-Z - UTO_IN_CLK rising to UTO_IN_ENBATM_CLAVPHY HIGH-Z	t_{UTXDZ}	1 1		17.5 28.5	ns ns	C_L=40 pF; UTO_IN_CLK ≤ 52 MHz C_L=80 pF; UTO_IN_CLK ≤ 33 MHz
High-Z to Drive - UTO_IN_CLK rising and UTO_IN_ENBATM_CLAVPHY HIGH-Z to UTO_IN_ENBATM_CLAVPHY change	t_{UTXZX}	1 1			ns ns	C_L=40 pF; UTO_IN_CLK ≤ 52 MHz C_L=80 pF; UTO_IN_CLK ≤ 33 MHz

Table 105 - UTOPIA Level 2 Interface Timing - PHY mode - Incoming Data (UTOPIA TX Bus)



Note 1: M is the address of the MT90528; N is the address of another PHY device, where N is *not* equal to M. An address of 1Fh (31d) indicates a null PHY port.

Note 2: UTO_IN_DATA is a 16-bit bus; therefore, P24 indicates the last cell payload word to be transmitted.

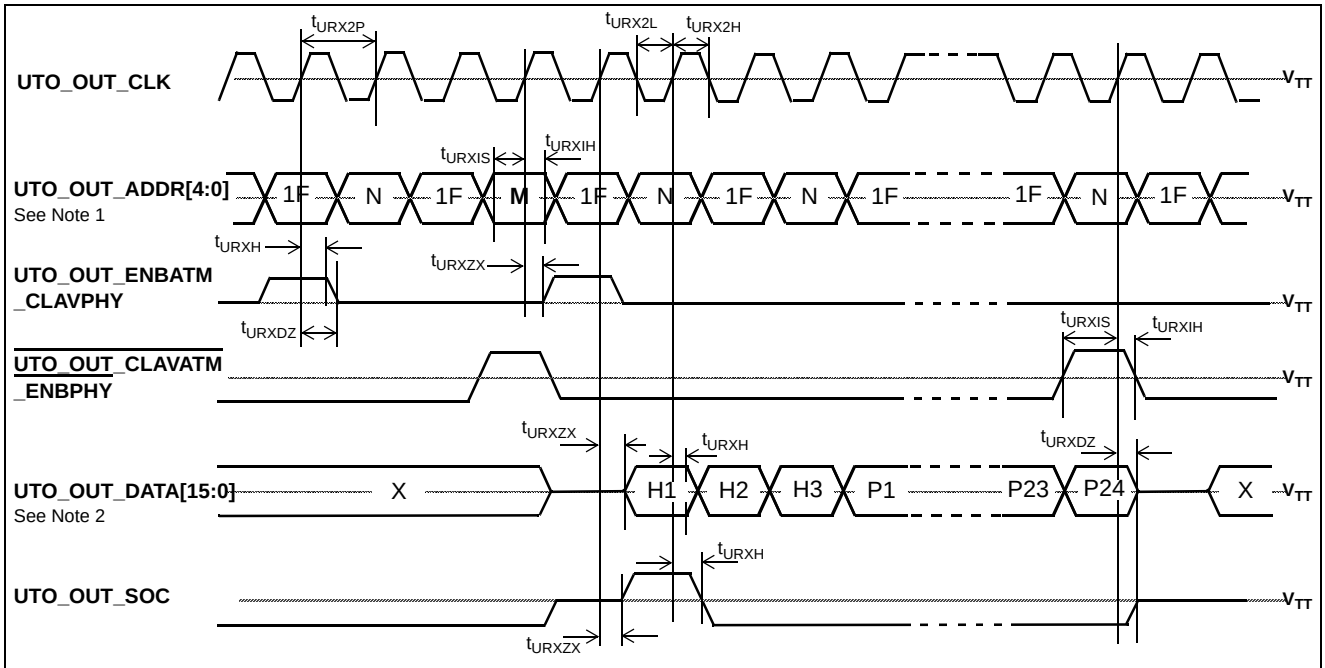
Figure 65 - UTOPIA Level 2 Interface Timing - PHY Mode - Incoming Data (UTOPIA TX Bus)

Characteristic	Sym.	Min.	Ty.p	Max.	Units	Test Conditions
UTO_OUT_CLK Period	t_{URX2P}	19.23			ns	UTO_OUT_CLK = 52 MHz
UTO_OUT_CLK Pulse Width (HIGH / LOW)	$t_{URX2H/L}$	7.7	$t_{URX2P}/2$		ns	
Input Setup Time - UTO_OUT_CLAVATM_ENBPHY asserted and UTO_OUT_ADDR[4:0] VALID) to UTO_OUT_CLK rising	t_{URXIS}	4			ns	
Input Hold Time - UTO_IN_CLK rising to (UTO_OUT_ADDR[4:0] INVALID and UTO_OUT_CLAVATM_ENBPHY de-asserted)	t_{URXIH}	1			ns	
Output Delay - UTO_OUT_CLK rising to (UTO_OUT_ENBATM_CLAVPHY, UTO_OUT_SOC asserted and UTO_OUT_DATA[15:0] VALID)	t_{URXD}			13.5 20.5	ns ns	C_L = 40 pF; UTO_OUT_CLK ≤ 52 MHz C_L = 80 pF; UTO_OUT_CLK ≤ 33 MHz
Output Hold Time - UTO_OUT_CLK rising to (UTO_OUT_DATA[15:0] INVALID and UTO_OUT_ENBATM_CLAVPHY, UTO_OUT_SOC de-asserted)	t_{URXH}	1 1			ns ns	C_L = 40 pF; UTO_OUT_CLK ≤ 52 MHz C_L = 80 pF; UTO_OUT_CLK ≤ 33 MHz
Drive to High-Z - UTO_OUT_CLK rising to (UTO_OUT_ENBATM_CLAVPHY, UTO_OUT_SOC, UTO_OUT_DATA[15:0] HIGH-Z)	t_{URXDZ}	1 1		17.5 28.5	ns ns	C_L = 40 pF; UTO_OUT_CLK ≤ 52 MHz C_L = 80 pF; UTO_OUT_CLK ≤ 33 MHz

Table 106 - UTOPIA Level 2 Interface Timing - PHY mode - Outgoing Data (UTOPIA RX Bus)

Characteristic	Sym.	Min.	Ty.p	Max.	Units	Test Conditions
High-Z to Drive - UTO_OUT_CLK rising and (UTO_OUT_ENBATM_CLAVPHY, UTO_OUT_SOC, UTO_OUT_DATA HIGH-Z) to (UTO_OUT_ENBATM_CLAVPHY, UTO_OUT_SOC, UTO_OUT_DATA[15:0]) change	t_{URXZX}	1 1			ns ns	C_L = 40 pF; UTO_OUT_CLK ≤ 52 MHz C_L = 80 pF; UTO_OUT_CLK ≤ 33 MHz

Table 106 - UTOPIA Level 2 Interface Timing - PHY mode - Outgoing Data (UTOPIA RX Bus)



Note 1: M is the address of the MT90528; N is the address of another PHY device, where N is *not* equal to M. An address of 1Fh (31d) indicates a null PHY port.

Note 2: UTO_OUT_DATA is a 16-bit bus; therefore, P24 indicates the last cell payload word to be transmitted.

Figure 66 - UTOPIA Level 2 Interface Timing - PHY Mode - Outgoing Data (UTOPIA RX Bus)

8.0 Applications

8.1 Board-Level Applications

8.1.1 Power-Up and Power-Down Sequence

To prevent device latch-up, it is recommended to turn on the I/O power (3.3 V) first, followed by the core power (2.5 V). This can be done in one of two ways:

- By powering up the 3.3 V rail first, preventing the 2.5 V rail from powering up until the 3.3 V rail is stable.
- By placing a Schottky diode between the 3.3 V and 2.5 V power rails (connecting the anode to the 2.5 V rail and the cathode to the 3.3 V rail).

In general, the power-down sequence should be the reverse of the power-up sequence. Thus, the 2.5 V rail should be turned off first, followed by the 3.3 V rail.

8.1.2 External Memory Interface Connections

The MT90528 can interface with both the pipelined and flow-through types of synchronous static zero bus turnaround (ZBT) RAM. The clock driving the external memory device **must** be the same as the clock which is fed to the MT90528 at its MCLK input, as shown in Figure 67 below.

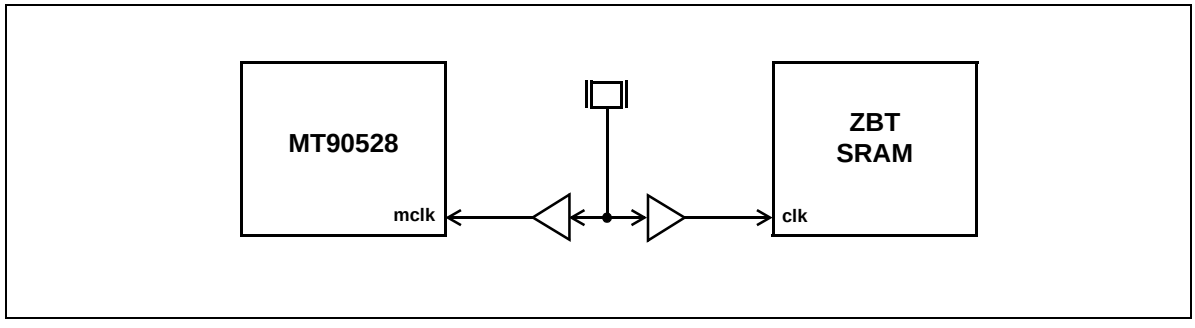


Figure 67 - External Memory Interface

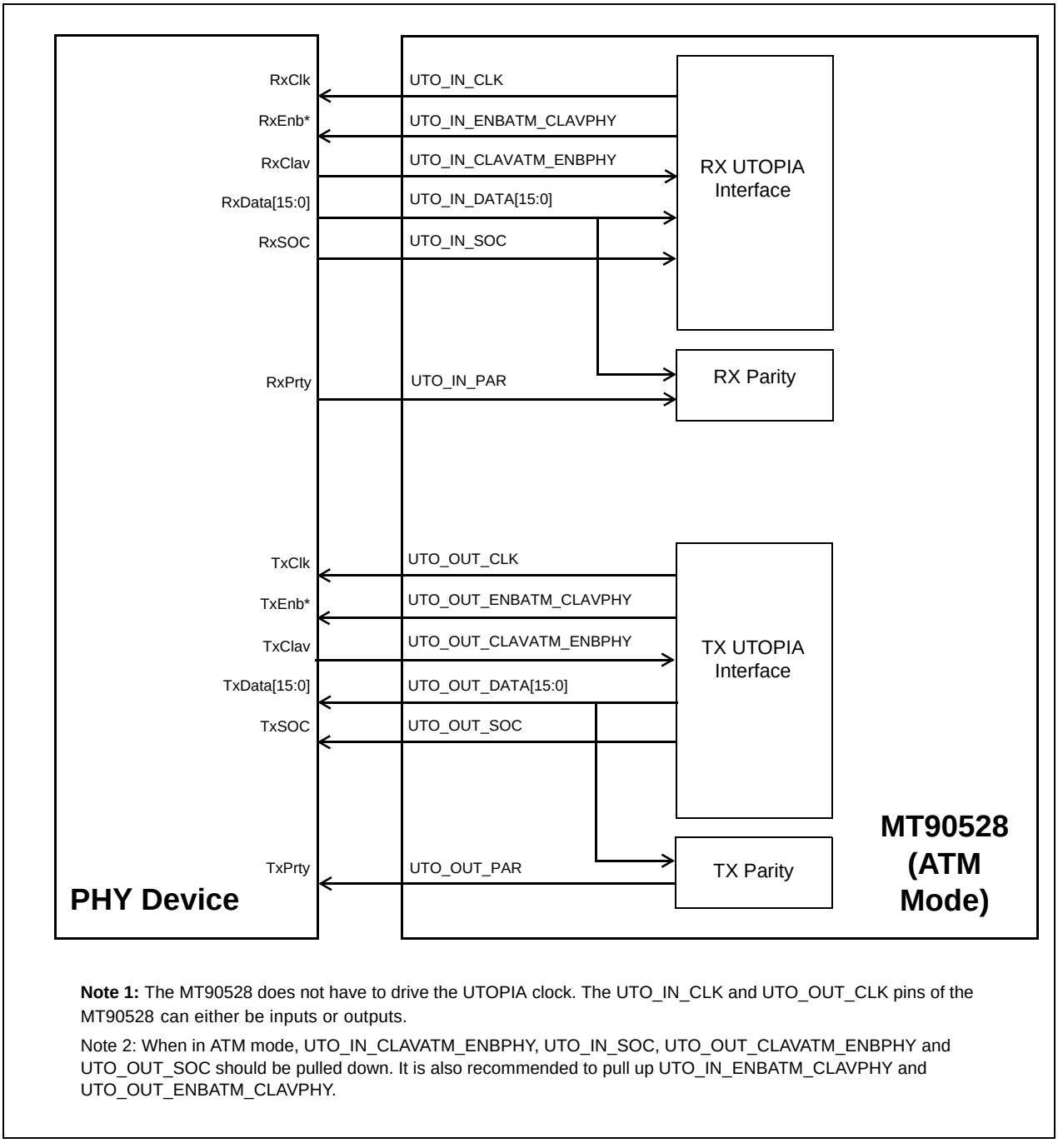
8.1.3 UTOPIA Interface Connections

The following table lists all of the signals on the UTOPIA interface of the MT90528. In addition, it indicates what the pin corresponds to in terms of the functionality of the UTOPIA standard, depending on the mode of operation of the UTOPIA interface.

MT90528 Signal Name	MT90528 Signal Direction	Standard Signal Name - Level 1 ATM	Standard Signal Name - Level 1 PHY	Standard Signal Name - Level 2 ATM	Standard Signal Name - Level 2 PHY
UTO_IN_CLK	I / O	RxClk	TxClk	RxClk	TxClk
UTO_IN_ADD[4:0]	I	-	-	-	TxAddr[4:0]
UTO_IN_DATA[15:8]	I	-	-	RxData[15:8]	TxData[15:8]
UTO_IN_DATA[7:0]	I	RxData[7:0]	TxData[7:0]	RxData[7:0]	TxData[7:0]
UTO_IN_PAR	I	RxPrty	TxPrty	RxPrty	TxPrty
UTO_IN_SOC	I	RxSOC	TxSOC	RxSOC	TxSOC
UTO_IN_CLAVATM _ENBPHY	I	RxClav	TxEnb*	RxClav	TxEnb*
UTO_IN_ENBATM _CLAVPHY	O	RxEnb*	TxClav	RxEnb*	TxClav
UTO_OUT_CLK	I / O	TxClk	RxClk	TxClk	RxClk
UTO_OUT_ADD[4:0]	I	-	-	-	RxAddr[4:0]
UTO_OUT_DATA[15:8]	O	-	-	TxData[15:8]	RxData[15:8]
UTO_OUT_DATA[7:0]	O	TxData[7:0]	RxData[7:0]	TxData[7:0]	RxData[7:0]
UTO_OUT_PAR	O	TxPrty	RxPrty	TxPrty	RxPrty
UTO_OUT_SOC	O	TxSOC	RxSOC	TxSOC	RxSOC
UTO_OUT_CLAVATM _ENBPHY	I	TxClav	RxEnb*	TxClav	RxEnb*
UTO_OUT_ENBATM _CLAVPHY	O	TxEnb*	RxClav	TxEnb*	RxClav

Table 107 - MT90528 UTOPIA Signal Directions

Figure 68 below illustrates the connections from the external pins of the UTOPIA interface to a PHY device, when the MT90528 is operating in ATM mode.

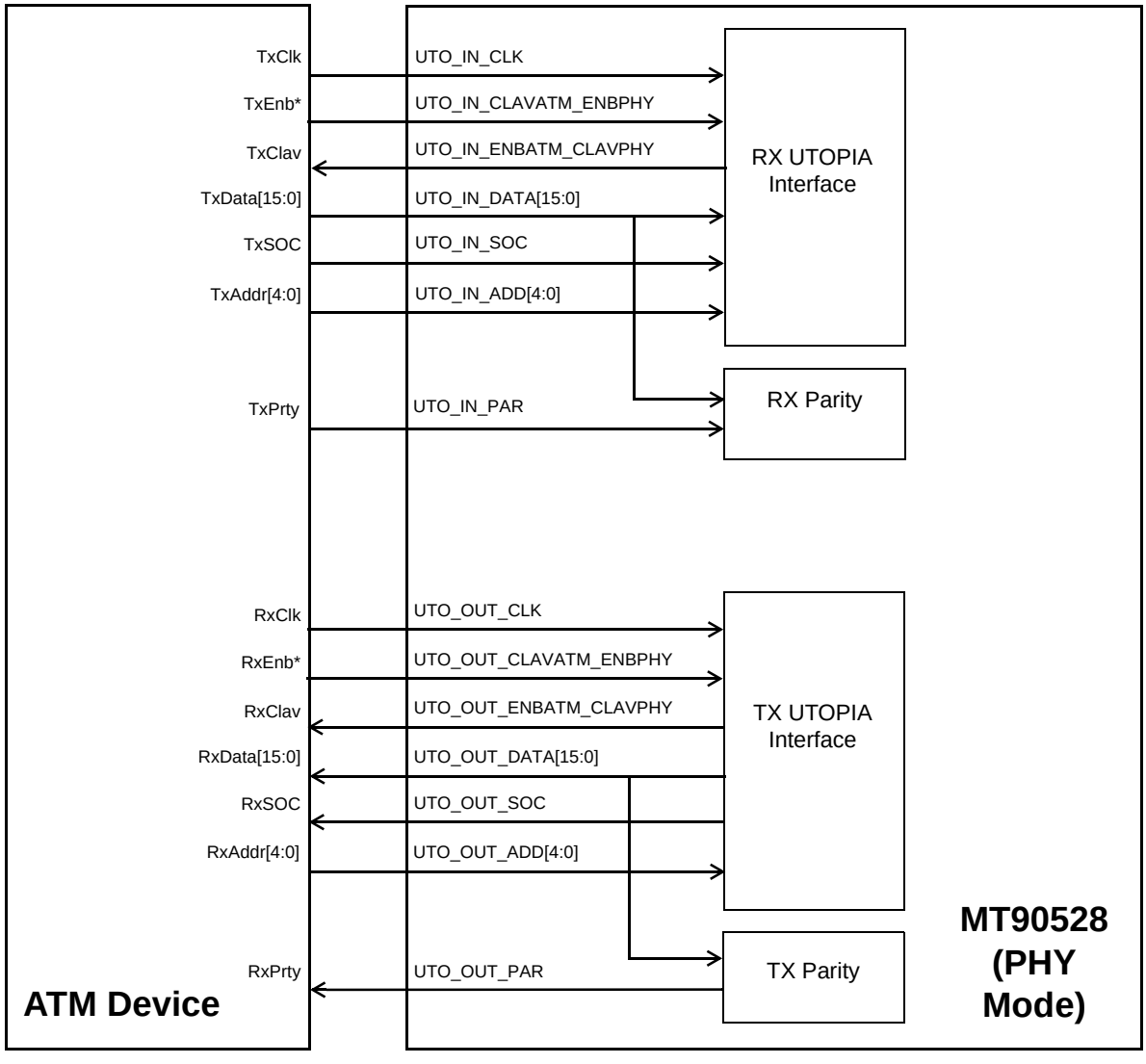


Note 1: The MT90528 does not have to drive the UTOPIA clock. The UTO_IN_CLK and UTO_OUT_CLK pins of the MT90528 can either be inputs or outputs.

Note 2: When in ATM mode, UTO_IN_CLAVATM_ENBPHY, UTO_IN_SOC, UTO_OUT_CLAVATM_ENBPHY and UTO_OUT_SOC should be pulled down. It is also recommended to pull up UTO_IN_ENBATM_CLAVPHY and UTO_OUT_ENBATM_CLAVPHY.

Figure 68 - ATM Mode: External UTOPIA Pin Connections

Figure 69 illustrates the connections from the external pins of the UTOPIA interface to an ATM device, when the MT90528 device is operating in PHY mode.



Note 1: The ATM device is not required to drive the UTOPIA clock. The UTO_IN_CLK and UTO_OUT_CLK pins of the MT90528 can either be inputs or outputs.

Note 2: When in PHY mode, UTO_IN_ENBATM_CLAVPHY, UTO_IN_SOC, UTO_OUT_ENBATM_CLAVPHY and UTO_OUT_SOC should be pulled down. It is also recommended to pull up UTO_IN_CLAVATM_ENBPHY and UTO_OUT_CLAVATM_ENBPHY.

Figure 69 - PHY Mode: External UTOPIA Pin Connections

8.2 Segmentation and Reassembly Latency

End-to-end latency, or delay, of the AAL1 segmentation and reassembly process of the MT90528 can be expressed in a simplified manner as:

end-to-end delay =

cell payload assembly time + internal TX queuing + internal TX processing

+ physical layer and network delays

+ UTOPIA RX queuing + internal RX processing + pointer offset + CDV buffering

Some components of the latency, such as UDT cell payload assembly delay, are determined by the AAL1 standards. Some components of the latency are partially under the control of the application, such as SDT cell payload assembly time where the number of channels can be increased to reduce cell payload assembly time. Some components of the latency are a function of the MT90528 architecture, which has been designed to minimize this latency. Finally, some components are externally determined, such as the physical layer and network delays, and network Cell Delay Variation (CDV) which must be compensated for in the CDV buffering.

Mode	Cell Payload Assembly (μsec)	TX Queuing (μsec)	TX Processing (μsec)	Total TX / Segmentation (μsec)
UDT T1	243.5	min: 0 max: 62.9	2.3	min: 245.8 max: 308.7
UDT E1	183.6	min: 0 max: 62.9	2.3	min: 185.9 max: 248.8
SDT	min: FLOOR[46/N] X 125 max: CEIL[47/N] X 125	min: 0 max: 125	125	min: 125 + FLOOR[46/N] X 125 max: 250 + CEIL[47/N] X 125
SDT Trunking N > 46	125	min: 0 max: 125	125	min: 250 max: 375

Table 108 - Segmentation Latency

NOTE: “N” is the number of TDM channels carried by a particular ATM VC.

Cell Payload Assembly delay is the amount of time the TDM interface requires to deliver enough data to fill an AAL1 cell. Note that the latency given in Table 108 is for the first bit of TDM data packed in the AAL1 cell, i.e. the bit which sees the longest delay before cell transmission. Since reassembly latency is inverted from this segmentation latency (first-in-first-out) this method gives correct end-to-end latency for all bits in the cell when segmentation and re-assembly delays are summed. The cell payload asssembly delay in SDT mode is a function of “N”, the number of TDM channels carried by the VC. The FLOOR[x] function means “the largest integer less than, or equal to, x” and the CEIL[x] function means “the smallest integer greater than, or equal to, x”. Cell payload assembly is a static delay in UDT mode. Cell payload assembly is a variable delay in SDT mode, due both to the variation in payload size (46 bytes and 47 bytes) specified in the AAL1 standards, and to remainders when fitting N channels into the cell payload.

TX Queuing represents the possible delay due to cell operations queuing in front of the single high-speed TDM segmentation and cell-assembly engine (TX_SAR). In UDT mode, worst case for this is the time taken to process 27 cells (one for each of the other TDM ports). In SDT mode, worst case for TX Queueing with a porperly configured control structure is always less than a TDM frame (125 microseconds). This is a variable delay, and the number given here is the peak, worst-case, low-probability value.

TX Processing is the time required for internal processing and data moves. This is a fixed delay in UDT and SDT mode.

Physical layer and network delays are the delays due to speed-of-transmission delays in the physical layer, including transmission time on the UTOPIA bus, and queuing delays at the switches through the network, including queuing in front of the physical layer devices directly connected to the MT90528. This is in general a variable delay, and usually represents the largest source of Cell Delay Variation (CDV) that the reassembly path (RX_SAR) has to deal with.

Mode	RX UTOPIA Queuing (μsec)	RX Processing (μsec)	Pointer Offset (μsec)	CDV Buffering (μsec)	Total RX / Reassembly (μsec)
UDT T1	min: 0 max: 45.8	1.7	min:0 max: 243.5	0.5 X Max_Lead X 5.18	min: 1.7 + 2.59 X Max_Lead max: 291 + 2.59 X Max_Lead
UDT E1	min: 0 max: 45.8	1.7	min: 0 max: 183.6	0.5 X Max_Lead X 3.91	min: 1.7 + 1.95 X Max_Lead max: 231.1 + 1.95 X Max_Lead
SDT	min: 0 max: 125	125	min: 0 max: 125	0.5 X Max_Lead X 125	min: 125 + 62.5 X Max_Lead max: 375 + 62.5 X Max_Lead
SDT Trunking N > 46	min: 0 max: 125	125	min: 0 max: 125	0.5 X Max_Lead X 125	min: 125 + 62.5 X Max_Lead max: 375 + 62.5 X Max_Lead

Table 109 - Reassembly Latency

RX UTOPIA Queuing represents the possible delay due to a burst of cells arriving faster than the RX_SAR can process them. In UDT mode, the worst case is 27 cells (one for each of the other TDM ports), and in SDT mode the worst case is always less than 125 microseconds. This is a variable delay.

RX Processing delay is the time required for internal processing and data moves. This is a fixed delay in UDT and SDT mode.

Pointer Offset represents the random time-offset between segmentation operation at one end of link, and reassembly operation at the other end of link. In UDT mode this is some fraction of a cell payload assembly period. In SDT mode this is some fraction of the 125 microsecond TDM frame. This is a static delay, except for wander difference in the segmentation and reassembly TDM clocks.

CDV Buffering is the delay due to the cell-delay-variation buffer, and is controlled by the setting (per-VC) of the internal “Maximum Lead” variable. The delay through the CDV buffer is generally one-half of the limit set by the “Maximum Lead” variable.

Mode	Total Static TX / Segmentation (μsec)	Total Static RX / Reassembly (μsec)	End-to-End Latency (μsec)
UDT T1 - min	245.8	1.7 + 2.59 X Max_Lead	490.96 + CDV + network
max	245.8	245.2 + 2.59 X Max_Lead	734.46 + CDV + network
UDT E1 - min	185.9	1.7 + 1.95 X Max_Lead	370.9 + CDV + network
max	185.9	185.3 + 1.95 X Max_Lead	554.5 + CDV + network
SDT - min	125 + FLOOR[46/N] X 125	125 + 62.5 X Max_Lead	375 + FLOOR[46/N] X 125 + CDV + network
max	125 + CEIL[47/N] X 125	250 + 62.5 X Max_Lead	500 + CEIL[47/N] X 125 + CDV + network
SDT Trunking - min	250	125 + 62.5 X Max_Lead	500 + CDV + network
max	250	250 + 62.5 X Max_Lead	625 + CDV + network

Table 110 - End-to-End Latency

Since the variable portions of the delay in segmentation and reassembly effectively become part of the CDV that must be compensated for in the CDV buffer, we can omit them from the end-to-end calculation. (Also remembering that the variable delays given in Table 108 and Table 109 are worst-case numbers that will never be experienced by most applications.) The delay variation in SDT mode due to payload size variation and divide-by-N remainders is also part of the CDV compensated for by the CDV buffer, but is left in here to illustrate the effects on delay of the value of N.

The Max_Lead values should be set by the user in accordance with the expected or negotiated CDV, as explained in “UDT Mode of Operation” on page 79 and in “SDT Mode of Operation” on page 80. These recommended settings are used to evaluate Max_Lead in Table 110. It can be seen that the difference between the minimum and maximum static delay in each mode is due largely to the pointer offset, which, as described earlier, is the random offset between the time of the segmentation operation and the time of the reassembly operation.

The delay values for SDT assume no TDM switching delay. This means that the given delay is for a TDM byte which is driven out at the RX end on the same TDM channel number as it was sampled in at the TX end. For example, if the TDM byte comes into the segmentation end on TDM channel 3, it is driven out at the reassembly end on TDM channel 3.

9.0 Reference Documents

9.1 Normative Standards

- ITU-T Rec. I.363.1, “B-ISDN ATM Adaptation Layer Specification: Type 1 AAL,” Aug. 1996.
- ATM Forum af-vtoa-0078.000, “Circuit Emulation Service Interoperability Specification Version 2.0,” Jan. 1997.
- ATM Forum, af-vtoa-0089.001, “ATM Trunking using AAL1 for Narrowband Services Version 1.1,” Feb. 2000.
- ITU-T I.361, “B-ISDN ATM Layer Specification,” Nov. 1995.
- ITU-T I.362, “B-ISDN ATM Adaptation Layer (AAL) Functional Description,” Mar. 1993.
- IEEE Std. 1149.1a-1993, “IEEE Standard Test Access Port and Boundary Scan Architecture.”
- ATM Forum af-phy-0017.000, “UTOPIA, An ATM-PHY Interface Specification: Level 1, Version 2.01,” Mar. 1994.
- ATM Forum af-phy-0039.000, “Utopia Level 2, Version 1.0,” June 1995.
- ITU-T G.823, “The Control of Jitter and Wander within Digital Networks which are based on the 2048 kbit/s Hierarchy,” Mar. 1993.
- ITU-T G.824, “The Control of Jitter and Wander within Digital Networks which are based on the 1544 kbit/s Hierarchy,” Mar. 1993.
- ANSI T1.102, “Telecommunications - Digital Hierarchy - Electrical Interfaces,” 1993.
- ANSI T1.403, “Telecommunications - Network and Customer Installation Interfaces - DS1 Electrical Interface Informative Standards and References,” 1995.

9.2 Informative Standards

- ANSI T1.630 -1993, “Broadband ISDN - ATM Adaptation Layer for Constant Bit Rate Services Functionality and Specification,” Aug. 1993.
- ETSI Std. ETS 300 353, “B-ISDN; ATM Adaptation Layer (AAL) specification - type1,” Dec. 1996 (2nd Ed, Draft)
- Telcordia GR-1113-CORE, Issue 1, July, 1994, Asynchronous Transfer Mode (ATM) and ATM Adaptation Layer (AAL) Protocols.
- MSAN-163, “Multitrunk System Synchronizer”, Issue 1, Zarlink Application Note for the MT9042 PLL, December 1996.
- M. Noorchasm et al., “Buffer Design for Constant Bit Rate Services in Presence of Cell Delay Variation,” ATM Forum Contribution 95-1454.
- Paul E. Fleischer and Chi-Leung Lau, “Synchronous Residual Time Stamp for Timing Recovery in a Broadband Network,” United States Patent 5,260,978, Nov. 1993.

Note: Telcordia (formerly Bellcore) asserts that its U.S. Patent No. 5,260,978 for Synchronous Residual Timestamp (SRTS) Timing Recovery in a Broadband Network may apply to the ATM Adaptation Layer Type 1 (AAL1) ANSI Standard (T1.630-1993) referenced in Section 3.4 of af-vtoa-0078.000.

10.0 Glossary

AAL - *ATM Adaptation Layer*; standardized protocols used to translate higher layer services from multiple applications into the size and format of an ATM cell.

AAL1 - *ATM Adaptation Layer 1*, used for the transport of constant bit rate, time-dependent traffic (e.g., voice, video); requires transfer of timing information between source and destination; maximum of 47-bytes of user data permitted in payload as an additional header byte is required to provide sequencing information.

Asynchronous - 1. Not **synchronous**; not periodic. 2. The temporal property of being sourced from independent timing references. Asynchronous signals have different frequencies, and no fixed phase relationship. 3. In telecom, data which is not synchronized to the public network clock. 4. The condition or state when an entity is unable to determine, prior to its occurrence, exactly when an event will transpire.

ATM - *Asynchronous Transfer Mode*; a method in which information to be transferred is organized into fixed-length cells; asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic. (While ATM cells are transmitted synchronously to maintain clock between sender and receiver, the sender transmits data cells when it has something to send and transmits empty cells when idle, and is not limited to transmitting data every Nth cell.)

CBR - *Constant Bit Rate*; an ATM service category supporting a constant or guaranteed rate, with timing control and strict performance parameters. Used for services such as voice, video, or circuit emulation.

CDV - *Cell Delay Variation*; a **QoS** parameter that measures the peak-to-peak cell delay through the network; results from buffering and cell scheduling.

Cell - fixed-size information package consisting of 53 bytes (octets) of data; of these, 5 bytes represent the cell header and 48 bytes carry the user payload and required overhead. **Note:** If a 16-bit UTOPIA interface is used, each cell is 54 bytes long, composed of 6 bytes of cell header and 48 bytes carrying user payload and required overhead.

CES - *Circuit Emulation Service*; ATM Forum service providing a virtual circuit which emulates the characteristics of a constant bit rate, dedicated-bandwidth circuit (e.g., DS1).

CLP - *Cell Loss Priority*; a 1-bit field in the ATM cell header that corresponds to the loss priority of a cell; cells with CLP = 1 can be discarded in a congestion situation.

CSI - *Convergence Sublayer Indication* bit in the AAL1 header byte; when present in an even-numbered cell using SDT, indicates the presence of a pointer byte; used to transport RTS values in odd-numbered cells using SRTS clock recovery.

GFC - *Generic Flow Control*; 4-bit field in the ATM header used for local functions (not carried end-to-end); when cells are configured for NNI formatting, this value forms the four MSBs of the VPI field.

HEC - *Header Error Control*; using the fifth octet in the ATM cell header, ATM equipment (usually the PHY) may check for an error and correct the contents of the header; CRC algorithm allows for single-error correction and multiple-error detection.

Isochronous - The temporal property of an event or signal recurring at known periodic time intervals (e.g., 125 μs). Isochronous signals are dependent on some uniform timing, or carry their own timing information embedded as part of the signal. Examples are DS1, E1 and TDM in general. From the root words, “iso” meaning equal, and “chronous” meaning time.

OAM - *Operations, Administration and Maintenance*; MSB within the PTI field of the ATM cell header which indicates if the ATM cell carries management information such as fault indications.

PHY - *Physical Layer*; bottom layer of the ATM Reference Model; provides ATM cell transmission over the physical interfaces that interconnect the various ATM devices.

Plesiochronous - The temporal property of being arbitrarily close in frequency to some defined precision. Plesiochronous signals occur at nominally the same rate, any variation in rate being constrained within specific limits. Since they are not identical, over the long term they will be skewed from each other. This will force a switch to occasionally repeat or delete data in order to handle buffer underflow or overflow. (In telecommunications, this is known as a frame slip.)

PTI - *Payload Type Identifier*; 3-bit field in the ATM cell header - MSB indicates if the cell contains **OAM** information or user data.

QoS - *Quality of Service*; ATM performance parameters that characterize the transmission quality over a given VCC (e.g., cell delay variation; cell transfer delay, cell loss ratio).

RTS - Residual Time Stamp; see **SRTS**.

SAR - *Segmentation and Reassembly*; method of partitioning, at the source, frames into ATM cells and reassembling, at the destination, these cells back into information frames; lower sublayer of the **AAL** which inserts data from the information frames into cells and then adds the required header, trailer, and/or padding bytes to create 48-byte payloads to be transmitted to the ATM layer.

SDT - *Structured Data Transfer*; format used within **AAL1** for blocks consisting of Nx64 kbps channels; blocks are segmented into cells for transfer and additional overhead bytes (pointers) are used to indicate structure boundaries within cells (therefore aiding data recovery).

SN - *Sequence Number*; 4-bit field in the **AAL1** header byte used as a sequence counter for detecting lost or misinserted ATM cells.

SNP - *Sequence Number Protection*; 4-bit field in the **AAL1** header byte consisting of a 3-bit CRC and a parity bit which are designed to provide error-correction on the **SN**.

SRTS - *Synchronous Residual Time Stamp*; method for clock recovery in which difference signals between a source clock and the network reference clock (time stamps) are transmitted to allow reconstruction of the source clock. The destination reconstructs the source clock based on the time stamps and the network reference clock. (Note that the same network reference clock is required at both ends.)

Synchronous - 1. The temporal property of being sourced from the same timing reference. Synchronous signals have the same frequency, and a fixed (often implied to be zero) phase offset. 2. A mode of transmission in which the sending and receiving terminal equipment are operating continually at the same rate and are maintained in a desired phase relationship by an appropriate means.

UDT - *Unstructured Data Transfer*; format used within **AAL1** for transmission of user data without regard for structure boundaries (e.g., circuit emulation).

UTOPIA - *Universal Test and Operations Physical Interface for ATM*; a **PHY**-level interface to provide connectivity between ATM components.

VC - *Virtual Channel* (also, *Virtual Circuit*); one of several logical connections defined within a virtual path (**VP**) between two ATM devices; provides sequential, unidirectional transport of ATM cells.

VCC - *Virtual Circuit Connection;* term used to include both **VPI** and **VCI**.

VCI - *Virtual Channel Identifier*; 16-bit value in the ATM cell header that provides a unique identifier for the virtual channel (**VC**) within a virtual path (**VP**) that carries a particular cell.

VP - *Virtual Path*; a unidirectional logical connection between two ATM devices; consists of a set of virtual channels (**VC**).

VPI - *Virtual Path Identifier*; 8-bit value (in UNI; 12 bits in NNI) in the ATM cell header that indicates the virtual path (**VP**) to which a cell belongs.

VTOA - *Voice and Telephony over ATM*; intended to provide voice connectivity to the desktop, and to provide interoperability with existing N-ISDN and PBX services.

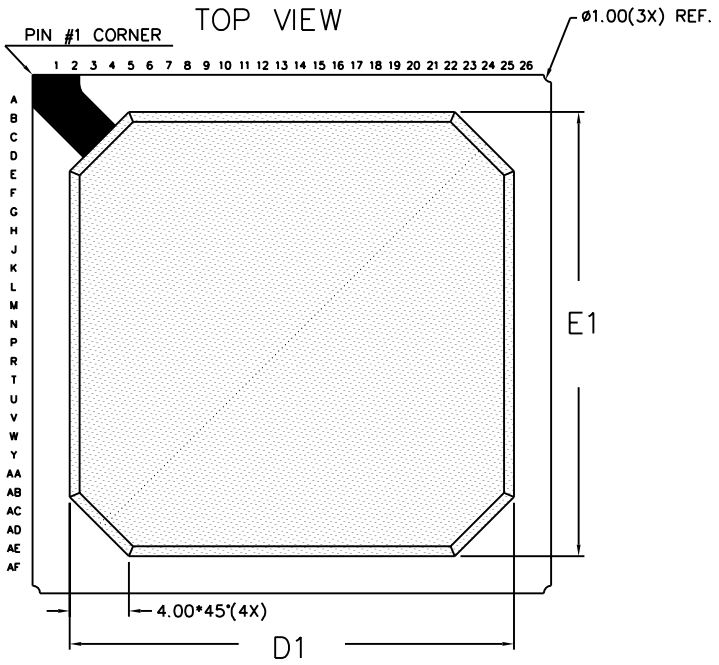
ZBT - *Zero Bus Turnaround;* a type of memory interface which does not require wait states between read and write cycles. ZBT and Zero Bus Turnaround are trademarks held by Integrated Device Technology Inc.

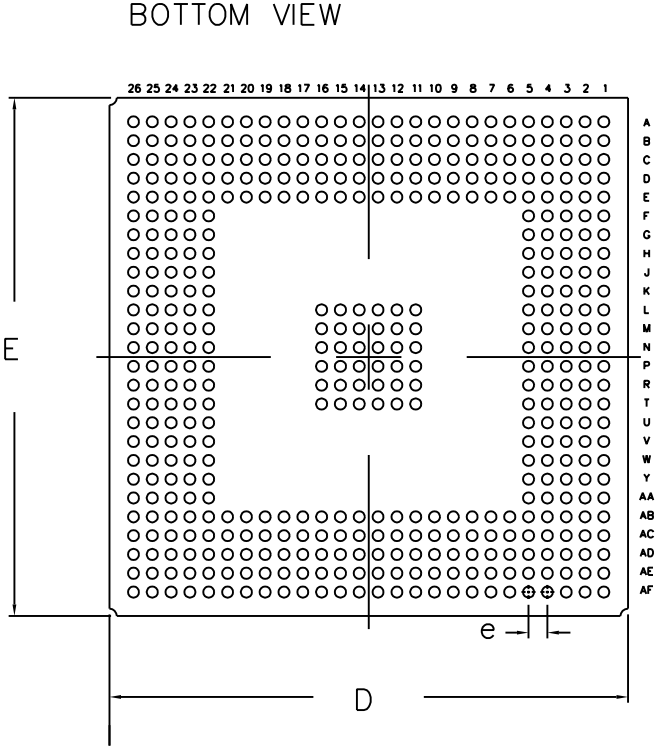
10.1 Glossary References:

The ATM Glossary - ATM Year 97 - Version 2.1, March 1997

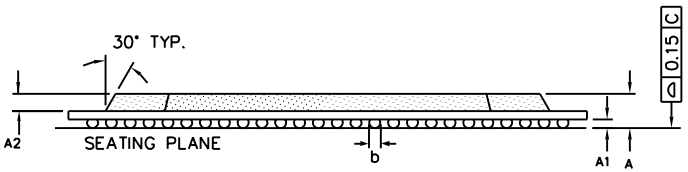
The ATM Forum Glossary - May 1997

Zarlink Semiconductor Glossary of Telecommunications Terms - May 1995.





DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	34.80	35.20
D1	30.00 REF	
E	34.80	35.20
E1	30.00 REF	
b	0.60	0.90
e	1.27	
N	456	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM.

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ACN	10Sep02			
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ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GA

Package Outline for
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