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1.0 Decoder Section

Following the filter section in the MT8870D is a decoder employing digital counting techniques to determine the frequencies of the incoming tones. A complex algorithm is then used to validate DTMF in the presence of speech and noise. EST output will go high to indicate a valid DTMF detection.

2.0 Steering Circuit

Before registration of a decoded tone pair, the MT8870D checks for a valid signal duration. The check is performed by an external RC time constant driven by EST and is known as the guard time circuit. Provided signal condition is maintained (EST remains high) for the guard time and Vc (voltage of capacitor C) reaches the threshold (VTST) at St/GT input, the steering logic will then register the tone pair, latching its corresponding 4-bit code into the output latch. Finally, after a short delay for the output latch to settle, the delayed steering output flag STD goes high, signaling that the received DTMF 4-bit code is ready for the external micro-controller. And STD pin will go low after the valid DTMF signal disappears as validated by the algorithm.

3.0 Power Down

The MT8870D provides a power down mode to minimize power consumption. A logic high applied to PWDN pin stops the crystal oscillator and the function of the analog filters by shutting down the operational amplifiers. In the event that PWDN pin is set high when a valid DTMF tone pair is present, STD will not go low immediately. This is due to the fact that the typical analog circuitry power down time is 30 ms and could be as long as a second depending on the power supply decoupling arrangement. When PWDN is set high, DTMF signal in the filters could still appear for sometime and hence STD will go low only after the valid DTMF disappears as validated by the algorithm. In other words, STD will not go low at the same time when PWDN is activated.

4.0 PWDN and STD

For applications that require STD to go low immediately when PWDN is high, the following external arrangement could be used. STD1 will go low when PWDN goes high.
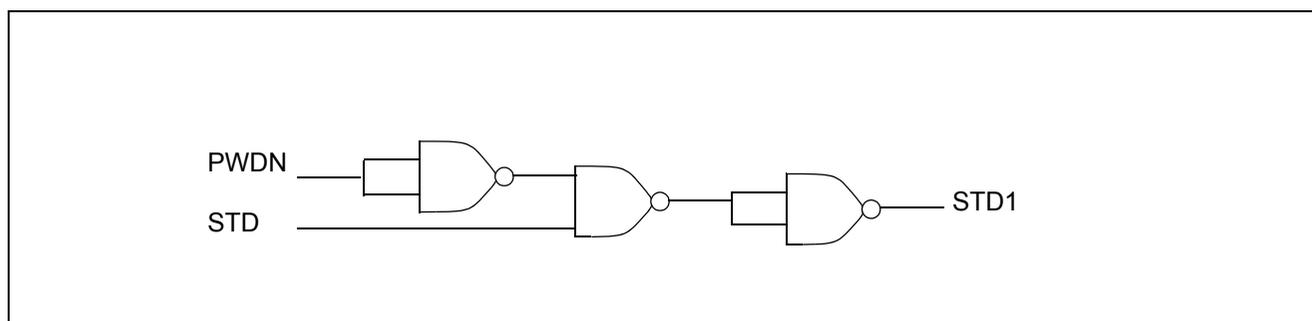

Figure 1 - Power Down and Delayed Steering Output (STD) Detail

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