Application Note **MSAN-179**

MT88E46 and MT88E45 CAS Detector Design Guide

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Contents

1.0 Abstract

This application note describes the differences between the CAS detectors in the MT88E46 and MT88E45 integrated circuits. The devices are pin compatible and are functionally the same, except that the MT88E46 CAS detector uses a different architecture which provides better speech immunity than the MT88E45. The CAS detection AC electrical characteristics are also different. The CPE designer should consult the datasheets for details.

Design guidelines are provided so that for Bellcore CIDCW (Calling Identity Delivery on Call Waiting) and CWD (Call Waiting Deluxe) CPE applications, a design can use the devices interchangeably to address different market segments. The design would be manufactured using the MT88E46 or MT88E45, depending on whether the market segment requires Bellcore speech immunity compliance.

CAS detection firmware design guidelines are also provided for MT88E46 only and MT88E45 only applications.

2.0 CAS Detection Modes

For FSK and power down, the CB1 and CB2 input pins control both devices in the same way. For CAS detection, CB1/2 select between the GS1 and GS2 input op-amps the same way in both devices. However, the MT88E46 CAS detector uses different algorithms depending on which op-amp is selected, as shown in Table 1, whereas the MT88E45 algorithm remains the same in both CB1/2 states.

The MT88E46 CAS detector has 2 modes of operation - 'off-hook mode' and 'on-hook mode'. The 2 modes employ different algorithms which are optimized for the CPE states (off-hook and on-hook). Both algorithms are different from that in MT88E45.

The MT88E46 'off-hook mode' is available at the GS2 op-amp. It is optimized for both talk off and talkdown, and is fully Bellcore compliant when the near end speech is attenuated 8dB or better. The off-hook mode should be used when the CPE itself is off-hook.

CB1	CB2	Input Op-Amp	MT88E46	MT88E45
1	0	GS2	**'Off-hook Mode' CAS Detection.** The algorithm is optimized for both talkoff and talkdown.	**CAS Detection at the GS2 op-amp.** There is only one detection algorithm.
0	1	GS1	**'On-hook Mode' CAS Detection.** The algorithm is optimized for talkdown only.	**CAS Detection at the GS1 op-amp.** There is only one detection algorithm.

Table 1 - CAS Detection Selected by CB1/2

The MT88E46 'on-hook mode' is available at the GS1 op-amp. It is optimized for talkdown only and typically meets Bellcore talkdown condition 1 without near end speech attenuation. The enhanced talkdown performance is designed to work with the TIA's MEI scheme (TIA = Telecommunications Industry Association, MEI = Multiple Extension Interworking) for the situation when the CPE itself is on-hook but the line is in use, so that the CPE can fulfill its role as the ACK-Sender or Backup ACK-Sender (see MT88E46 datasheet). Since the on-hook mode is optimized for talkdown only, it must not be used when the CPE itself is off-hook.

When the application is a telephone set, or a telephone adjunct box with a telephone hybrid / speech IC, the GS1 and GS2 op-amps of both devices should be connected as follows:

- The GS2 op-amp should be used to connect to the receive pair of the telephone hybrid or speech IC and selected when the CPE itself is off-hook. For the MT88E46, when CAS detection from the GS2 op-amp is selected, the 'off-hook mode' algorithm is also selected. The off-hook mode is optimized for both talkoff and talkdown.
- The GS1 op-amp should be used to connect to Tip/Ring and selected when the CPE itself is on-hook but the line is in use. For the MT88E46, when CAS detection from the GS1 op-amp is selected, the 'on-hook mode' algorithm is also selected. The on-hook mode is optimized for talkdown in the MEI on-hook CPE situation so that the CPE can fulfill its role as the ACK-Sender or Backup ACK-Sender.

When the application is a telephone adjunct box and there is no telephone hybrid / speech IC, for both devices the GS2 op-amp should be connected as a voltage follower to the output of the GS1 op-amp as shown in Figure 1. Then for the MT88E46, when the GS1 or GS2 op-amp is selected the proper algorithm will also be selected, as in the telephone set case.

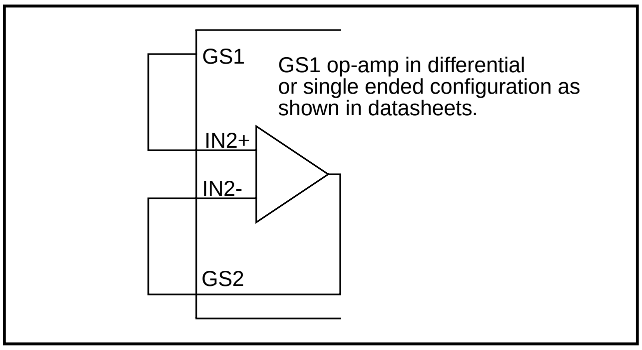


Figure 1 - GS2 Op-Amp Connected as GS1 Voltage Follower

3.0 Pinout Difference

Three pins are different between the MT88E46 and MT88E45, as shown in Table 2.

For both devices, when CAS detection is selected pin 11 is the output which indicates that CAS has been detected. The output signals are named differently because they have different timing characteristics (see 'CAS Detection Timing Overview' section).

If the application firmware is interrupt driven, pin 11 should be connected to the microcontroller's interrupt input. If pin 11 shares the interrupt input with other devices, then pin 11 should also be connected to the input port of the microcontroller so that it can be read to determine whether the device is the interrupt source. If the firmware is poll driven, pin 11 should be connected to the input port of the microcontroller.

If the device is the only interrupt source, and the design is targeted to use the MT88E45 only or the MT88E46 only, the firmware schemes described in this application note do not require pin 11 to be read.

If the design is targeted to use either device interchangeably, then pin 11 must be read by the CAS detection firmware.

Pin #	Name	Description
		MT88E46
11	$\overline{DR}$/$\overline{DET}$	**3-wire FSK Interface Data Ready / CAS Detect (CMOS Logic Output).** Active low. This is a dual purpose pin which indicates the end of an FSK word or the end of CAS. **Data Ready:** Same as MT88E45. **CAS Detect:** When CAS detection is enabled, this pin goes low after the end of CAS for 416±1µs to indicate that CAS has been detected.
12	IC	**Internal Connection.** Must be left open circuit.
13	NC	**No Connection.** This pin is not bonded to the die and is unaffected by external connections.
		MT88E45
11	$\overline{DR}$/$\overline{STD}$	**3-wire FSK Interface Data Ready / CAS Detection Delayed Steering (CMOS Logic Output).** Active low. **Data Ready:** Same as MT88E46. **CAS Detection Delay Steering:** When CAS detection is enabled, this pin is the Delayed Steering Output. It goes low to indicate that a time qualified CAS has been detected.
12	EST	**CAS Detection Early Steering (CMOS Output).** Active high. This pin is the raw CAS detection output. It goes high to indicate the presence of a signal meeting the CAS accept frequencies and signal level. It is used in conjunction with the ST/GT pin and external components to time qualify the detection to determine whether the signal is a real CAS.
13	ST/GT	**CAS Detection Steering/Guard Time (CMOS Output/Analog Input).** It is used in conjunction with the EST pin and external components to time qualify the detection to determine whether the signal is a real CAS.

Table 2 - Differences between the MT88E46 and MT88E46 Pinouts

The MT88E45 pins 12 and 13 are connected to the external guard time components. The MT88E46 pin 12 must be left open circuit and pin 13 is not affected by external connections. When the design is manufactured using the MT88E46, these requirements can be met by simply omitting the guard time components from the circuit board.

4.0 CAS Detection Timing Overview

When CAS detection is selected, in both devices pin 11 is the output which indicates that CAS has been detected. Because of the different CAS detector designs, the pin 11 output signals $\overline{DET}$ (MT88E46) and $\overline{STD}$ (MT88E45) have different timing characteristics. Both indicate that CAS has been detected, but the MT88E46 $\overline{DET}$ is a fixed duration pulse (416±1µs) which indicates that the end of CAS has been detected (see Figure 2), whereas the MT88E45 $\overline{STD}$ goes low while CAS is still on-going and returns to high after CAS has ended (see Figure 3a).

GR-30-CORE Issue 1 specifies that at the central office, the DTMF receiver which is used to detect the ACK from the CPE is connected to the line card right after the central office has finished transmitting CAS. The DTMF receiver remains connected for up to 165ms. To work with the GR-30-CORE central office timing, SR-TSV-002476 Issue 1 requires the CPE to start transmitting ACK within 100ms after the end of CAS as measured on Tip/Ring. Therefore, the end of CAS must be detected within 100 ms after the end of CAS as seen on Tip/Ring. Note that SR-TSV-002476 Issue 1 states that the CPE should ACK only when there is no parallel off-hook extension.

When more than one CPE is off-hook, the MEI (Multiple Extension Interworking) protocol in TIA/EIA-777 allows one CPE to ACK when all off-hook CPEs are MEI compatible, so that all CPEs will receive the CIDCW information. Telcordia (formerly Bellcore) has indicated that MEI will be incorporated into its future standards. The following MEI description from TIA/EIA-777 Issue 1 has been provided for convenience only. The CPE designer must consult the relevant standards to obtain the current requirements.

MEI introduces the concept of the ACK-Sender and the Backup ACK-Sender. The ACK-Sender is the

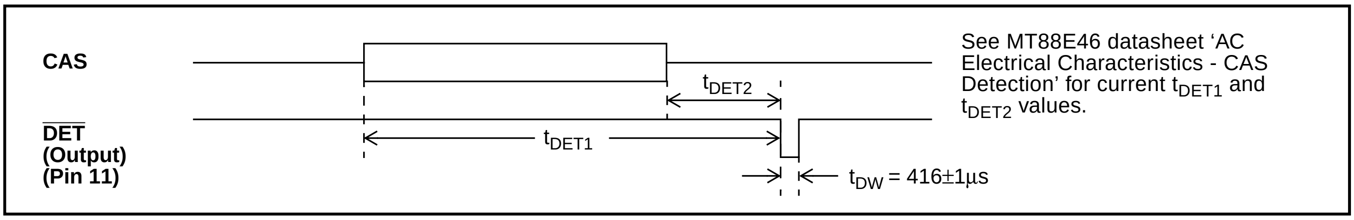


Figure 2 - MT88E46 CAS Detector Output Timing

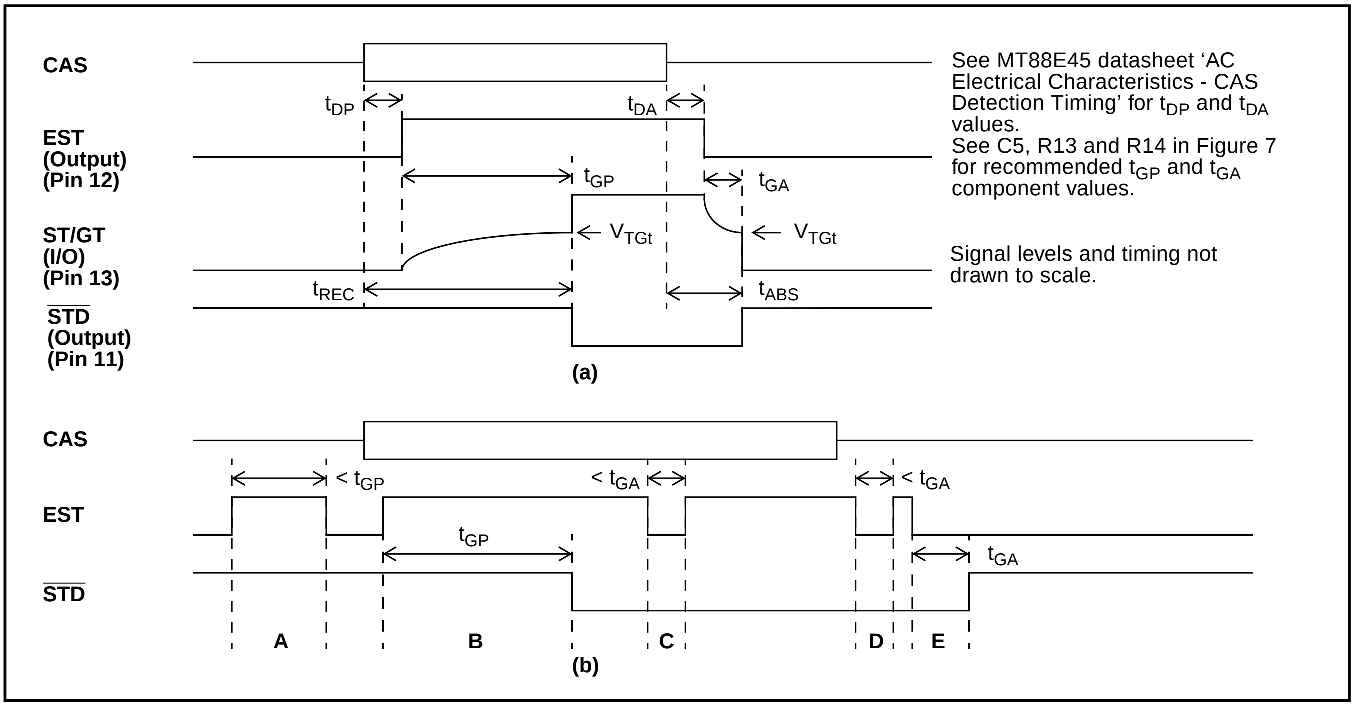


Figure 3 - MT88E45 CAS Detector Output Timing

single CPE that completes the CAS-ACK handshake and terminates the line during FSK data transmission.

- On a per call basis, the ACK-Sender is the first CPE to go off-hook for the call. <u>It retains its status even if it returned on-hook while the line remains in use.</u> The ACK-Sender must give up its status if a Type 3 (Analog Display Services Interface) CPE asserts its ACK-Sender status.
- The Backup ACK-Sender is the CPE to last respond to CAS with an ACK and successfully received FSK data. It retains its status from call to call but must give up its Backup ACK-Sender status when another CPE successfully completes the CAS-ACK-FSK sequence.

The MEI CAS-ACK handshake rules are as follows (slightly paraphrased):

1. Each off-hook CPE shall proceed to the on-hook state not earlier than 25ms and no later than 60ms after the end of CAS as measured on the Tip & Ring interface.
[An explanatory note states that the 25ms delay is necessary to prevent the electrical transients caused by the off-hook CPE's going on-hook from corrupting the CAS for other CPE that may not have completely qualified the signal. The additional 35ms that defines the 60ms upper limit allows for variation in CAS detection delay. In this application note, the 25ms delay will be referred to as the 'non-interference delay'.]
2. After detecting a line HIGH state [the line voltage when the line is not terminated by any CPE], the ACK-Sender shall go off-hook. The ACK-Sender shall allow the line to remain in the HIGH state for at least 5ms but not more than 8ms. If no line HIGH state is detected within 100ms after going on-hook, all previously off-hook CPE shall return to the off-hook state.
3. Following a CAS the Backup ACK-Sender shall monitor the line for a line HIGH state lasting a minimum of 15ms. Once this condition has been detected, the Backup ACK-Sender shall immediately become the ACK-Sender, go off-hook no later than 20ms after the start of the line HIGH state,

complete the CAS-ACK handshake, and remain as ACK-Sender for the remainder of the call. This situation may happen if the designated ACK-Sender is not MEI compliant.

4. An MEI compliant CPE that is not the designated ACK-Sender or the Backup ACK-Sender but which is off-hook at the time of the CAS, shall monitor the line for a line HIGH state lasting a minimum of 30ms. Once this condition has been detected, the CPE shall immediately become the ACK-Sender, go off-hook no later than 35ms after the start of the line HIGH state, complete the CAS-ACK handshake, and remain as ACK-Sender for the duration of the call. This situation can happen if the designated ACK-Sender and the Backup ACK-Sender are not MEI compliant.
5. After going off-hook the ACK-Sender shall begin transmission of the ACK no earlier than 30ms and no later than 40ms after the leading edge of the line HIGH voltage transition.
6. All CPE, regardless of their prior CPE state, shall be ready to receive the start of FSK data 85ms to 605ms after the leading edge of the line HIGH voltage transition.
7. All CPE shall return to their previous state and be ready to receive CAS (on-hook or off-hook) within 50ms after the end of reception of data.
8. If data transmission does not begin within 605ms from the start of the line HIGH pulse all CPE shall return to their previous state and be ready to receive CAS within 50ms.
9. All CPE shall monitor the line while on-hook or off-hook to receive Caller ID messages to maintain a consistent call log.

After stating the rules, TIA/EIA-777 goes on to state that "... the CAS-ACK handshake protocol allows for up to 35ms of CAS detection delay and signal extension after the true end of CAS. It also allows for up to 25ms of signal shortening." Therefore, for MEI the end of CAS must be detected within 35ms after the true end of CAS, whereas in SR-TSV-002476 the CPE has up to 100ms, minus the time needed for the parallel off-hook CPE check, to detect the end of CAS.

5.0 MT88E46 CAS Detection Timing

The MT88E46 ‘on-hook mode’ and ‘off-hook mode’ use different CAS timing qualifications. Both are completely internal and require no external components. $\overline{DET}$ is the only CAS detector output and indicates that the end of CAS has been detected (see Figure 2). $\overline{DET}$ is a fixed duration 416µs low going pulse which ought to be long enough for the application’s microcontroller to react.

Normally $\overline{DET}$ goes low within t_{DET2} after CAS has ended. However, because of speech interference (speech includes music in this context), the detected CAS may be shortened or extended. When the detected CAS is shortened, $\overline{DET}$ may go low before the true end of CAS but both the on-hook and off-hook mode algorithms ensure that $\overline{DET}$ will occur no earlier than t_{DET1} after the beginning of CAS (t_{DET1} = 60ms minimum in the Issue 1 datasheet).

When speech interference causes the detected CAS to be extended, $\overline{DET}$ may go low later than t_{DET2} after the true end of CAS. The off-hook mode algorithm ensures that $\overline{DET}$ will occur no later than 35ms after the end of CAS even with speech interference. In on-hook mode, although the algorithm does not limit the detection delay from the end of CAS, talkdown typically meets the SR-TSV-002476 talkdown condition 1 (the average case) when only the detections which occur from the beginning of CAS to up to 35ms after the end of CAS are counted.

In summary, the MT88E46 $\overline{DET}$ is a fixed duration 416µs low going pulse which indicates the end of CAS. When there is no speech interference, it can occur from just after the end of CAS up to t_{DET2}. When there is speech interference, it occurs anywhere from t_{DET1} after the beginning of CAS to up to 35ms after the end of CAS.

5.1 MT88E46 Only Off-hook CPE CAS Detection Firmware

For firmware designed specifically for the MT88E46, when the CPE is off-hook the application’s microcontroller should initiate the CAS-ACK handshake protocol once the $\overline{DET}$ falling edge has been detected. To initiate the handshake, a 25ms timer should be started. If the CPE supports MEI, the timer implements the non-interference delay. If the CPE does not support MEI, the timer implements a delay to ensure that the CAS has truly ended.

If the CPE supports MEI, when the timer has expired the CPE should go on-hook and continue the MEI CAS-ACK handshake. If the CPE does not support MEI, when the timer has expired the CPE should perform the SR-TSV-002476 Issue 1 parallel off-hook extension check and send the ACK when there are no parallel off-hook CPEs. Note that to comply with TIA/EIA-777, the CPE must support MEI. Telcordia has also indicated that MEI will be incorporated into its future standards.

The $\overline{DET}$ falling edge can be detected by either interrupting the microcontroller with the $\overline{DET}$ falling edge or by the microcontroller polling the $\overline{DET}$ pin. When the MT88E46 is the only interrupt source, the microcontroller does not need to read $\overline{DET}$ because the interrupt itself tells the microcontroller that the end of CAS has been detected. For MEI, the CPE needs to monitor the line HIGH state only after the CPE has gone on-hook upon expiration of the 25ms non-interference delay.

When there is no speech interference, after the 25ms delay the CPE will go on-hook between 25ms (when t_{DET2} = 0) and 25ms + 15ms (15ms is the maximum t_{DET2} from the Issue 1 datasheet) after the end of CAS as measured on Tip/Ring. Thus the CPE timing meets the MEI rule 1 requirement.

When there is speech interference, the detected CAS may be extended. The off-hook mode algorithm ensures that $\overline{DET}$ will go low within 35ms after the true end of CAS. Thus after the 25ms delay, the CPE will go on-hook between 25ms to 60ms after the true end of CAS, as required by MEI rule 1.

When there is speech interference, the detected CAS may be shortened. The intent of the 25ms non-interference delay in MEI rule 1 is to ensure that even if the detected CAS is shortened, the off-hook CPE will go on-hook after the end of CAS as measured on Tip/Ring, so that the transients caused by the CPE going on-hook will not corrupt the CAS for other CPEs which may not have completely qualified the signal. The MT88E46 ensures that when the detected CAS is shortened, $\overline{DET}$ will occur after t_{DET1} (60ms minimum in the Issue 1 datasheet) from the start of CAS. Thus when the CAS duration is at minimum (75ms) and t_{DET1} is also at minimum (60ms), $\overline{DET}$ will occur 15ms before the true end of CAS. After the 25ms delay, the CPE will go on-hook 10ms after the true end of CAS. When the CAS duration is at maximum (85ms) and t_{DET1} is at minimum (60ms), $\overline{DET}$ will occur 25ms before the true end of CAS. After the 25ms delay, the CPE will go on-hook at or after the true end of CAS. Since at worst the CPE goes on-hook right at the true end of CAS, the on-hook transition will not corrupt the CAS because CAS has already ended. Therefore the $\overline{DET}$ timing meets MEI rule 1.

If the CPE does not support MEI, the microcontroller should wait 25ms after the $\overline{DET}$ falling edge to ensure that CAS has truly ended. After the delay, a test should be made to determine whether there is any other off-hook CPE. If the CPE is the only one off-hook, then the CPE should ACK.

There is no need for any external CAS detection qualification. The speech immunity test results reported in the datasheet were obtained by simply counting the number of detections indicated by $\overline{DET}$. There is also no need to implement the MT88E45 ‘clustered imitation consolidation algorithm’ described later since the MT88E46 off-hook mode talkoff test result does not have any clustered imitations. If the consolidation algorithm is implemented, the MT88E46 speech immunity performance will not be affected.

6.0 MT88E45 CAS Detection Timing

Figure 3 shows the MT88E45 CAS detector signals. EST and ST/GT are intermediate signals. $\overline{STD}$ is the final CAS detector output. EST goes high when both tones of a dual tone input meet the CAS frequencies and minimum signal level characteristics. Then a ‘guard time’ circuit comprising of external RC and the ST/GT pin is used to qualify the duration of the EST output. When both tones have been detected continuously for t_{GP} set by the guard time circuit (i.e. after EST has been high continuously for t_{GP}), the final CAS detector output $\overline{STD}$ goes low to indicated that CAS has been detected. When one of the tones or both tones has stopped, $\overline{STD}$ returns to high after a delay (t_{ABS}) to indicate that CAS has ended.

Figure 3b shows the relationship between the MT88E45 EST and $\overline{STD}$ signals. When both tones are detected momentarily, such as caused by speech imitation (speech includes music in this context), EST goes high but if the duration is less than t_{GP} (interval A in Figure 3b), the detection is rejected and $\overline{STD}$ stays high. When both tones have been detected continuously (i.e. EST high continuously) for t_{GP} (interval B), $\overline{STD}$ goes low to indicate that CAS has been detected. Once $\overline{STD}$ has become low, momentary EST dropouts such as when CAS is interfered by speech, are tolerated and $\overline{STD}$ will stay low if the dropouts are less than t_{GA} (interval C). At the end of CAS, sometimes speech will cause spurious EST activities. If the time between the spurious activities is less than t_{GA} (interval D), $\overline{STD}$ will not return high and the detected end of CAS will be delayed. $\overline{STD}$ returns high only after EST has been continuously low for t_{GA} (interval E).

The longer t_{GP} is, the harder it is for speech to imitate CAS. Conversely, if t_{GP} is long, detection of a valid CAS which is corrupted by speech is more difficult. Therefore a long t_{GP} improves talkoff but degrades talkdown. It is a trade-off. For optimal speech immunity, it is recommended that t_{GP} be set to 66ms (R13 = 825K, C5 = 0.1µF in Figure 7). Once $\overline{STD}$ has gone low, a longer t_{GA} tolerates EST dropouts better. However a longer t_{GA} increases the likelihood of the detected end of CAS (i.e. the $\overline{STD}$ rising edge) being delayed.

6.1 MT88E45 Clustered Imitation Consolidation Algorithm

In the Bellcore speech test material, some musical passages generate imitations which occur within a short interval, usually within 2 seconds. That is, the imitations are clustered together. The clustered imitations can be consolidated into a single imitation, hence improving the talkoff test result, by adopting the following simple algorithm.

When CAS is detected, start a 2 second window after the $\overline{STD}$ rising or falling edge. Further detections which occur in the window are to be ignored. A detection within the window should restart the window. After the window has expired successfully, the microcontroller would accept further CASes.

In CIDCW, if the first CAS is not acknowledged, the central office will send another after 10 seconds. Therefore real CASes are at least 10 seconds apart and the application will not be affected by the algorithm.

This algorithm should be implemented especially if t_{GA} is short. In a clustered imitation situation, the EST pulses tend to be quite long and are separated by short dropouts. Since a short t_{GA} is less effective in tolerating EST dropouts, a long imitation will tend to be broken up into a number of shorter imitations and the number of imitations will be increased.

6.2 MT88E45 Only Off-hook CPE CAS Detection Firmware

If the CPE supports MEI, the end of CAS must be identified within 35ms after the true end of CAS so that after a 25ms non-interference delay, the CPE will go on-hook no later than 60ms after the true end of CAS.

If the CPE does not support MEI, the CPE needs to detect CAS only when itself is off-hook. The time available to identify the end of CAS is 100ms minus the time needed for the SR-TSV-002476 Issue 1 parallel off-hook CPE check. Therefore the CPE has more time to detect the end of CAS. Note that to comply with TIA/EIA-777, the CPE must support MEI. Telcordia has also indicated that MEI will be incorporated into its future standards.

For firmware designed specifically for the MT88E45, the off-hook CPE can use the following scheme to identify the end of CAS regardless of whether MEI is supported. In this scheme, the firmware does not rely on the $\overline{STD}$ rising edge to identify the end of CAS. Instead, the end of CAS is determined simply as a fixed delay after the $\overline{STD}$ falling edge. Any value of t_{GP} and t_{GA} can be used.

Figure 4 shows the timing. At the $\overline{STD}$ falling edge, the firmware starts a timer to expire after an (85ms - t_{GP}) interval. The end of CAS is determined as when the timer has expired (Time A in Figure 4a and b). At that time (Time A), a 25ms delay timer should be started. If the CPE supports MEI, the delay is the non-interference delay. If the CPE does not support MEI, the delay ensures that CAS has truly ended. The (85ms - t_{GP}) delay and the 25ms delay can be added together and implemented as a single delay starting at the $\overline{STD}$ falling edge.

The maximum CAS duration is 85ms. At the $\overline{STD}$ falling edge, an interval $t_{REC} = t_{DP} + t_{GP}$ has already elapsed with respect to the beginning of CAS. Thus even for a maximum duration CAS the true end of CAS must have occurred at (85ms - t_{GP}) after the $\overline{STD}$ falling edge. Hence the end of CAS can be determined simply as (85ms - t_{GP}) after the $\overline{STD}$ falling edge.

When the CAS duration is 75ms, the non-interference delay expires at least 35ms after the true end of CAS as shown in Figure 4a. When the CAS duration is 85ms, the non-interference delay expires at least 25ms after the true end of CAS as shown in Figure 4b. Therefore this scheme meets the MEI rule 1 timing.

When the 25ms timer has expired, if MEI is supported the CPE should go on-hook and proceed with the MEI CAS-ACK handshake; if MEI is not supported the CPE should proceed with the parallel off-hook CPE check and complete the SR-TSV-002476 Issue 1 CAS-ACK handshake.

Since the firmware does not rely on the $\overline{STD}$ rising edge to indicate the end of CAS, the firmware does not need to read the $\overline{STD}$ signal. Furthermore, since it does not matter whether the $\overline{STD}$ rising edge is delayed by speech interference after the true end of CAS, any t_{GA} can be used. Figure 4 shows the timing for t_{GP} = 66ms, but any value of t_{GP} can be used.

In an interrupt driven application, the microcontroller should be interrupted by the $\overline{STD}$ falling edge. If the MT88E45 is the only interrupt source, the

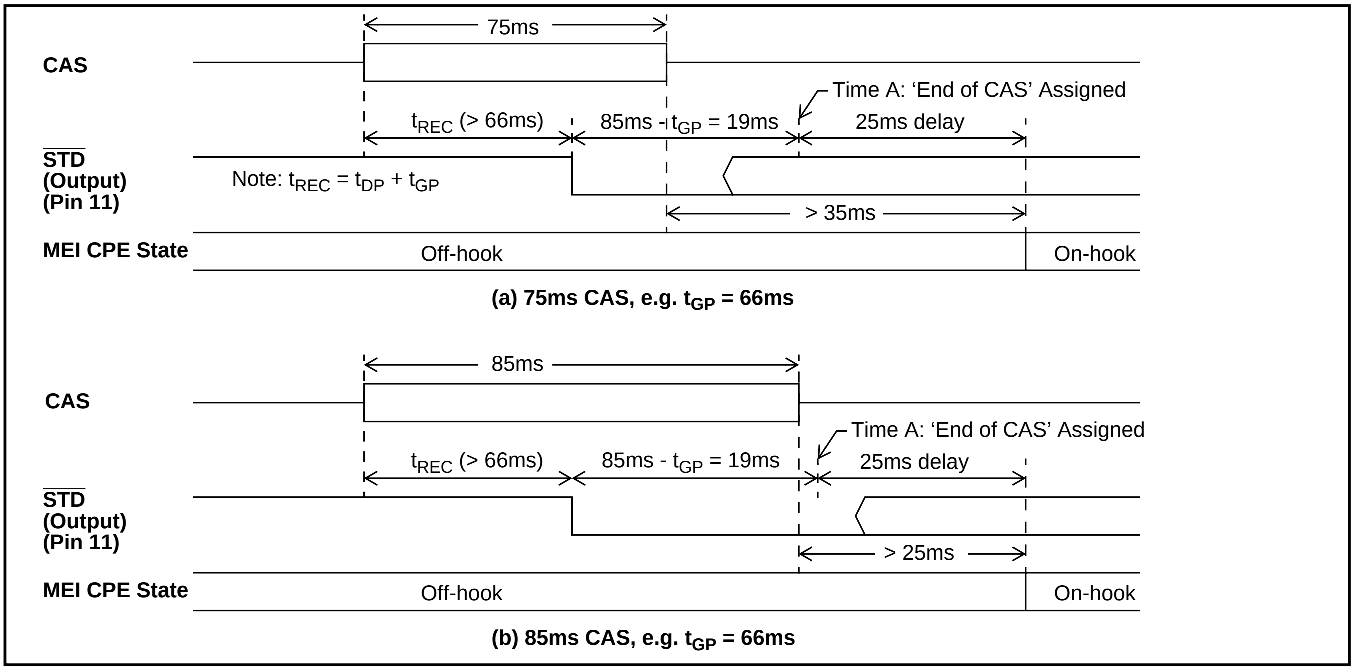


Figure 4 - MT88E45 Off-hook CPE CAS Detection Timing

microcontroller does not even need to read the $\overline{\text{STD}}$ signal to identify the MT88E45 as the interrupt source. In an application which is not interrupt driven, the microcontroller polls the $\overline{\text{STD}}$ signal and looks for the falling edge.

7.0 MT88E45 and MT88E46 Compatible Off-hook CPE CAS Detection Firmware

This section provides an example on how to design the CPE firmware so that it will operate transparently between the MT88E46 and MT88E45. Specifically, the example shows how the firmware should process the CAS detection output from both devices in the off-hook CPE situation, regardless of whether the CPE supports MEI or not. Note that to comply with TIA/EIA-777, the CPE must support MEI. Telcordia has also indicated that MEI will be incorporated into its future standards.

In this method, the starting point of the firmware is the MT88E46 $\overline{\text{DET}}$ / MT88E45 $\overline{\text{STD}}$ falling edge. Both signals are at pin 11 when CAS detection is selected. After the falling edge has occurred, the firmware monitors the $\overline{\text{DET}}$ / $\overline{\text{STD}}$ signal and identifies the end of CAS as the earlier of one of two events: either the $\overline{\text{DET}}$ / $\overline{\text{STD}}$ rising edge, or at a time (85ms - t_{GP}) after the $\overline{\text{DET}}$ / $\overline{\text{STD}}$ falling edge if the rising edge has not occurred by that time. The MT88E45 t_{GP} should be 66ms, t_{GA} can be long or short.

For the MT88E45, the first event corresponds to the normal situation where the end of CAS is not extended by speech interference and the end of CAS is simply indicated by the $\overline{\text{STD}}$ rising edge. The second event corresponds to the situation where the end of CAS is delayed by speech interference and the $\overline{\text{STD}}$ rising edge is delayed. For the second event, since the maximum CAS duration is 85ms and t_{REC} ($t_{REC} = t_{DP} + t_{GP}$) has already elapsed when $\overline{\text{STD}}$ goes low, the true end of CAS must have already occurred when the (85ms - t_{GP}) time limit expires. At that time, the firmware should give up waiting for the $\overline{\text{STD}}$ rising edge and decide that the end of CAS has occurred.

For the MT88E46, the end of CAS will always be identified as the $\overline{\text{DET}}$ rising edge. This is because the MT88E45 t_{GP} in this scheme is 66ms. The time limit for the second event is (85ms - t_{GP}) = 19ms. Since $\overline{\text{DET}}$ always returns to high 416µs after it went low, the end of CAS will always occur within the time limit and be identified as the $\overline{\text{DET}}$ rising edge.

When the end of CAS has been determined, a 25ms delay timer should be started. If the CPE supports MEI, the delay is the non-interference delay. If the CPE does not support MEI, the delay ensures that the CAS has truly ended. Once the 25ms delay timer has expired, if MEI is supported the CPE should go on-hook and proceed with the MEI CAS-ACK handshake; if MEI is not supported the CPE should check for parallel off-hook CPEs and complete the SR-TSV-002476 Issue 1 CAS-ACK handshake.

The MT88E45 'clustered imitation consolidation algorithm' can also be implemented. The MT88E46 does not need the algorithm but will not be affected by it.

Figure 5 shows the MT88E45 CPE timing under this scheme. In Figure 5a, the CAS duration is at the minimum of 75ms. The $\overline{STD}$ rising edge is delayed by speech. Therefore the 'end of CAS' is identified as (85ms - t_{GP}) after the $\overline{STD}$ falling edge. The 25ms delay timer expires at least 35ms after the true end of CAS and the timing meets MEI rule 1.

In Figure 5b, the CAS duration is at the minimum of 75ms. $\overline{STD}$ is shortened by speech. The 25ms delay timer expires at least 16ms after the true end of CAS. Hence any action taken by the CPE will not corrupt the CAS and the timing meets MEI rule 1.

In Figure 5c, the CAS duration is at the maximum of 85ms. The $\overline{STD}$ rising edge is delayed by speech. The 'end of CAS' is identified as (85ms - t_{GP}) after the $\overline{STD}$ falling edge. The 25ms delay timer expires at least 25ms after the true end of CAS and the timing meets MEI rule 1.

In Figure 5d, the CAS duration is at the maximum of 85ms. $\overline{STD}$ is shortened by speech. The 25ms delay timer will expire at least 6ms after the true end of CAS. Hence any action taken by the CPE will not corrupt the CAS and the timing meets MEI rule 1. The 6ms interval is the closest the end of the 25ms delay will come to the true end of CAS. The 6ms allows for shortened t_{GP} caused by RC component tolerance.

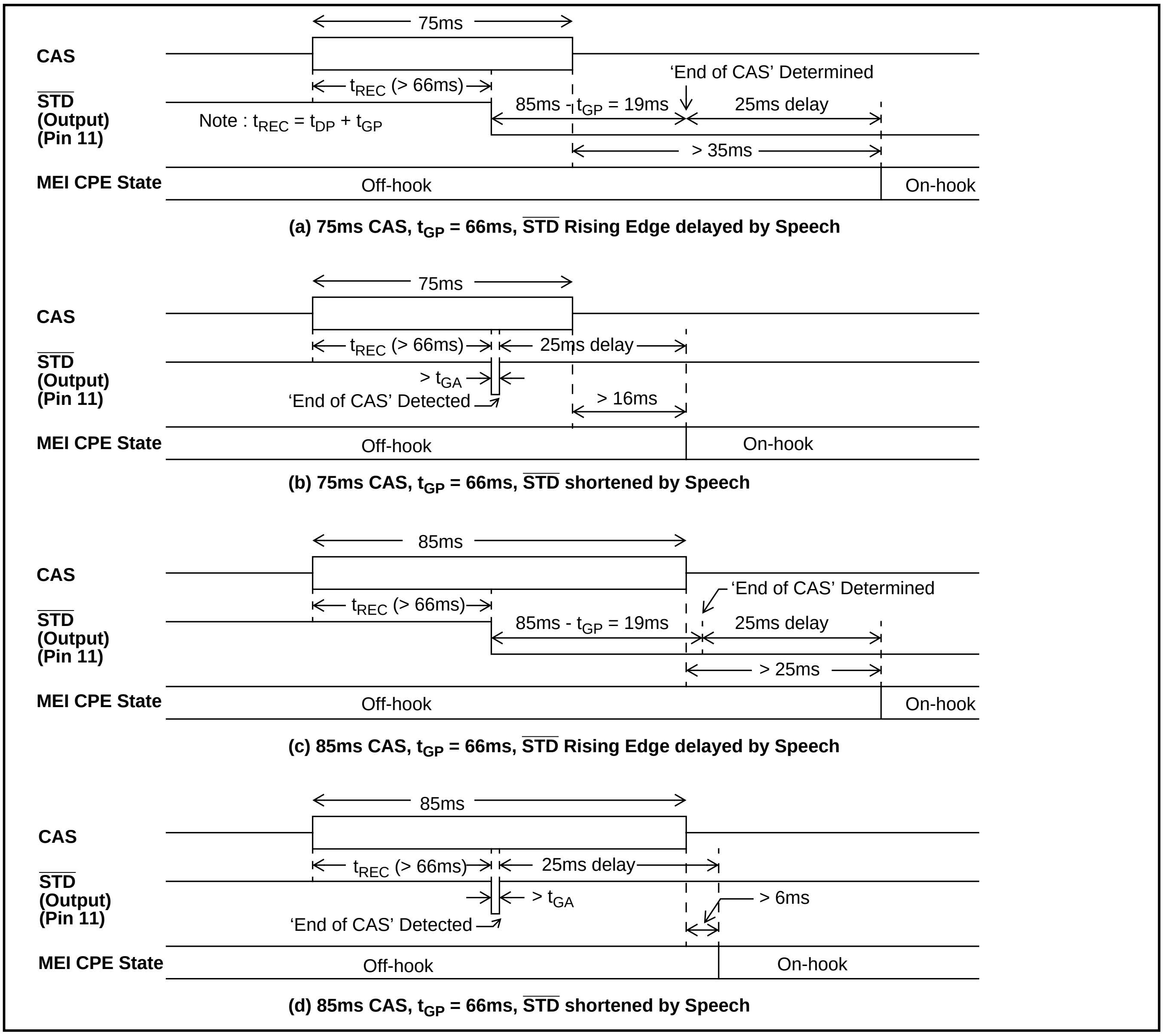


Figure 5 - MT88E45 Off-hook State CPE Timing in MT88E45/E46 Compatible Firmware

Figure 6 shows the MT88E46 CPE timing under this scheme. In Figure 6a, there is no speech interference. $\overline{DET}$ occurs up to 15ms (t_{DET2} max) after the end of CAS. The 25ms delay ends between 25.4 to 40.4ms after the true end of CAS and meets the MEI rule 1 timing.

In Figure 6b, speech interference causes the detected end of CAS to be delayed. $\overline{DET}$ occurs up to 35ms after the end of CAS. The 25ms delay ends between 25.4 to 60.4ms after the true end of CAS. In reality, valid CASes are detected well within 35ms after the true end of CAS. Hence the delay will end before 60ms and meets the MEI rule 1 timing.

In Figure 6c, speech interference causes the detected CAS to be shortened so that the $\overline{DET}$ pulse occurs before the true end of CAS. The CAS duration is at minimum (75ms). Since $\overline{DET}$ occurs at least 60ms after the beginning of CAS, the 25ms delay ends at least 10.4ms after the true end of CAS. In Figure 6d, speech interference also causes the detected CAS to be shortened for the maximum duration CAS (85ms). Since $\overline{DET}$ occurs at least 60ms after the beginning of CAS, the 25ms delay ends 0.4ms after the true end of CAS. In both cases, the delay ends after the true end of CAS. Hence the MEI CPE's going on-hook will not corrupt the CAS for other CPEs and the timing meets MEI rule 1.

For this method to work properly, the microcontroller must monitor the $\overline{DET}$ / $\overline{STD}$ output after its falling edge. The firmware must not determine the end of CAS just as (85ms - $t_{GP,}$ t_{GP} = 66ms) after the $\overline{DET}$ / $\overline{STD}$ falling edge and ignore the $\overline{DET}$ / $\overline{STD}$ rising edge occurring during that interval. Otherwise the

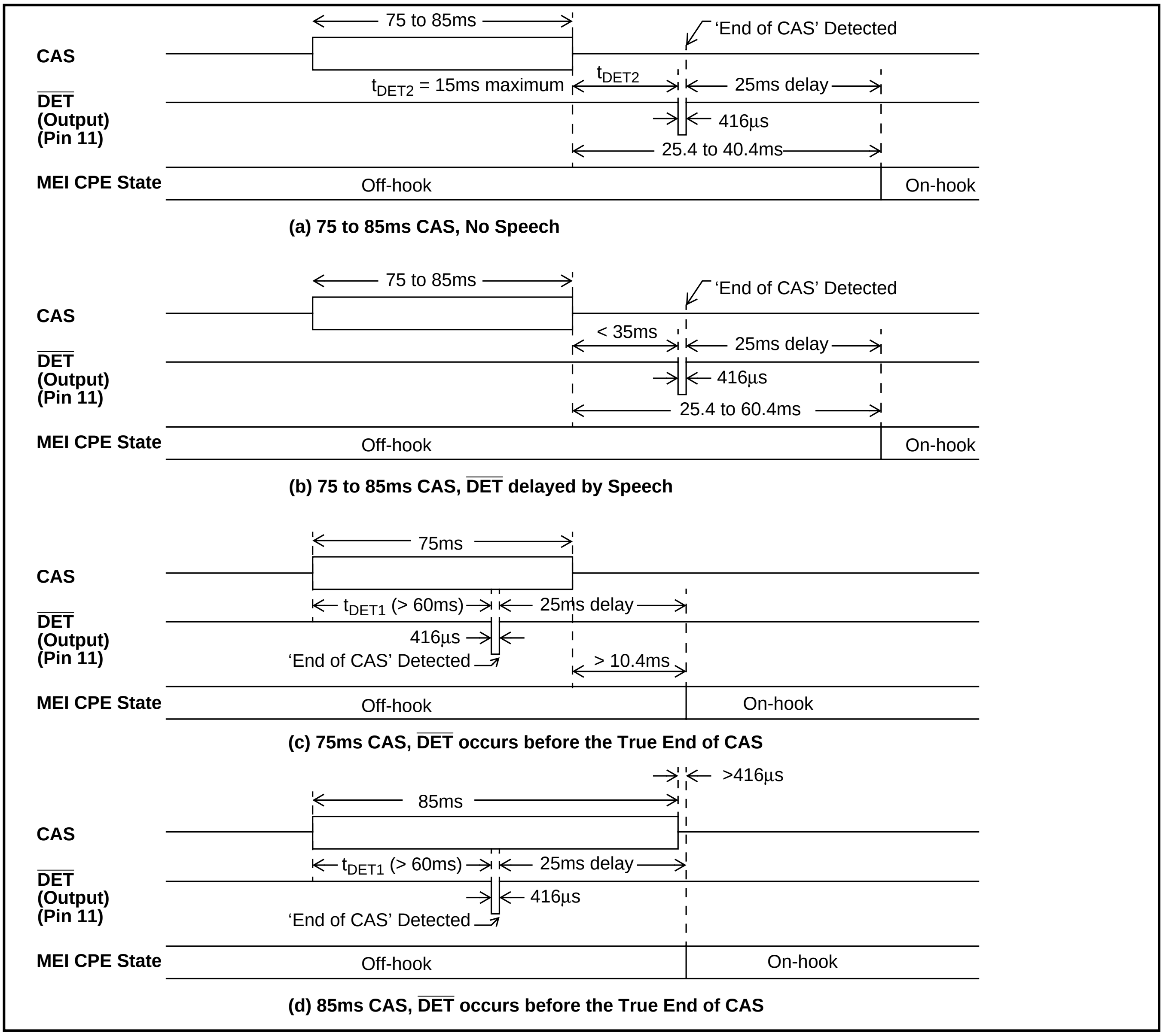


Figure 6 - MT88E46 Off-hook State CPE Timing in MT88E45/46 Compatible Firmware

design will not work properly when it is manufactured with the MT88E46. When interfered by speech the MT88E46 DET falling edge can occur up to 35ms after the true end of CAS. If the microcontroller ignores the DET rising edge and always starts the 25ms timer at (85ms - t_{GP}) after the falling edge, then when DET is delayed 35ms the CPE will go on-hook at 79ms after the true end of CAS (35ms + 85ms - t_{GP} + 25ms, t_{GP} = 66ms) and exceed the 60ms limit allowed in the MEI CAS-ACK handshake.

This scheme will work in an MT88E45 only design whose t_{GP} is shorter, but the 25ms delay timer should be increased to (25ms + 66ms - t_{GP}) so that in the Figure 5d situation, the delay will still end after the true end of CAS. But in an MT88E46/E45 compatible design, because the MT88E46 needs a 25ms delay in the Figure 6d situation, the MT88E45 t_{GP} should be 66ms.

The starting point of the off-hook CAS detection firmware can be detected by interrupting the microcontroller with the DET / STD falling edge, or the microcontroller can poll the DET / STD signal. In both cases, the DET / STD signal should be connected to the microcontroller input port so that the status of the signal can be monitored during the (85ms - t_{GP}) interval.

8.0 MT88E46 Compatibility with Other Commonly Used MT88E45 Off-hook CPE CAS Detection Firmware

Some MT88E45 designs qualify the duration of the STD output to improve talkoff. In this method, t_{GA} is set to 1 or 2ms so that the end of CAS as indicated by the STD rising edge is not extended by speech. After STD has gone low, the near end speech is not muted but the firmware monitors the duration of the STD low pulse. If the duration is too long, the detection is rejected as an imitation. Since the MT88E46 DET is only 416µs long, a detection by the MT88E46 will pass the duration test and the firmware will work with both devices transparently.

Some MT88E45 designs use a ‘CAS Mute Check’ method. In this method, a short t_{GP} is set. When STD goes low, the microphone is muted or attenuated. The firmware then monitors the STD output to see whether STD still indicates detection. If STD returned high shortly after the microphone has been muted / attenuated, the detection is considered an imitation and rejected because it was probably caused by the near end speech from the microphone. The MT88E46 will not work properly with this method. Since DET is only 416µs long, all MT88E46 detections will be classified as an imitation. But with the MT88E46’s much better speech immunity, this method is also no longer necessary. When the design is manufactured using the MT88E46, the microcontroller firmware must bypass the muting and checking. This can be accomplished, for example, by the microcontroller’s reading an external status bit to determine whether to do the CAS mute check, or by loading the microcontroller with the proper firmware.

9.0 MT88E45 and MT88E46 On-hook CPE CAS Detection Firmware

This section describes the MEI CPE CAS detection firmware when the CPE itself is on-hook but the line is in use. It is suitable for both the MT88E46 and MT88E45.

The firmware should determine that CAS has been detected when the DET / STD falling edge occurs. Once CAS has been detected, there is no need to start the 25ms non-interference timer because the CPE itself is already on-hook. The CPE should monitor the line voltage for the HIGH state. To be responsive, the CPE should continuously monitor the line voltage for the HIGH state regardless of whether CAS has been detected.

If the CPE is the ACK-Sender, after it detected CAS the CPE should go off-hook at least 5ms after the leading edge of the line HIGH voltage transition. The CPE should ensure that the line is in the HIGH state for no more than 8ms. It should then start sending ACK between 30 to 40ms after the leading edge of the line HIGH transition. After the end of ACK, it should prepare to receive FSK.

If the CPE is the Backup ACK-Sender, after it detected CAS and the line has been in the HIGH state for at least 15ms after the leading edge of the line HIGH transition, the CPE should take over as the ACK-Sender and go off-hook so that the line is in the HIGH state for no more than 20ms. It should then send ACK and prepare to receive FSK as in the ACK-Sender case.

If the CPE is neither the ACK-Sender nor the Backup ACK-Sender, after CAS has been detected the CPE should prepare to receive FSK at 85ms after the leading edge of the line HIGH transition. The 85ms is composed of the 30ms minimum line HIGH to ACK delay and the 55ms minimum ACK duration. If the ACK-Sender delays the ACK to 40ms after the line HIGH transition and sends the maximum duration ACK (65ms), this CPE’s FSK demodulator will see the tail of the ACK (up to 20ms). The FSK carrier detector may be activated by that portion of the ACK and a few bytes of false data may be generated.

To be responsive, the CPE should always monitor the line voltage when itself is on-hook, regardless of the line status, so that the CPE can determine whether it is the first CPE to go off-hook and assume the ACK-Sender role.

10.0 GS1 and GS2 Gains

For nominal Vdd = 5V, both devices should be configured to 0dB gain at the GS1 and GS2 input op-amps. For nominal Vdd = 3V, the gains are different between the MT88E46 and MT88E45: the MT88E46 GS1 and GS2 gains should be -4dB, the MT88E45 GS1 and GS2 gains should be -3.5dB.

The MT88E45 minimum CAS detect levels is -37.78dBm. To improve talkoff, some MT88E45 designs may have set the GS2 gain so that the 4-wire side input signal is attenuated more than recommended in the datasheet. The MT88E46 minimum CAS detect level is -32dBm, the GS2 gain should follow the datasheet value.

11.0 Partial Power Down

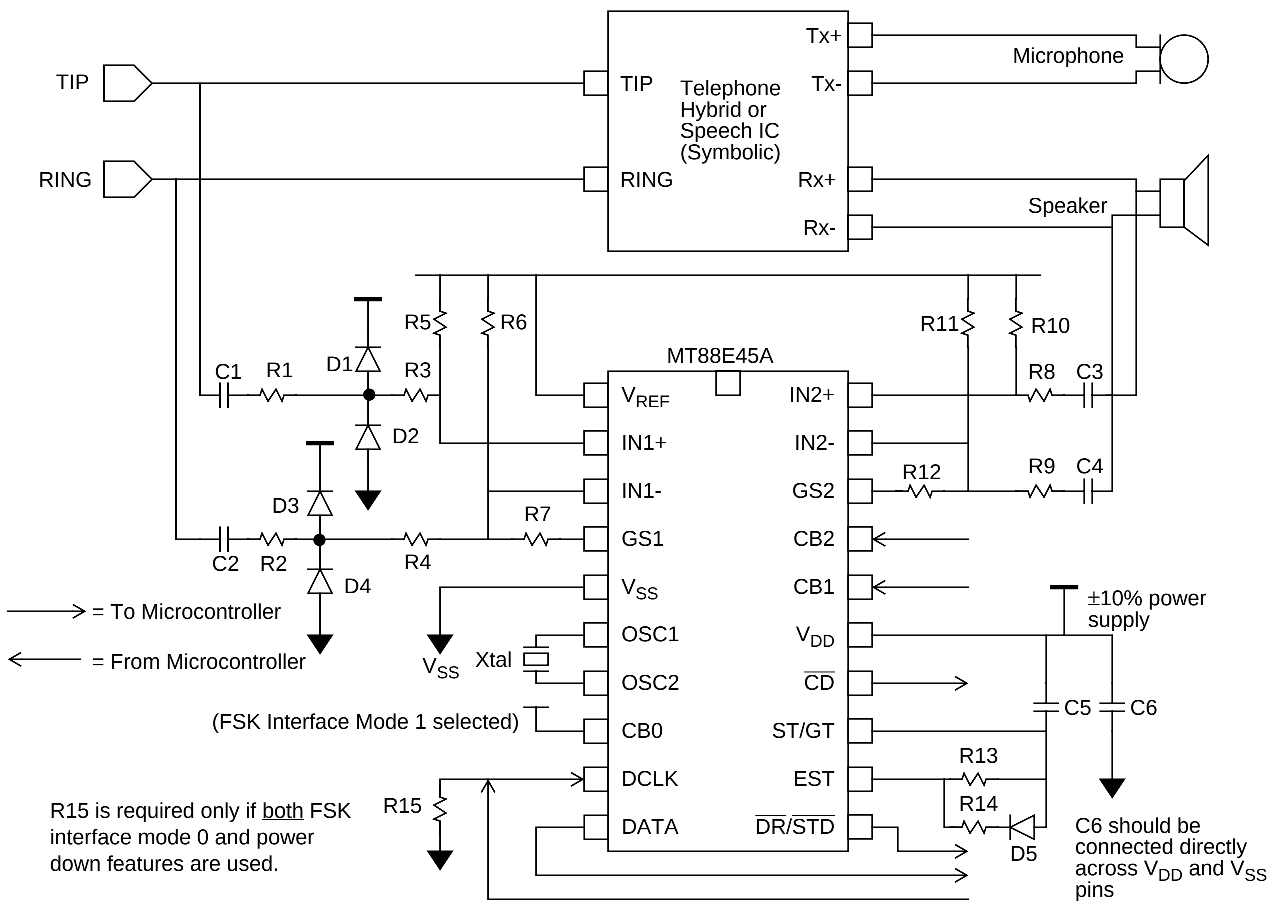
In both devices, the partial power down feature can also be used to reset the FSK or CAS circuits for situations such as system power up. To reset the FSK demodulator, use CB1/2 to select CAS mode for about 10µs, $\overline{DR}$ will become high. To reset the CAS detector, select FSK mode for about 1ms for the MT88E45, about 10µs for the MT88E46, $\overline{DET}$ and $\overline{STD}$ will become high. The MT88E45 requires a longer reset interval to charge the guard time capacitor via the ST/GT pin so that $\overline{STD}$ will stay high after the reset.

12.0 Crystal versus Ceramic Resonator

Although it is unlikely, some MT88E45 applications may have been designed to use a ceramic resonator instead of a crystal. The MT88E46 must be used with a 3.579545MHz clock source which has ±0.1% tolerance. It is unlikely that such tolerance can be provided by a ceramic resonator. Therefore, when the design is manufactured using the MT88E46, it must also be manufactured using a 3.579545MHz ± 0.1% crystal.

13.0 References

MT88E46 Datasheet	Issue 1, Mar 2000
MT88E45 Datasheet	Issue 2, Mar 1999
TIA/EIA-777	"Telecommunications telephone terminal equipment - Type 2 caller identity equipment performance requirements", Nov 1999, Telecommunications Industry Association
SR-TSV-002476	"Customer premises equipment compatibility considerations for the voiceband data transmission interface", Issue 1, Dec 1992, Bellcore (now Telcordia)
GR-30-CORE	"Voiceband data transmission interface", Issue 1, Dec 1994, Bellcore (now Telcordia)



Unless stated otherwise, resistors are 1%, 0.1Watt; capacitors are 5%, 6.3V.

For 1000Vrms, 60Hz isolation from Tip to Earth and Ring to Earth:

R1,R2	430K, 0.5W, 5%, 475V min. (e.g. IRC type GS-3)	C1,C2	2n2, 1332V min.

If the 1000Vrms is handled by other methods then this circuit has to meet the FCC Part 68 Type B Ringer requirements:

R1,R2	432K, 0.1W, 1%, 56V min.	C1,C2	2n2, 212V min.

Common to both sets of R1, R2 and C1, C2:

R3,R4	34K	C3,C4	2n2
R8, R9	464K	C5	100n
R13	825K	C6	100n, 20%
R14	226K or 26K1	D1-D5	Diodes. 1N4148 or equivalent
R15	100K, 20%	Xtal	3.579545MHz, 0.1% crystal or ceramic resonator

V_{DD}	5V±10%
GS1/2 gain	0dB
R5, R10	53K6
R6, R11	60K4
R7, R12	464K

For R13 = 825K, C5 = 100n, t_{GP} = 66ms.
For R13 = 825K, R14 = 226K, C5 = 100n, t_{GA} = 15ms.
For R13 = 825K, R14 = 26K1, C5 = 100n, t_{GA} = 2.3ms.

Figure 7 - MT88E45 Application Circuit

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