1.0   Introduction

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This document details the register configuration settings required to receive and output Ethernet frequencies on the ZL30120/1.

2.0   Configuration of Custom A/B Input Frequencies

The Custom A and B frequencies can be configured to detect frequencies in the range 8 kHz to 77.76 MHz in 8 kHz multiples. Refer to Table 1 for a list of configuration registers and example values for 25 MHz or 50 MHz. For more details as to the calculations of these values, refer to the design manual.

Register Description	Custom Registers		Register Value	
	A	**B**	**25 MHz**	**50 MHz**
Multiple0	0x67	0x71	0x35	0x6A
Multiple1	0x68	0x72	0x0C	0x18
SCM Low	0x69	0x73	0x06	0x03
SCM High	0x6A	0x74	0x12	0x09
CFM Low0	0x6B	0x75	0x37	0x37
CFM Low1	0x6C	0x76	0x06	0x06
CFM High0	0x6D	0x77	0x99	0x99
CFM High1	0x6E	0x78	0x06	0x06
CFM Cycle	0x6F	0x79	0x7f	0xFF
Divide	0x70	0x7A	0x01	0x01

Table 1 - Custom A and B Configuration

3.0   Configuration of SONET/SDH APLL for Ethernet Frequencies

The following sequence of register writes shifts the SONET/SDH APLL's center frequency to Ethernet base frequencies.

```
Write 0x04 to address 0x64
Write 0x7C to address 0x65
Write 0x92 to address 0x66
Write 0x00 to address 0x64
Write 0xBB/0xAA to register 0x52
Write 0x07 to address 0x64
Read register VALUE from address 0x6E
if VALUE <= 0x0B
   NewValue = VALUE + 4
else
   NewValue = 0xFF
Write NewValue to address 0x6E
Write 0x00 to address 0x64
```

After changing the APLL's center frequency to Ethernet base frequencies, SONET/SDH base frequencies are no longer available from the APLL output pins. To return the APLL to SONET/SDH base frequencies, a device reset must be performed.