ZLAN-200

Applications of the ZL30116/121 Master Slave Configuration in ATCA Systems

Application Note

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1.0 Introduction

A common architecture in telecommunications products is comprised of 2 central control cards and multiple line cards that communicate over a common backplane. The control cards will typically include features such as a system control processor, switching fabric and system timing. For the purposes of this application note we will be looking at the system timing architecture of one such system.

The Advance Telecom Computing Architecture (ATCA) is an open standard optimized for next-generation telecommunications equipment. It provides a common platform that allows telecom equipment manufacturers to develop modular and interoperable hardware and software. A carrier grade solution can be developed using standard hardware and software building blocks from a variety of vendors, thereby reducing the cost and development time of telecom equipment.

This application note will discuss an implementation of a redundant timing solution in an ATCA system using a centralized architecture. This timing architecture is commonly called Master/Slave. In this configuration as shown in Figure 1, the Master (Active) Timing card is synchronized to an external network reference and the Slave (Redundant) timing card is synchronized to the Master. The result is 2 sets of identical redundant phase aligned system clocks for use by the system's line cards. In the case of a failure on the Master timing card, the Slave card will seamlessly assume control of the system and become the Master without causing any disruptions to the system.

For an introduction to the ATCA Synchronization interface and it's centralized timing architecture visit the Zarlink website at http://timing.zarlink.com/assets/ATCATimingWhitepaper_Part2.pdf

2.0 Master/Slave Design Considerations ATCA Systems

Figure 1 shows the basic architecture for a redundant centralized timing solution in an ATCA system. It shows 2 Central Timing cards, each containing a ZL30116/121 Network synchronizer, providing a redundant set of system clocks to the ATCA synchronization backplane. The Master Timing card, takes an network reference from either an external source such as a BITS or SSU clock or a clock from one of the CLK3 ATCA buses, which is typically a recovered line clock from one of the systems linecards. The master is responsible for providing all standards compliant network level synchronization. The slave card locks itself to the output of the master card and tracks it, ensuring that the 2 pairs of system clocks remain aligned on the backplane. The main considerations for choosing a timing solution for this application are as follows:

- The Timing Card must be able to be configured as either the master or the slave, it must also be able to seamlessly transition from one to the other without causing disruptions downstream on the linecards.
- The timing card must be able to be configured to drive and receive either the A or B set of system clock buses.
- When operating as a master, the card must be able to provide Stratum 3 level network synchronization.
- When operating as a slave, the card must be able to align its output clock to much the phase of the master clocks within +/-10 ns. It must therefore be able to compensate for the static misalignment caused by buffer and trace delays, as well as the dynamix misalignment caused by jitter/wander and or transients on the master clock.

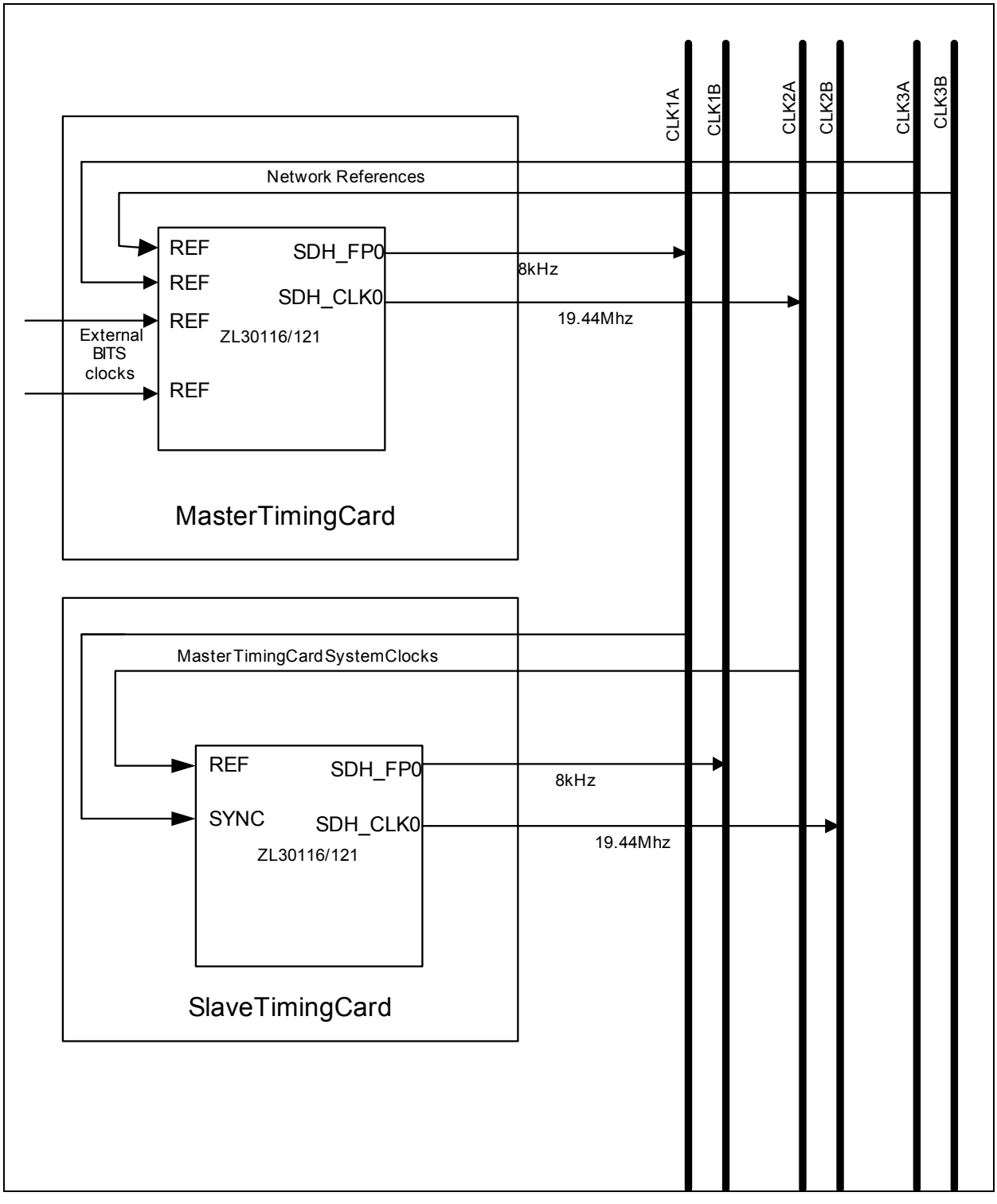

Figure 1 - ATCA Centralized Architecture

3.0 Implementing Redundancy Protection using the ZL30116/121

The design of the central timing cards must be such that the card is able to fulfil the requirements of either the Master or the Slave.

3.1 Features of the ZL30116/121 to Support the ATCA Master Timing Function

The main function of the Master timing Card is to provide complete network synchronization and distribute its standards compliant systems clocks to all the line cards in the system. The ATCA synchronization specification requires that the backplane system clocks conform to Stratum 3 levels at a minimum. The ZL30116/121 provides a fully compliant Stratum 3 timing solution thanks to the following features.

Wander/Jitter Filtering

The Loop bandwidth of the ZL30116/121 can be configured as to meet network synchronization standards, including Stratum 3, as shown in Table 1.

BW (Hz)	Application
0.1	GR-253 SONET Stratum 3, SMC, G.813 Option 2
1.7	GR-1244 Stratum 3, G.813 option 1
3.5	G.813 option 1

Table 1 - ZL30116/121 Loop bandwidth options for the Master Timing Card

Phase Slope Limiting

The ZL30116/121 also provides application specific Phase slope limiter settings used to limit the rate of change of phase on the output clocks, Table 2 show the available options.

Phase Slope Limit	Application
885ns/s	GR-1244 Stratum2, 3E, 3 (objective)
7.5us/s	G.813 option 1
61us/s	GR-1244 Stratum 3
unrestricted	

Table 2 - ZL30116/121 Phase Slope Limiting options for the Master Timing Card

Holdover

In the event that all the available network reference are lost, the Master Timing card must be able to enter its Holdover mode and continue to output valid system clocks until such a time as at least one valid network reference becomes available again. The ZL30116/121 provides an initial holdover accuracy of better than 1 ppb which meets the Stratum 3E requirement. The drift and long-term stability of the holdover clock is dependant on the 20 Mhz oscillator. A oscillator must be chosen in accordance with the targeted application of the system, which in the case of ATCA is Stratum 3. For a list of recommended oscillators refer to ZLAN-68 on the Zarlink timing and synchronization website at www.zarlinktiming.com.

Reference Monitoring and Automatic Hitless Reference Switching

The master timing card should continuously monitor all incoming network references for quality and be able to automatically switch in the event of a failure on one these references. The ZL30116/121 provides 8 input references, and an automatic state machine that will automatically select the proper input reference based on the user defined priority table and the reference quality. The ZL30116/121 also provides extensive reference monitoring that will detect missing clocks, large frequency offsets and a programmable monitor that will detect precise, application specific frequency offsets shown in Table 3.

Acceptance Range	Rejection Range	Typical Application
+/-9.2 ppm	+/-12 ppm	Stratum 3/3E, G.813 option 1
+/-13.8 ppm	+/-18 ppm	
+/-24.6 ppm	+/-32 ppm	
+/-36.6 ppm	+/-47.5 ppm	
+/-40 ppm	+/-52 ppm	SMC, G.813 option 2
+/-52 ppm	+/-67.5 ppm	
+/-64 ppm	+/-83 ppm	Stratum 4, G.824
+/-100 ppm	+/-130 ppm	G.823

Table 3 - Frequency Out of Range Limits for the ZL30116/121

3.2 Features of the ZL30116/121 to Support the Slave Timing Function

The Slave timing card must lock to and monitor the master timing card's system clocks and provide a phase aligned redundant version of those system clocks to the backplane.

High Bandwidth Mode

As mentioned in an earlier section the ZL30116/121 has numerous options for providing network synchronization jitter and wander flittering, but it also provides the option of opening up the bandwidth to 890 Hz that will allow the slave to quickly track any jitter/wander or transients that may appear on the master clocks. This is necessary, since the phase alignment between the master and slave must remain intact even in the presence of high levels of network jitter and wander. If the slave has a low bandwidth then it cannot react quickly to changes on the master and will therefore lag behind and cause phase misalignments that could adversely affect the operation of the linecards.

Ref and Sync pairs

In order to take advantage of the High bandwidth mode of 890 Hz, the input reference frequency must be greater than 8 kHz. This will cause problems in an ATCA system, since there is a requirement to provide phase aligned 8 kHz frame pulse system clocks on the backplane. With the Ref and Sync pair feature of the ZL30116/121 we can synchronize to a high frequency reference clock (19.44 MHz from the CLK2 bus) and still ensure that the frame boundaries of the master and slave are still aligned.

In ATCA the Master and Slave cards are required to output both a 19.44 MHz and a 8 kHz clock on the ATCA sync bus that are phase aligned. Under regular circumstances in order to ensure that both the 19.44 Mhz clocks and the 8 kHz frame pulses are aligned we would have to force the Slave card to synchronize to the 8 kHz frame pulse. However in this configuration, the loop bandwidth is restricted (even in High bandwidth mode) to 56 Hz. Under certain network jitter/wander/transient conditions the Slave card will not be able to track the incoming master clocks quickly enough to maintain the necessary phase alignment. As a result we must synchronize to the 19.44 Mhz clock and utilize the 890 Hz mode, however if we are simply locked to the 19.44 Mhz clock we cannot ensure that the 8 kHz frame pulses are aligned properly. The solution is to use the Ref and Sync pairs.The ZL30116/121

provides 3 Ref and Sync pairs, Sync0 corresponds to it's pair Ref0 and Sync1 to Ref1, etc.... If no valid signal is applied to the Sync input it is ignored and the corresponding Ref signal operates normally. In our example we can now synchronize the slave to the incoming 19.44 Mhz and send the incoming 8 khz clock to the corresponding Sync input. The result is a high bandwidth (890 Hz) PLL that has all of its inputs and outputs (frame pulses include) aligned properly

Reference Monitoring

The Slave card must monitor the qualities the Master system clocks. As discussed earlier the ZL30116/121 has a wide array of frequency monitoring features available to this. I the event that the slave card detects an error on the master clocks it will enter holdover and signal the system controller to begin the process of switching the Slave into the Master Timing card.

Phase Alignment

The ZL30116/121 provides a tight phase alignment between it's inputs and outputs, however in a redundant Master/Slave architecture we must ensure that the Systems clocks are aligned at the back plane, and often times there are other components such buffers, muxes, CPLDs, etc. that introduce delays that will ruin the backplane phase alignment. The ZL30116/121 has 2 available features to help rectify this problem.

Option 1- Output Phase Adjustment

The ZL30116/121 offers a input to output fine delay adjustment. This feature allows you to configure each of the output synthesizers to lag or lead the input reference. You can adjust the output phase in steps of 120 ps from -15.24 nsec to +15.35 nsec. If you calculate all the typical delays in the clock path on the slave card then you can easily program the DPLL to compensate for these delays ensuring that the active and redundant clocks are properly aligned. Figure 1. shows a typical setup where the slave card takes the master system clocks form the back plane. The clocks then must propagate through the TX buffer, RX buffer, PCB traces and the PLL before arriving back at the back plane. If we add up all of the delay elements as in equation 1. then we can program the PLL to delay the output clocks into the appropriate registers (0x3D, 0x4F or 0x55)

$$T_{delay} = T_{PDrxbuffer} + T_{PDrtxtrace} + T_{PDpll} + T_{pdtxtrace} + T_{PDtxbuffer}$$

where,

T_{delay} = Delay programmed into the fine delay adjustment registers

$T_{PDrxbuffer}$ = Typical delay through the Receive Buffer at the backplane.

$T_{PDrtxtrace}$ and $T_{pdtxtrace}$= Typical delay of the traces on your PCB

T_{PDpll} = Typical input to output delay of the ZL30116/121

$T_{PDtxbuffer}$ = Typical delay of the transmit buffer at the backplane

The advantage of this method is its simplicity, it requires only a simple calculation and a couple of registers writes to accomplish the task. Its drawbacks are that it does not dynamically compensate for any variances or changes in the delays. For example, the transmit buffer may have a typical propagation delay of 3 nsec, but over the working temperature and voltage ranges the maximum delay could be significantly higher, say 6 nsec, so your delay calculation will compensate for only the typical case, and under worst case environmental conditions a phase skew between the master and slave clocks could be introduced.

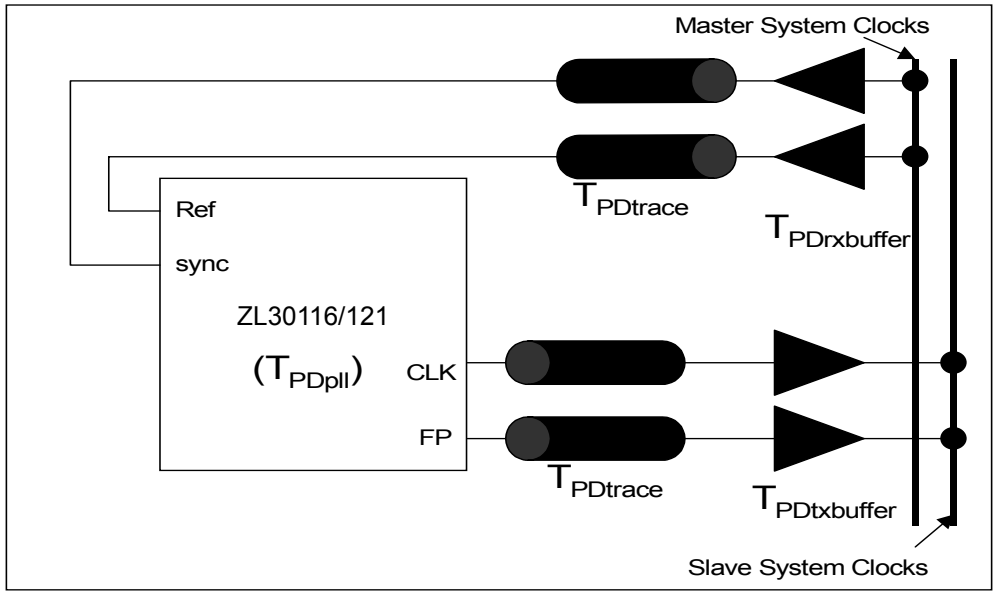

Figure 2 - Delay Path for Slave Timing Card

Option 2 - External Feedback

Another feature available on the ZL30116/121 is an external feedback path for the PLL. Using the ext_fb_clk_en bit of the fb_control register(0x62) the feedback path can be changed to use the external pins ext_fb_fp and ext_fb_clk. By introducing an equivalent delay path in the feedback loop of the DPLL we can essentially create a dynamic compensation for the clock path delays. In our example this would require adding another receive buffer and the matching the rxPCB trace length into the feedback path, see Figure 2 for details. In applications that do not require frame pulse alignment, the only the feedback clock is required

The advantage of this method is that as the environment changes and there are potential changes in the delay of the system clock path, this circuit will dynamically compensate for these changes since the buffers and traces on the feedback path will be experiencing the same operating conditions. The drawback is that the design requires an extra buffer that may take up extra board space. It also requires extra care during layout and component selection since jitter and noise on the feedback path will adversely affect the PLL's performance.

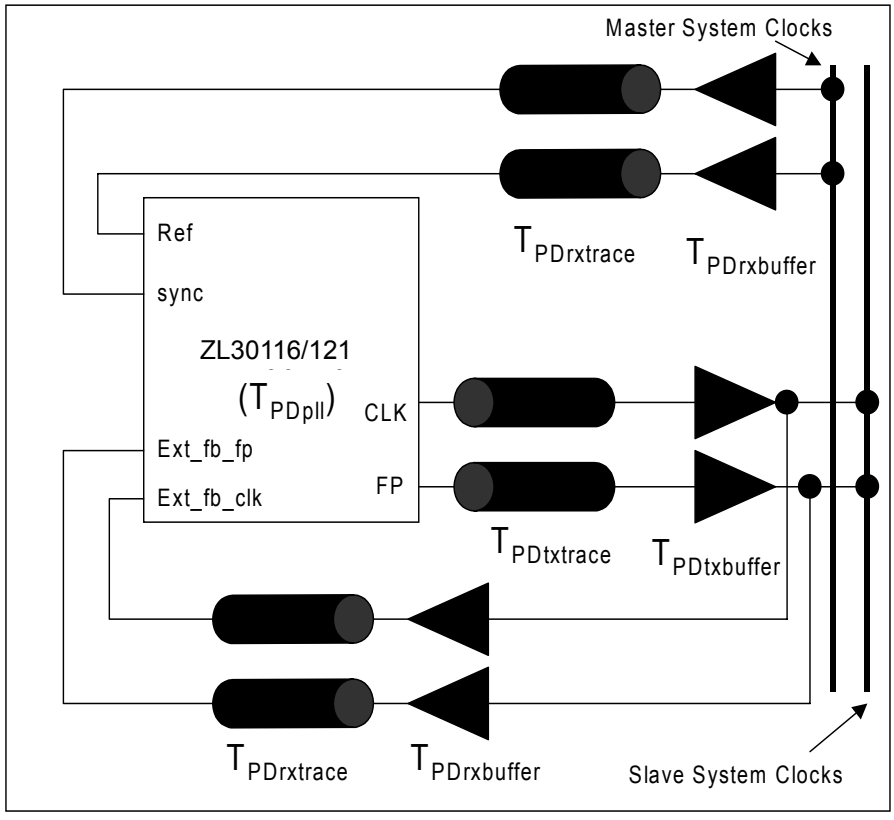

Figure 3 - ZL30116/121 Setup for External Feedback in a Master/Slave Application

4.0 Operating the ZL30116/121 in Master/Slave Mode

4.1 Master Configuration and Operation

The Basic ZL30116/121 Configuration for an ATCA Master Card is as follows;

- Automatic Reference Switching Mode
- Bandwidth of 1.7 Hz (0.1Hz if you want to support SONET)
- Phase Slope Limiting of 61 us/sec
- Pull-in range of +/-12 ppm
- Out of range detectors set to 9.2-12 ppm
- Input references carrying the CLK1 and CLK2 system clocks are disabled
- Input references carrying network references are prioritized.

Once the device has been initially configured there is very little interaction that is needed between the Master timing card and the system controller. In automatic mode, the Master will lock to the appropriate references and make all of the reference switching decisions that are necessary, and in the event that there are no valid network references available for synchronization, the device will enter holdover to ensure that valid uninterrupted system clocks are still available on the backplane.

4.2 Slave Configuration and Operation

The Basic ZL30116/121 Configuration for an ATCA Slave Card is as follows;

- Automatic Reference Switching Mode
- Bandwidth of 890 Hz
- Phase Slope Limiting is unlimited
- Pull-in range of +/-12 ppm
- Out of range detectors set to 9.2-12 ppm
- Input references carrying the CLK1 and 2 system clocks from the master card are enabled
- All other Input references are disabled.

The automated features of the ZL30116/121 again makes the basic operation of the slave card quite simple. It is configured to lock to the incoming master clocks. In the event of a failure on the master clocks, as detected by the slave, the slave will enter holdover and signal the processor to begin the master/slave switchover. Once in holdover the slave must go through the following steps to switch and become the Master Timing Card.

- Change Loop Bandwidth and Phase Slope Limits to appropriate application specific values for network synchronization via the DPLL1 control register 0 at address 0x1D
- Depending on the method used to phase align the clocks, you must either disable the external feedback path via the FB_control register at address 0x62 or reset the fine delay offset for the appropriate output paths via the P0_offset_fine(0.x3D), the P1_offset_fine(0x4F), and the SDH_offset_fine (0x55) registers.
- Reassign the input reference priorities to enable and prioritize the network references and disable the input carrying the crossover clock from the other timing card via the dpll1_ref_pri_ctrl_x registers at addresses 0x24, 0x25, 0x26, and 0x27.
- Once the device has qualified at least one of the valid references it will lock to it and this card is now the Master Timing card

5.0 ATCA Central Timing Card Block Diagram

Figure 4 shows the basic setup for using the ZL30116/121 in a central timing card application in ATCA. The card has the ability to sync to external BITS clocks, CLK3 network references as well as either of the CLK1/2 pairs of system clocks. It is also capable of driving either of the system clock pairs. Also shown here, is the use of external feedback path in slave mode to ensure tight alignment of the system clocks.

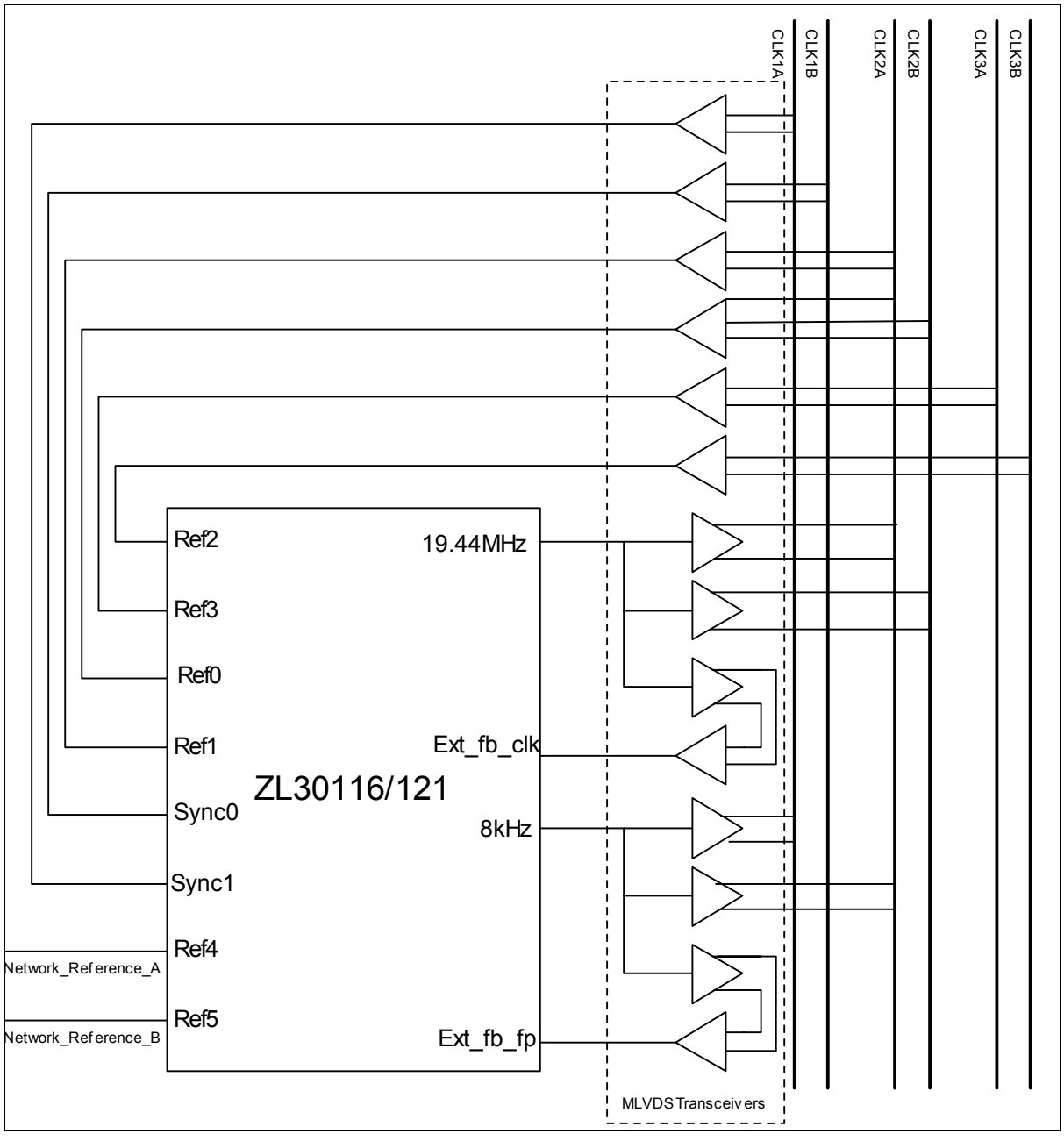

Figure 4 - ATCA Timing Card using the ZL30116/121

6.0 Summary

The ZL30116/121 contains all the features necessary to implement a robust redundant timing solution that conforms to the ATCA standard, with a minimum of effort.

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