ZLAN-179

Low Jitter Synchronizer Power Supply Decoupling and Layout Practices

Application Note

March 2007

Contents

1.0 Introduction

This document details the recommended power supply decoupling and device layout practices for the ZL30107, ZL30116, ZL30119, ZL30120, ZL30121, ZL30123, ZL30117 and ZL30122.

2.0 Power Supply Decoupling and Layout Practices

Jitter levels on the ZL30107, ZL30116, ZL30119, ZL30120, ZL30121, ZL30123, ZL30117 and ZL30122 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins as shown in Figure 1 for ZL30116, ZL30119, ZL30120, ZL30121, ZL30123 and in Figure 2 for ZL30107, ZL30117 and ZL30122.

The following common layout practices are recommended for improved power rail noise rejection.

- Two "power islands" should be created for the device, one for 3.3 V and the other for 1.8 V. A power island is a local copper area, separated from the main power plane by a series passive component. Its purpose is to provide improved isolation from noise on the board power planes. Ferrite beads provide additional suppression of digital switching noise generated by other integrated circuits connected to the main power planes. A recommended bead is Murata BLM21AG102SN1 or similar. Note that beads have some DC resistance which increases the minimum required supply voltage for the device (by about 1% for the above bead).
- Each power island should have a bulk cap of at least 10 µF with very low ESR. Ceramic provides the lowest ESR but tantalum may also be acceptable. These capacitors are used to filter low frequency (up to several hundreds KHz) noise that originate from switching power supplies. If the switching power supply is not filtered with large bulk capacitances (100 µF or more), then the 10 µf capacitors used for 1.8 V core voltage supplies (AV_{CORE} and V_{CORE}) should be replaced with low ESR 100 µF ceramic or tantalum capacitors.
- A 0.1 µF decoupling cap (ceramic X5R or X7R) must be allocated for each power pin and placed as close as possible to the via connected to the power pin. The smallest available package size should be used. Each decoupling cap should be connected directly to only one power pin, and should not share vias to power or ground with other caps.
- Priority should be given to placement of decoupling caps in nearest proximity to AV_{DD} and AV_{CORE} pins.
- AV_{CORE} pins B7 and H2 in Figure 1 and pins B6 and F1 in Figure 2 draw 25 mA each. This requires the series resistor to dissipate at least 1.25 mW of power.

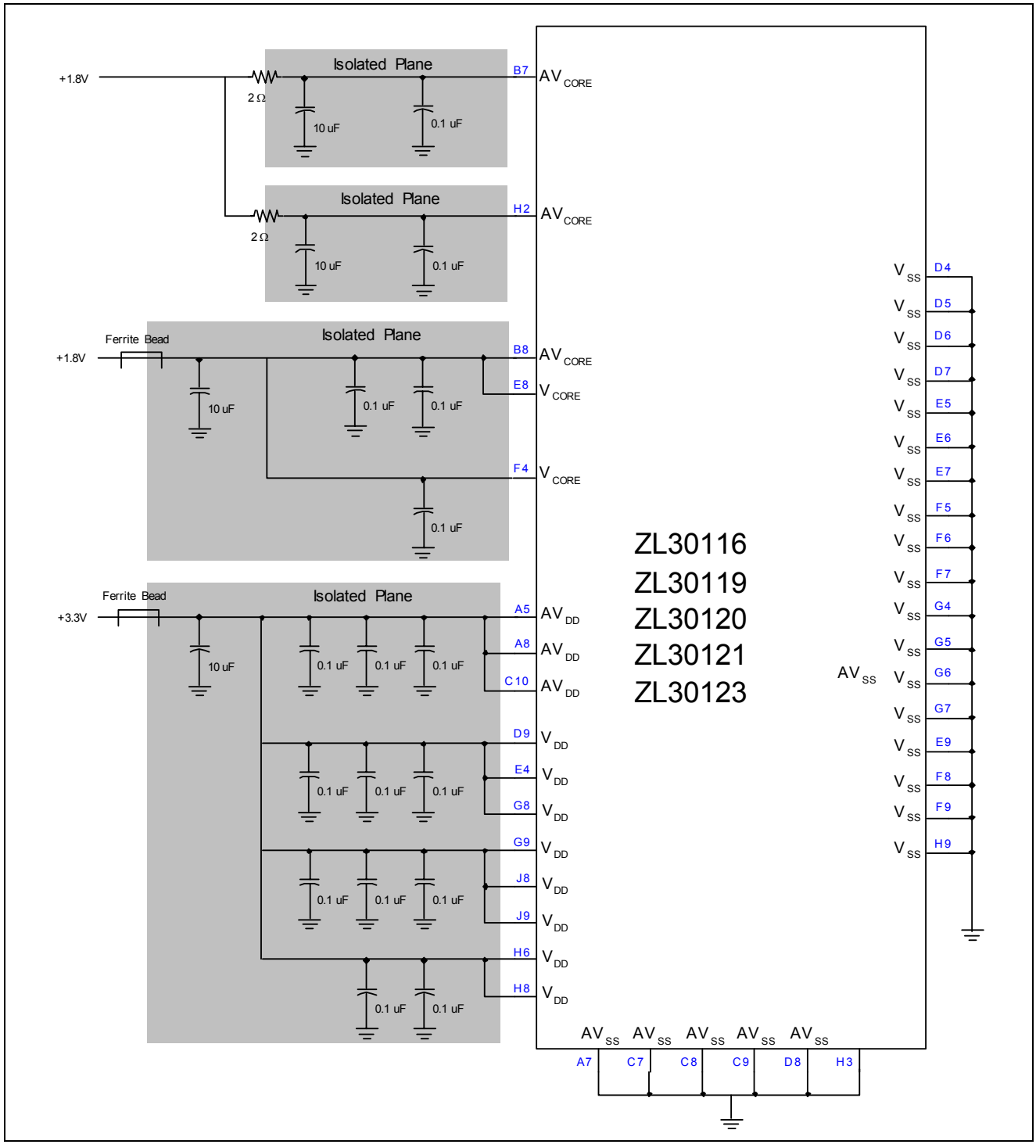

Figure 1 - Power Supply Decoupling for ZL30116, ZL30119, ZL30120, ZL30121 and ZL30123

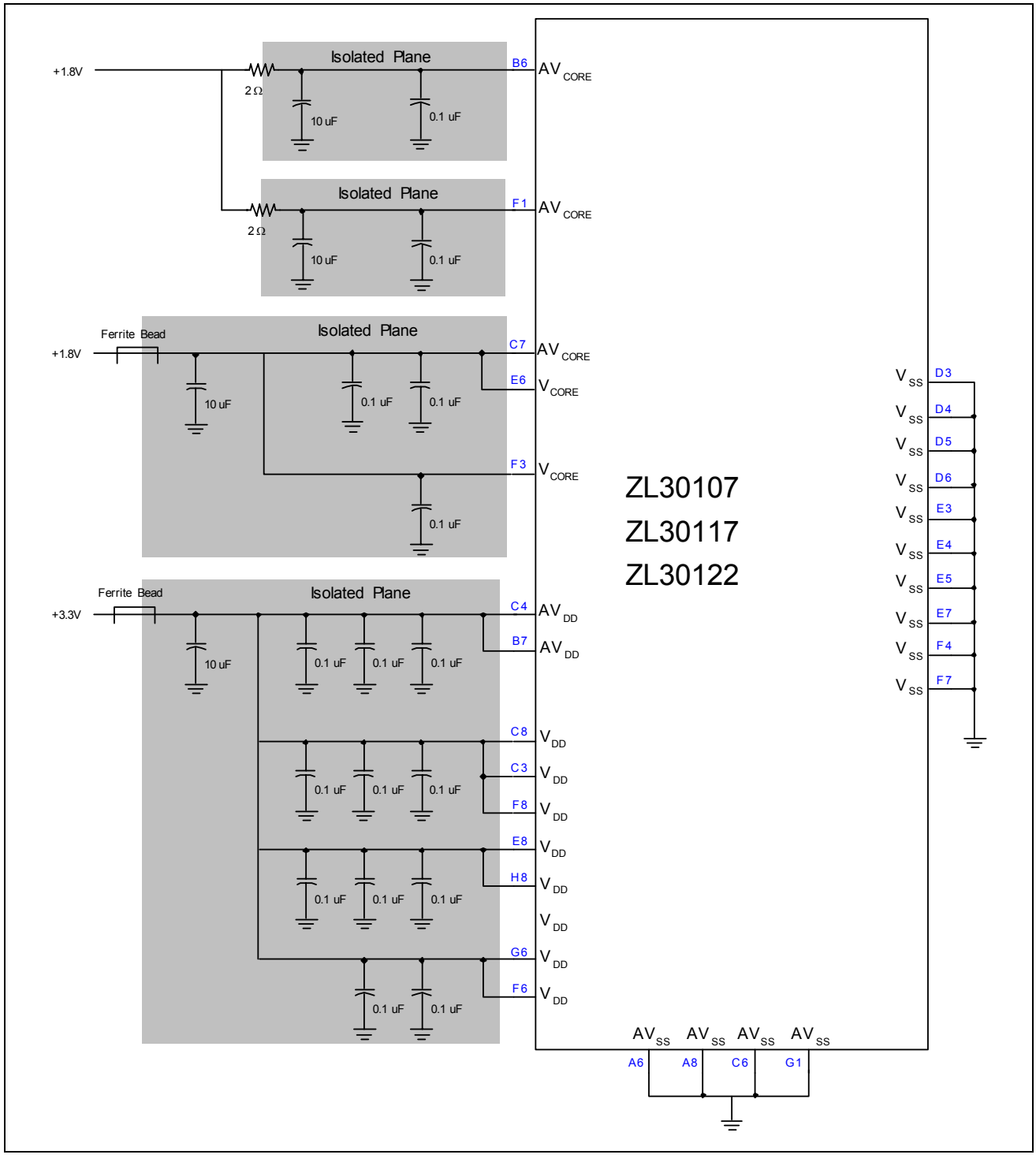

Figure 2 - Power Supply Decoupling for ZL30107, ZL30117 and ZL30122