## Contents



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## 1.0 Introduction

This application note introduces the BER (Bit Error Rate) testing capability of Zarlink's TDM switch products. It covers several product families. The basic idea of the BER test is the same for all of the TSI products, but there will be some variation in their implementation. Each implementation will be discussed in detail.

## 2.0 What is BERT?

BERT is a test that serves the purpose of testing the voice or data channels. It is an efficient way to identify problems in a design. The BERT will show errors in the case of excessive jitter, small sampling margins, incorrect configurations etc.

On the transmit side of the system under test, BERT involves selecting a test channel(s), and sending a pseudo random test pattern across that channel(s). The pseudorandom pattern is defined in the ITU standard O.151. The standard defines several possible

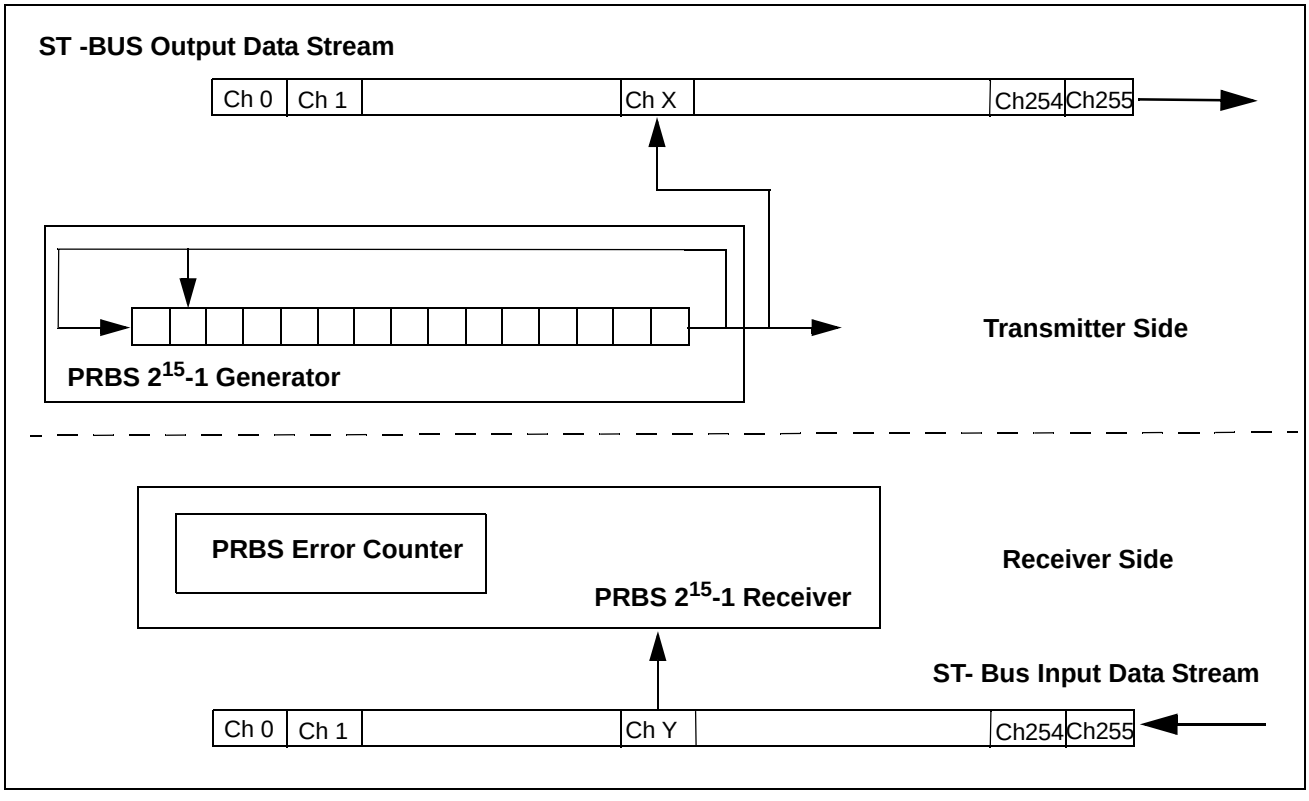


**Figure 1 - General BERT Configuration**

pseudorandom patterns but the most commonly used is the sequence of $2^{15}$-1. This sequence has a bit length of 32767. It is constantly repeated during the transmission of the BER test. This pattern is used in all of the devices discussed in this application note. Another pattern defined in O.151, implemented in one of the devices in this application note, is $2^{23}$-1.

On the receiver side, after the pseudorandom pattern is received, it is recognized and the bit errors are detected and reported in the bit error rate counter. The variations between different BER implementations may include, BERT that spans across several channels, or several BERT transmitters and receivers per device.

## 3.0 BERT in the MT90826

The MT90826 allows users to perform bit error rate monitoring by sending a pseudo random pattern to a selected ST-BUS output channel and receiving that pattern from a selected ST-BUS input channel. The pseudo random pattern is internally generated by the device with the $2^{15}$ -1 polynomial.

Users can select a pseudorandom pattern to be presented on a ST-BUS channel by programming the TM0 and TM1 bits in the connection memory. When TM0 and TM1 bits are high, the pseudorandom pattern is output on the selected ST-BUS output channel. The pseudo random pattern is then received by a ST-BUS input channel which is selected using the BSA and BCA bits in the Bit Error Rate Input Selection Register - BISR(0x0011). An internal bit error counter keeps track of the error counts which is then stored in the Bit Error Count Register - BECR(0x0012). The bit error test is enabled and disabled by the SBER (bit 9) in the Control Register(0x0000). Setting the bit from zero to one initiates the bit error test and enables the internal bit error counter. When the bit is programmed from one to zero, the device stops the bit error rate test and the internal bit error counter and transfers the error counts to the count register. A zero to one transition of the CBER (bit 10) of the Control Register (0x0000) resets the bit error count register and error counter.

### 3.1 Important Notes for BERT in MT90826

There are a few important notes about the MT90826 BERT test listed below:

1. The BERT must be enabled on a single only transmit channel and on one receive channel at any point in time. If the user mistakenly enables BER on several transmit ST- BUS channels, the BERT test will fail, because the BER polynomial will be split across all of the enabled channels, and one single receive channel will thus receive incorrect sequence.
2. The MT90826 BERT implementation doesn't have a lock indication on the receive side. Therefore, the programmer may not know whether the BERT errors are occurring because the sequence is not locked or because there is something wrong with the transmission channel. Therefore, the user must follow a specific programming sequence. The transmitter automatically starts transmitting when the output is enabled, the receiver will start receiving once the SBER(bit 9) of the Control Register (0x0000) is set. In all cases, the transmitter must be started before the receiver is enabled. If there is a significant delay in the system, it should be added between enabling of the transmitter and the receiver. If there is no significant delay in the system, the receiver can be enabled a couple of milliseconds after the transmitter. Before the lock has been achieved, there will be a constant number of bit errors counted in the bit error rate counter. The BER counter must be cleared before the actual test is started.
3. The MT90826 does not recognize an input of all ones as an error. If all ones are being sent to the input channel, the BER counter does not increment. Therefore, defined data should be sent to an input channel by using a message mode to ensure proper connectivity, and then running the BER test normally.
4. After the power up, the content of the connection and the data memories is unknown. In order to ensure that the BERT is enabled on only one channel when the BERT test is started, the user must program the connection memory to a known value. The easiest way to program the connection memory is through block programming. All of the channels in the memory should be put to a non BER mode, for example, the message mode or tristate.

### 3.2 MT90826 BERT Programming Sequence

The programming sequence for starting a BERT on channel 1, stream 0 and receiving it on channel 5, stream 2 is shown below. It is assumed that there is an external connection between the stream 0 and stream 2 and that external to the device channel 1, stream 0 is switched to channel 5 stream 2. One such connection can be established through another TSI device, BERT may be tested if there is a physical loopback from one stream to another.

The sequence is:

1. Enable ODE
2. Initialize the connection memory to message mode or tristate. The easiest way is to use connection memory block programming.
3. Program the connection memory at 0x2001 with 0xE000. This step selects and enables the BER pattern for selected transmit channel.
4. Wait a couple of milliseconds (or more depending on the external delay between the transmitter and the receiver). This wait is for the data to be looped from the transmitter to the receiver.
5. Write 0x0205 to the BISR register (0x0011). This step selects the receive channel for a BER pattern.
6. Clear the error counter by setting CBER bit (bit 10) of the Control Register (at address 0x0000) and clearing it. This step is needed to clear any initial errors that might have appeared before the lock has been established.
7. The BERT is enabled by setting bit 9(SBER bit) of the Control Register (at address 0x0000) to 1.
8. Wait for X msec. This is the user programmed desired BERT running time.
9. Disable BERT by clearing SBER (bit 9) of the Control Register(0x0000).
10. Check the Bit Error Counter Register(at 0x0012) for bit errors.

## 4.0 BERT in the MT90866 and ZL50030/31

The BER $2^{15}$ - 1 test pattern capability is available on the MT90866 and ZL50030/31 as well. The example below will focus on the MT90866, but the same programming sequence can be applied to the ZL50030 and ZL50031.There is one BERT test feature for the backplane streams and one for the local streams. Those two tests are fully independent and can be running at the same time.

For the test, the transmitter and receiver portion of the BERT need to be configured. The transmitter is configured when the output channel and stream are programmed through the backplane or local connection memory. The receiver is programmed when the input channel and stream are configured through the Local or Backplane BER Input Selection (BIS) registers.

### 4.1 Important Notes for BERT in the MT90866

There are few important notes about the MT90866 BERT test listed below:

1. For backplane or local streams the BERT must be enabled on only one transmit channel and on one receiver channel. For the backplane side, there can be only one backplane transmit channel and one receive channel running BERT. The same applies for the local side. There can be only one BER test running on the backplane and one BER test running on the local side simultaneously.

If for any reason, the user enables BER on several transmit ST- BUS channels on the same side(either local or backplane), the BERT test will fail, because the BER polynomial will be split accross all of the enabled channels on one side, and the receiver will not be able to synchronize to the correct pattern.

2. The MT90866 BERT implementation doesn't have a lock indication. Initially the user will not be able to determine if BER errors appear because of the sequence is not locked or because there is something wrong with the transmission channel. Therefore, a specific programming sequence must be followed. The transmitter automatically starts transmitting when the output is enabled and the receiver will start receiving once the SBERB(or SBERL for the local side) bit in the Control Register(0x0000) is set. So, in all cases, the transmitter must be started before the receiver is enabled. If there is a significant delay in the system, this delay must be taken into consideration and added to the programming sequence before the receiver is enabled. If there is no significant delay in the system, the receiver can be enabled a couple of milliseconds after the transmitter.

Before the lock has been achieved, a few bit errors may appear in the bit error rate counter. The BER counter must be cleared before the actual test can be started.

3. After a power up, the content of the connection and data memories is unknown. To ensure that the BERT is enabled on only one channel of the local or connection memory, before the BERT test is started, the user must program all the target connection memory to a known value. The easiest way to do this is through block programming, when all channels in the memory should be put to non BER mode, for example, the message mode, or tristate.

### 4.2 MT90866 BERT Programming Sequence

The programming sequence for starting a BERT on transmit backplane channel 1, stream 0 and the receiver on backplane channel 5, stream 2 is shown below. It is assumed that there is an external connection between stream 0 and stream 2 and that external to the device, channel 1, stream 0 is switched to channel 5 stream 2. One such connection can be established through another TSI. BERT can also be tested if there is a physical loopback from STo stream to STi streams. The same sequence can be used for programming BERT on local side when the corresponding registers/bits are used.

The sequence is:

1. Enable ODE
2. Initialize the backplane connection memory to message mode or tristate. The easiest way is to use the backplane connection memory block programming. This step is important to ensure that there are no channels of the backplane side that are in the BER mode before starting the test.
3. Program the backplane connection memory at 0x2001 with 0xE000. This step programs the backplane transmit stream 0, channel 1 for BER pattern. It also enables the backplane BER pattern on that channel.
4. Wait a couple of milliseconds (or more depending on the external delay between the transmitter and the receiver). This wait for the transmit data to be looped back to receive side.
5. Write 0x0205 to Backplane BER Input Selection Register - BBIS(0x0021). This step selects the backplane receive channel for BER pattern.
6. The BERT is enabled on the receive side by setting SBERB(bit 7) of the Control Register (0x0000) to 1.
7. Clear the error counter by setting CBERB bit (bit 8) of the Control Register (at address 0x0000) and clearing it. This step is needed to clear any initial errors that might have appeared before lock has been established.
8. Wait for X msec. This is user programmed desired BERT running time.
9. Disable the backplane BERT by clearing SBERB (bit 7) of the Control Register(at address 0x0000).

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10. Check the Backplane Bit Error Counter Register(at 0x0029) for bit errors.
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Step 10 can also be performed before step 9 while the BERT is running in order to dynamically check for errors.

## 5.0 BERT in the MT90869/70/71, ZL50060/61, ZL50057/58 and ZL50050

The BERT implementation is very similar in the MT90869/70/71 and the ZL50060/61(ZL50057/58 and ZL50050). Therefore, the details of the programming and description of the functionalities will be presented on the example of the MT90869. The only difference for ZL50060/61 (ZL50057/58 and ZL50050) devices, is the BERT test must be conducted offline, i.e the switch cannot pass traffic when the BERT is running.

Two separate BER test mechanisms are provided for the Local and Backplane ports. In both ports there is a BER transmitter and a BER receiver. The transmitter generates a $2^{15}$-1 or $2^{23}$ -1 Pseudo Random Binary Sequence (PRBS), which may be allocated to a specific stream and a number of channels. This is defined by a stream number, a start channel number, and the number of consecutive channels following the start channel.The stream, channel number and the number of consecutive channels following the start channel are similarly allocated for the receiver. An example of the PRBS test is presented in the Figure 2. In this figure, the BERT is enabled on channels one, two and three of the selected stream - for example stream 0. Also, an assumption is made that the backplane stream 0 is physically looped back to backplane stream 2.

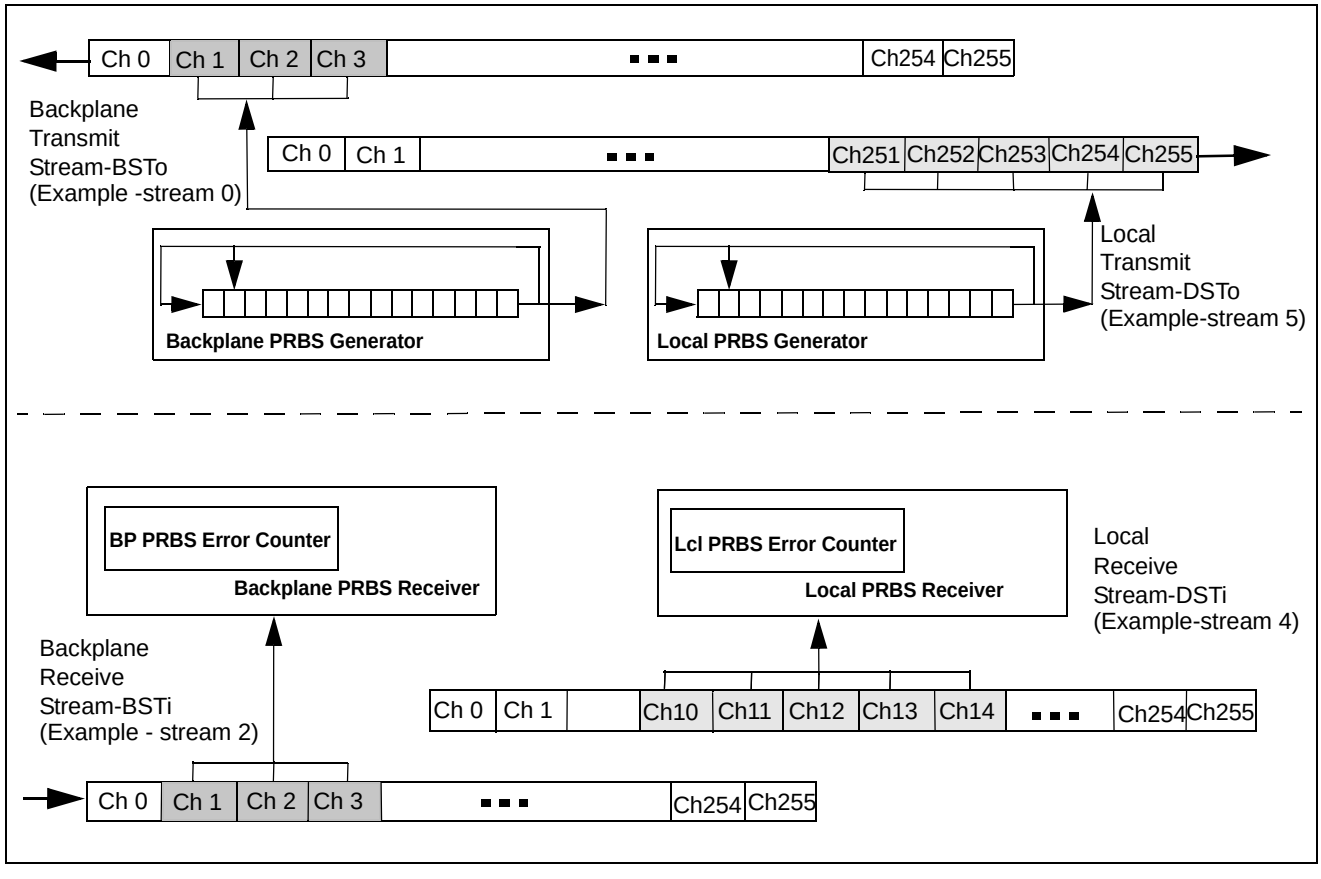


**Figure 2 - MT90869 BERT Implementation**

For the local side, the BERT is enabled on 5 consecutive transmit channels, channel 251 through channel 255 on transmit stream 5. On the receive local side, the matching number of channels need to be programmed. But this time, we've chosen receive channels 10 through 14 of stream 4. This kind of connection is possible only if the channels are externally switched using another TSI device which will switch transmit channels 251-255 of stream 5 to receive channels 10 to 14 of stream 4.

When enabled, the receiver attempts to lock to the PRBS on the incoming bit stream. Once the lock is achieved, by detection of a seed value, a bit by bit comparison takes place and each error increments a 16-bit counter.The lock is indicated by lock bits LOCKL for the local side and LOCKB for the backplane side. For MT90869/70/71 the counter will roll-over in the event of an error count in excess of 65535 decimal (0xFFFF). For ZL50060/61, ZL50057/58 and ZL50050, the BER counter will saturate.

### 5.1 The MT90869 BERT Programming Sequence

A programming example for setting up the backplane BERT test as shown in Figure 2 is described in this section. The same steps should be followed for running the BERT on the local side.

1. Enable ODE
2. Program the Backplane BER Start Send Register - BBSSR (0x00C8)with desired backplane stream and start channel for BERT sequence. For the backplane stream 0 from Figure 2, the content should be 0x0001.
3. The register Backplane Transmit BER Length Register - BTxBLR (0x00C9)contains the number of consecutive transmit channels that follow the start channel and that contain the transmit PRBS sequence. For the backplane example from figure 2, the content of the BTxBLR should be 0x0002.
4. Program the Backplane BER Start Receive Register - BBSRR(0x00CB)with desired receive backplane stream and start channel for BERT sequence. For backplane receive channels from Figure 2, the content should be 0x0401.
5. The Backplane Receive BER Length Register - BRXBLR (0x00CA)contains the number of consecutive receive channels that follow the start channel and receive the PRBS sequence. For this example, the content of the BRXBLR should be 0x0002.
6. The backplane BER counter should be cleared before starting the test. This is achieved by setting CBERB (bit 9) of the Bit Error Rate Test Control Register - BERCR (0x0002).
7. The desired backplane BER pattern should be chosen through PRBSB(bit 6) of the BERCR(0x0002). For $2^{15}$-1 sequence, this bit should be programmed to 0.
8. The BERT test is started by setting SBERRXB(bit 8) and SBERTXB(bit 7) of the BERCR register (0x0002). The order of setting these two bits is not important.
9. Wait for the backplane BERT lock indication. This is done by monitoring bit LOCKB(bit 11). If this bit is one the backplane BERT receiver has locked.
10. Wait for X msec. This is user programmed desired BERT running time.
11. The BERT test is stopped by programming bits SBERRXB(bit 8)and SBERTXB(bit 7) to 0.
12. Read the number of errors from BER counter - BBCR register(0x00CC).

## 6.0 BERT in the 4 K TDM Switches

The 4 K TDM switch portfolio consists of several devices ranging from the ZL50015 to ZL50023. The BERT will be explained on the example of the ZL50021 device, the most feature rich 4 K device. A similar test can be easily applied to the other 4 K devices.

The ZL50021 has one BER transmitter and one BER receiver for each pair of the input and the output streams, resulting in the 32 transmitters connected to the output streams and 32 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of $2^{15}$-1 pseudorandom code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame (125 μs). The global BER enable bits RBEREN (bit 5) and TBEREN (bit 4) in the IMS register should be programmed before the BER is started. In order to save power, the 32 transmitters and/or receivers can be

disabled. Multiple connection memory locations can be programmed for BER tests, such that the BER patterns can be transmitted for multiple consecutive output channels. If consecutive input channels are not selected, the BER receiver will not correctly compare the bit patterns. The number of output channels which the BER pattern occupies has to be the same as the number of channels defined in the BER Length Register (BRLR) which defines how many BER channels are to be monitor by the BER receiver. When the lock has been detected the lock indication bits in the BER receiver LOCK register will be set.

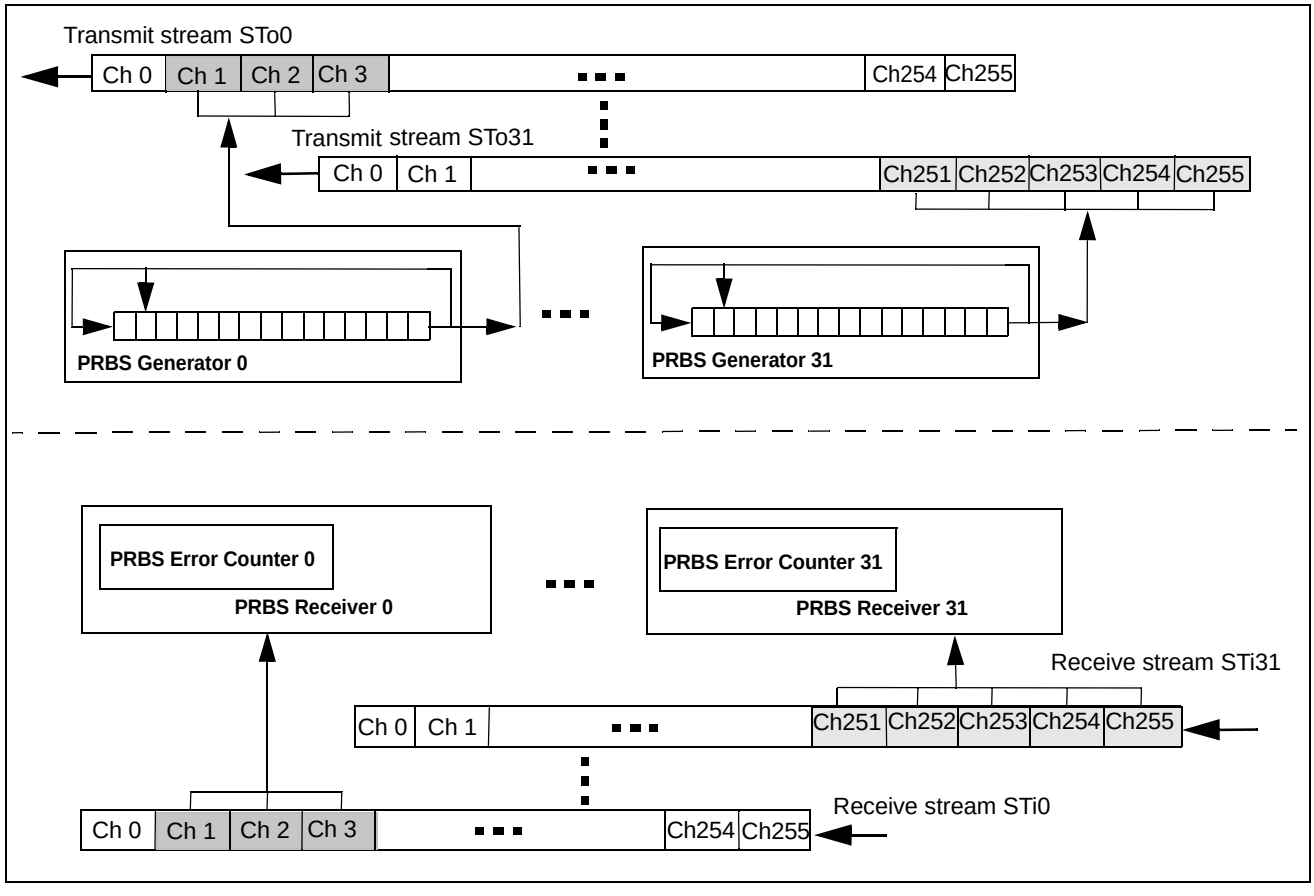


**Figure 3 - ZL50021 BERT Implementation**

## 6.1 The ZL50021 BERT Programming Sequence

The ZL50021 programming sequence is as follows:

1. Enable ODE
2. Initialize the connection memory to message mode or tristate. The easiest way is to use the connection memory block programming. This step is important to ensure that there are no channels that are in the BER mode before starting the test.
3. Program the TBEREN (bit 4) and RBEREN (bit 5) in the IMS(0x0001) register to enable all transmitters and receivers.
4. Program the desired channels in the connection memory to send the BERT. For the BERT to run, the CMM(bit 0) of the connection memory low must be 1. Also, bits PCC1-0(bits 2-1) must be 10 to enable the per stream BER transmitters. For the backplane example of figure 3, the connection memory addresses 0x2001,0x2003 and 0x2003 should be programmed with 0x0005.

5. Before enabling the transmitter and the receiver there must be a minimum two frame wait.If there is significant delay between transmitter and the receiver, that delay should be added to this wait.
6. Program a start channel in the receiver from which the BER receive test is starting to be monitored. This is done by writing to BER Receiver Start Register N - BRSR(n)(0x0300-0x031F).For the stream 0 example from figure 3, 0x0001 should be written to BRSR0(0x0300) There is one register for each receive stream.
7. The BER Receiver Length Registers BRLRn(0x0320 - 0x033F)contain the number of consecutive receive channels that are receiving the BER pattern per stream. The minimum number of channels that contain BERT is one and the maximum number is the number of channels in a frame. On the example of the receive stream 0, there are three channels, receiving the BER pattern and therefore the content of the BRLR0 should be 0x0003.
8. The BERT test is actually started by programming SBER(bit 0) of the BER Receiver Control Register BRCRn (0x0340 - 0x035F) for the desired stream.
9. Wait for BERT lock indication. This is done by monitoring the corresponding bit of the BER Receiver Lock Registers 0 and 1 - BERLR0(0x0013) and BERLR1(0x0014).
10. Clear the BERT counters. This is achieved by setting the CBER bit(bit 1)of the BER Control Registers - BRCRn (0x0340 - 0x035F) for the desired stream.
11. Wait for X msec. This is the user programmed desired BERT running time.
12. The BERT test is stopped by programming bit SBER(bit 0)of the BRCRn register to 0.
13. Read the number of errors from BER counter. There is one counter for each BER rate receiver for a total of 32 counters. The counters can be read from BRERn registers(0x0360 - 0x037F).

## 7.0 BERT in the 32 K TDM Switches

The 32 K TDM switch portfolio consists of several devices including the ZL50070, ZL50073, ZL50074 and ZL50075. The BERT will be explained on the example of the ZL50073 device, the most feature rich device. A similar test can be easily applied to other 32 K devices with the exception of the ZL50074 which doesn't support BERT capability.

There are 128 transmit streams and 128 receive streams in the ZL50073. Each transmit STo stream has an associated BER transmitter and each receive STi stream has an associated BER receiver. Similar to the other devices described in this note, the BERT pattern used is $2^{15}$-1. For 8.192 Mbps and 16.384 Mbps modes, the maximum number of transmit and receive streams is 128(each). Therefore, the maximum number of BER tests that can be running simultaneously is 128. For 32.768 Mbps the maximum number of BER tests simultaneously running is 64 and for 65.536 Mbps, it is 32. There is one BER counter associated with each BER receiver which amounts to the maximum of 128, 64 or 32 BERT counters depending on the stream rate. When the counter is saturated to 65535 it doesn't rollover. It can be reset by reseting the device or writing to the counter.

The BER pattern can be enabled on a minimum of one channel and a maximum of 1024 channels. The maximum number of channels depends on the stream rate, for the 65.536 Mbps, it is 1024, for the 32.768 Mbps it is 512, for 16.384 Mbps it is 256 and for 8.192 Mbps, it is 128 channels. Unlike other BERT implementations described in this document, here we can enable BERT mode for channels that are not consecutive. It is important that transmit and receive channels are corresponding and that the order in which the channels are sent is the same as the order in which they are received.

Figure 4 illustrates the BER test as implemented in the ZL50073 TDM switch.

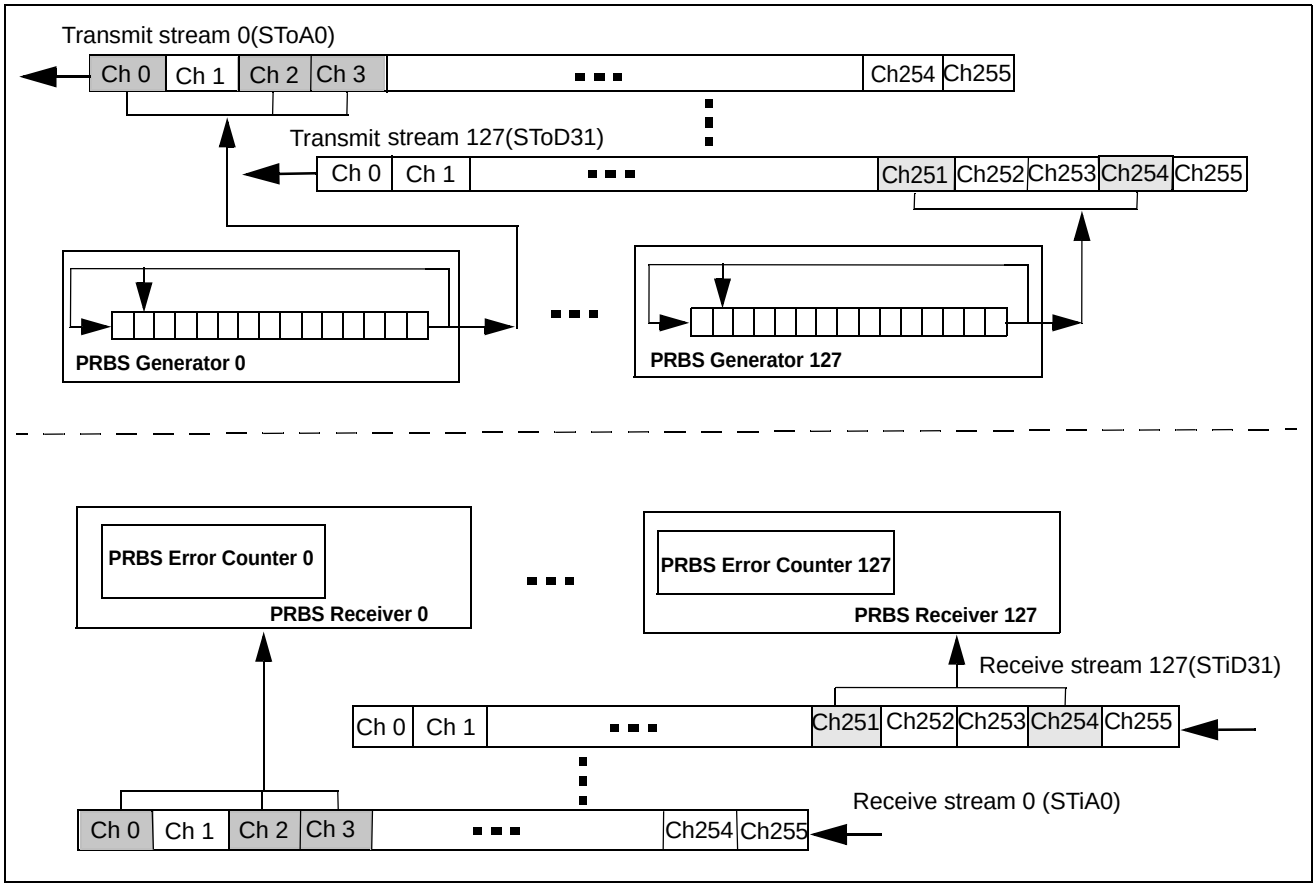


**Figure 4 - ZL50073 BERT Implementation**

### 7.1 The ZL50073 BERT Programming Sequence

Based on the Figure 4 example for the stream SToA0 and STiA0, the ZL50073 programming sequence is as follows:

1. Enable ODE
2. Initialize the connection memory to message mode or tristate mode. The easiest way is to use the connection memory block programming. This step is important to ensure that there are no channels that are in the BER mode before starting the test.
3. For the example of STiA0 stream, channels 0,2 and 3, programPCF2-0(Bits 31-29) of the connection memory at addresses 0x00000,0x00008 and 0x0000C to 0xA0000000. This step programs the transmit stream STiA0, channels 0,2 and 3 for the BER pattern.It also enables the BER pattern on those channels.
4. Wait a couple of ms (or more depending on the external delay between the transmitter and the receiver). This wait is needed for the transmit data to be looped back to receive side.

5. The receive stream and channel for the BER pattern is enabled by writing to the BER Enable Control Memory. For the full BER Enable Control Memory Address Map, please refer to ZL50073 datasheet, section 14.3.1. The start of BER Enable Control Memory is at address offset 0x030000. So, in order to enable the receiver on stream 0 to receive the BER pattern on channels 0,2 and 3,bit BCE(bit 0) in the BER Enable Control Memory Addresses, should be programmed to 0x01000101 (for 32 bit access). Each byte of this 32 bit memory location corresponds to one of the first four channels of the stream 0.
6. Before starting the BER test, the corresponding counter for the input stream should be cleared.The counter is cleared by writing 0 to it.For the example, in figure 4, for stream 0, 0 would be written to address 0x040000.
7. Wait for X msec. This is the user programmed desired BERT running time.
8. Check the Bit Error Counter Register(0x040000 address offset for stream 0) for bit errors.
9. Disable the BERT by programming the BCE bit of the BER Enable Control Memory Address for stream 0 to 0x0. As in step 5, the address location 0x030000 should be programmed with 0x0.

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