ZLAN-120

Mid Density Digital Switches Timing Modes

Application Note

Contents

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1.0 Introduction

This document describes operation of different timing modes offered on mid density digital switches. The mid density switches are offered in 1024 x 1024, 2048 x 2048 and 4096 x 4096 64 Kbps channel sizes. All devices in this family (ZL50015, ZL50016, ZL50017, ZL50018, ZL50019, ZL50020, ZL50021, ZL50022 and ZL50023) can operate in slave timing mode and those with integrated DPLL (ZL50015, ZL50018, ZL50019, ZL50021 and ZL50022) can operate in master timing mode as well. This DPLL meets Stratum 4E and Stratum 3 and has very low intrinsic jitter (below 1 ns) on its outputs.

All devices in this family have very good jitter tolerance which is critical in designs where the serial streams are running at high data rates.

Typically there is only one timing master in the system (or two if system has redundancy protection) and a number of timing slaves. The timing master usually gets extracted line clock from a line interfaces (T1/E1), cleans it from jitter and wander, and generate clock and frame pulses for timing slave devices. This clock is also fed to the line interface devices to read the received data as well as to clock transmit signal, as shown in Figure 1.

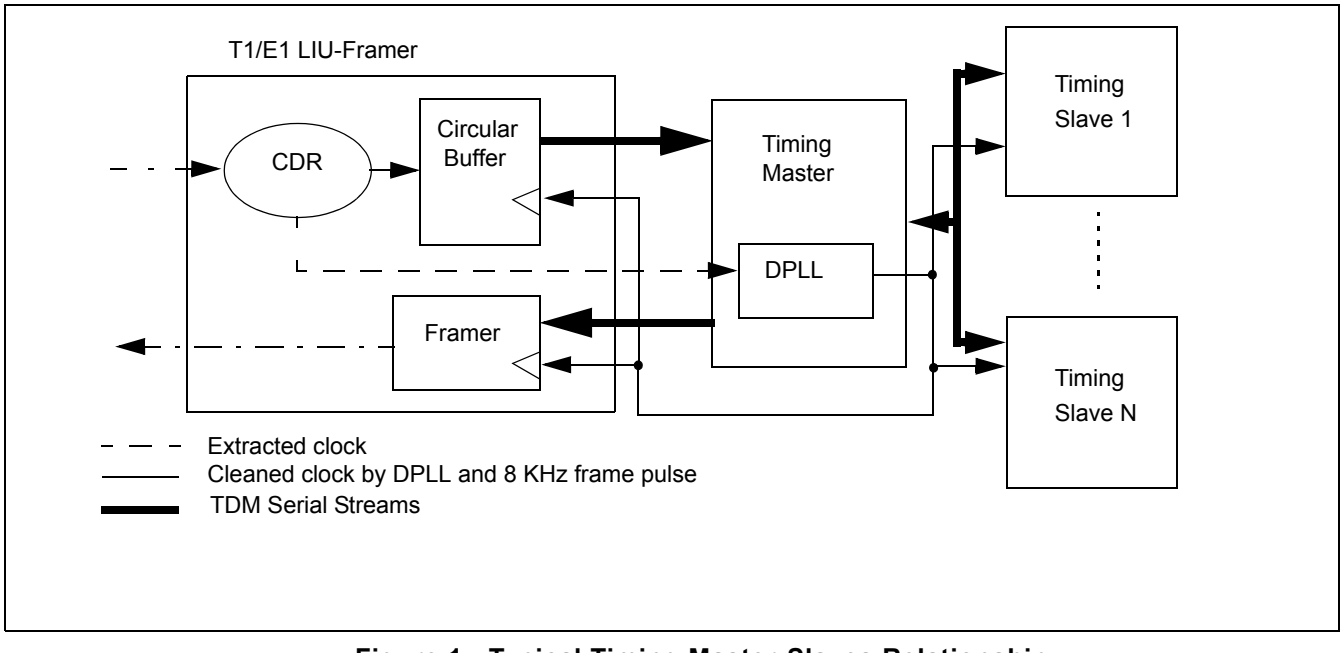

Figure 1 - Typical Timing Master-Slaves Relationship

2.0 Master Timing Mode

In this mode the internal timing of the device is driven by DPLL synchronized to one of its four input references as shown in Figure 2. The references are usually extracted clocks generated by line interface devices such as T1/E1 framers. The output of the DPLL is used to drive the core logic block as well as the input and the output buffers. Alternatively it is possible to use CKi and FPi inputs to drive the input buffer. Typically this would be used where there is a large offset between the input data and the clock as shown in Figure 3.

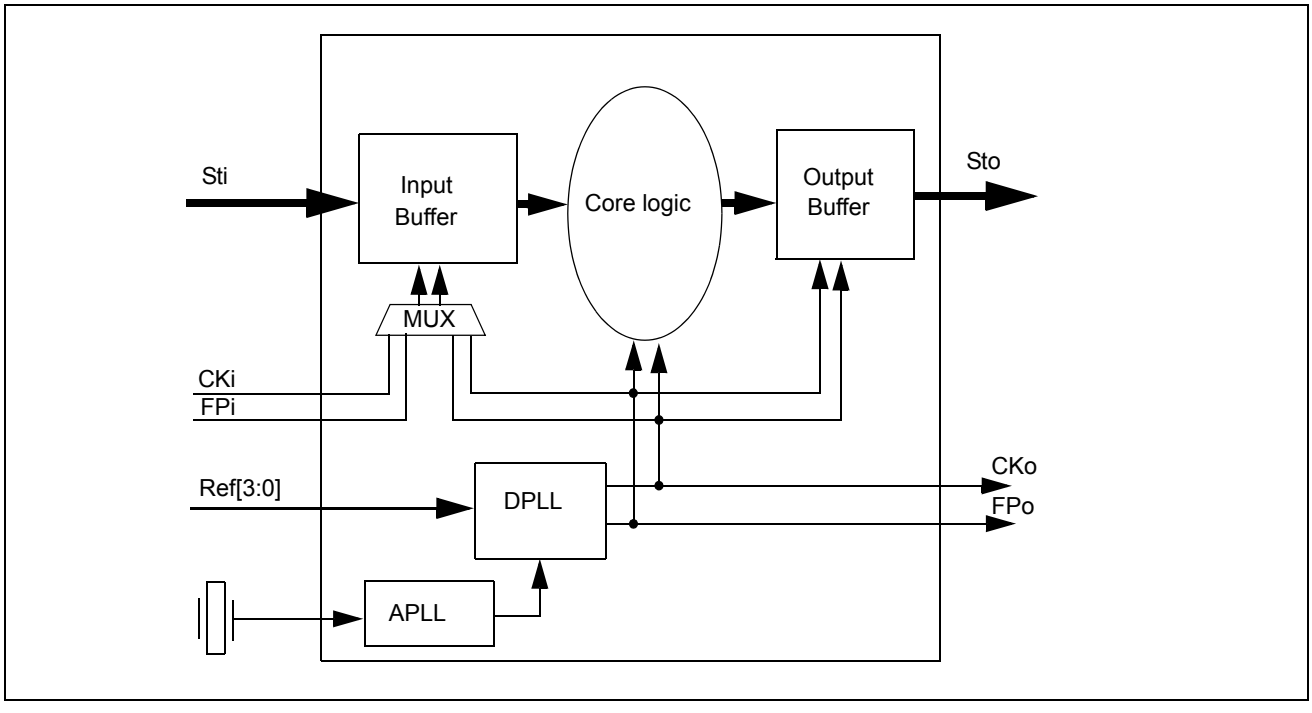

Figure 2 - Master Timing Mode

The T1/E1 framer-LIU extracts clocks from the T1/E1 links it terminates and drives them over the backplane to the Timing Master. The DPLL in the Timing Master locks to one of the extracted clocks, cleans it from the jitter and wander and outputs it at CK0 and FPo.

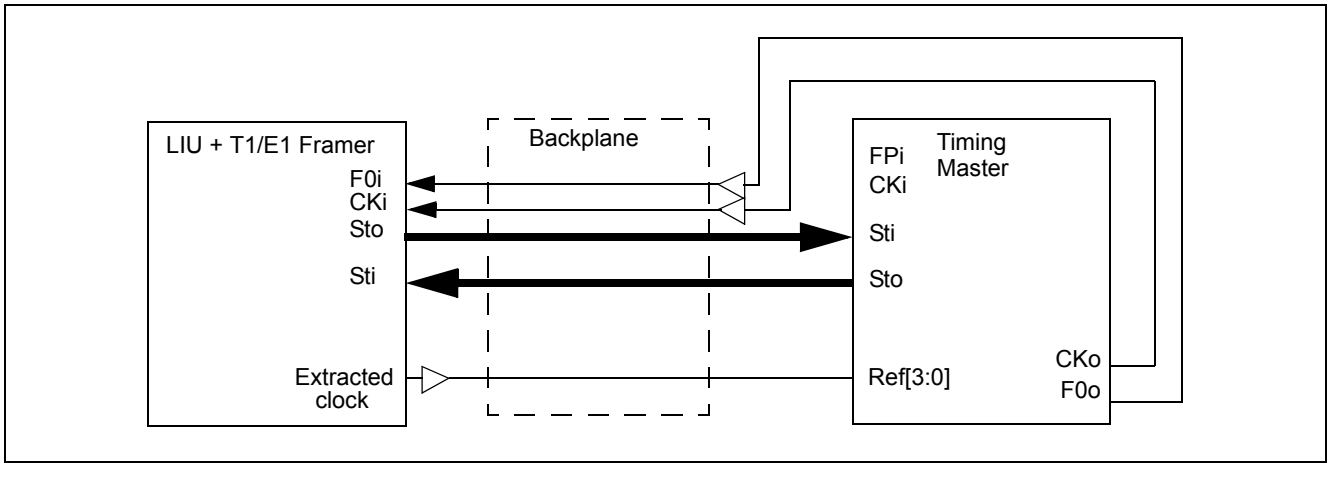

Figure 3 - Example of an Application where the External Feedback is Needed

The Cko and FPo are fed back to the Framer where it is used to sample serial TDM streams in and out of the Framer. By the time data arrive to the inputs of the Timing Master, it is delayed relative to the clock by: delay of the Timing Master output buffer plus two times propagation delay between the Timing Master and the Framer plus clock to data out delay of the Framer plus any additional clock/data buffering delay. The total delay could violate setup time at the Sti inputs of the Timing Master at the high data rates such as 16.384 Mbps. This can be solved by routing Cko and F0o to CKi and F0i respectively and inserting the adequate delay in the path rather than using internally generated clocks as can be seen in Figure 4.

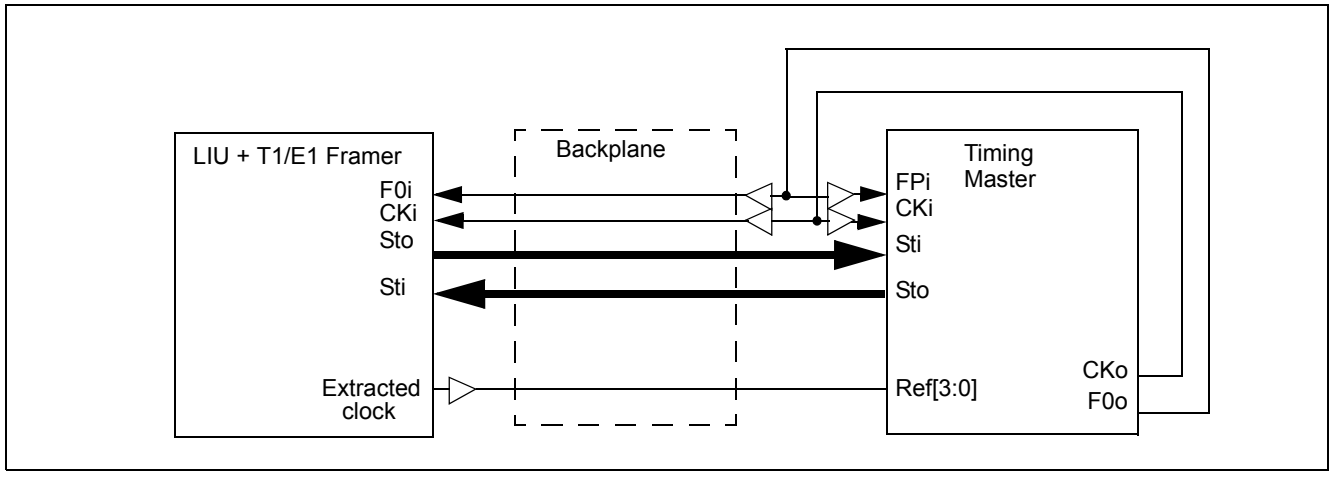

Figure 4 - Typical Application of the Timing Master Mode with external feedback

3.0 Multiplied Slave Mode

In this mode DPLL is not used and timing (clock and frame pulse) is provided by external device. The block diagram of internal timing is shown in Figure 5.

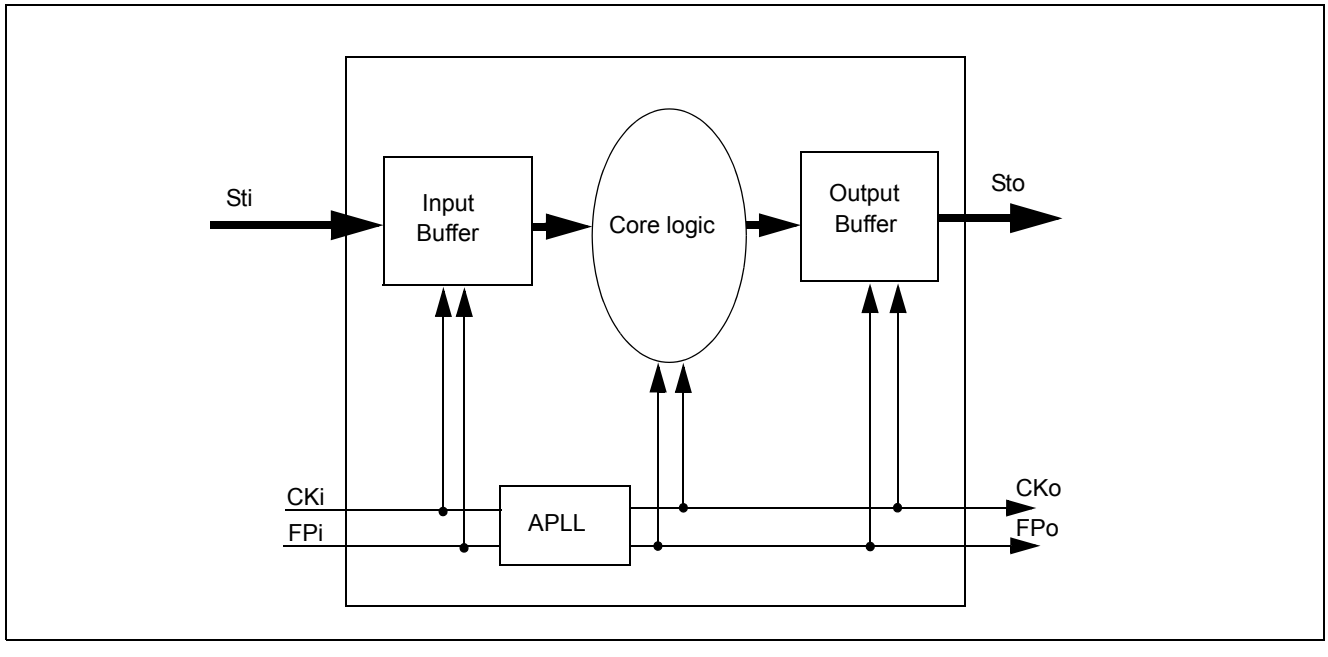

Figure 5 - Multiple Slave Mode

To make device highly tolerant to jitter, the input data is sampled with the input clock. If the input clock is jittery, than the input data will have the same jitter but relative to each other they will have fixed relationship (no jitter). Maximum data rate the switch can accept at its inputs is equal to frequency of the CKi clock. For instance device will be able to accept 8.192 Mbps data streams only if the CKi runs at 8.192 MHz or 16.384 MHz.

The input clock is further multiplied and cleaned from the jitter with an analog PLL. Although this analog PLL has high bandwidth it can still filter higher frequency jitter (above 100 KHz) like cycle to cycle jitter. The output of the analog PLL is used to time the Core logic and the output buffers. The output data streams Sto can be programmed to run at any data rate (2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps) regardless of the input data rate.

4.0 Divided Slave Mode

This mode is similar to the Multiplied Slave Mode except that now the output is also timed by the input clock CKi and the frame pulse FPi as shown in the Figure 6.

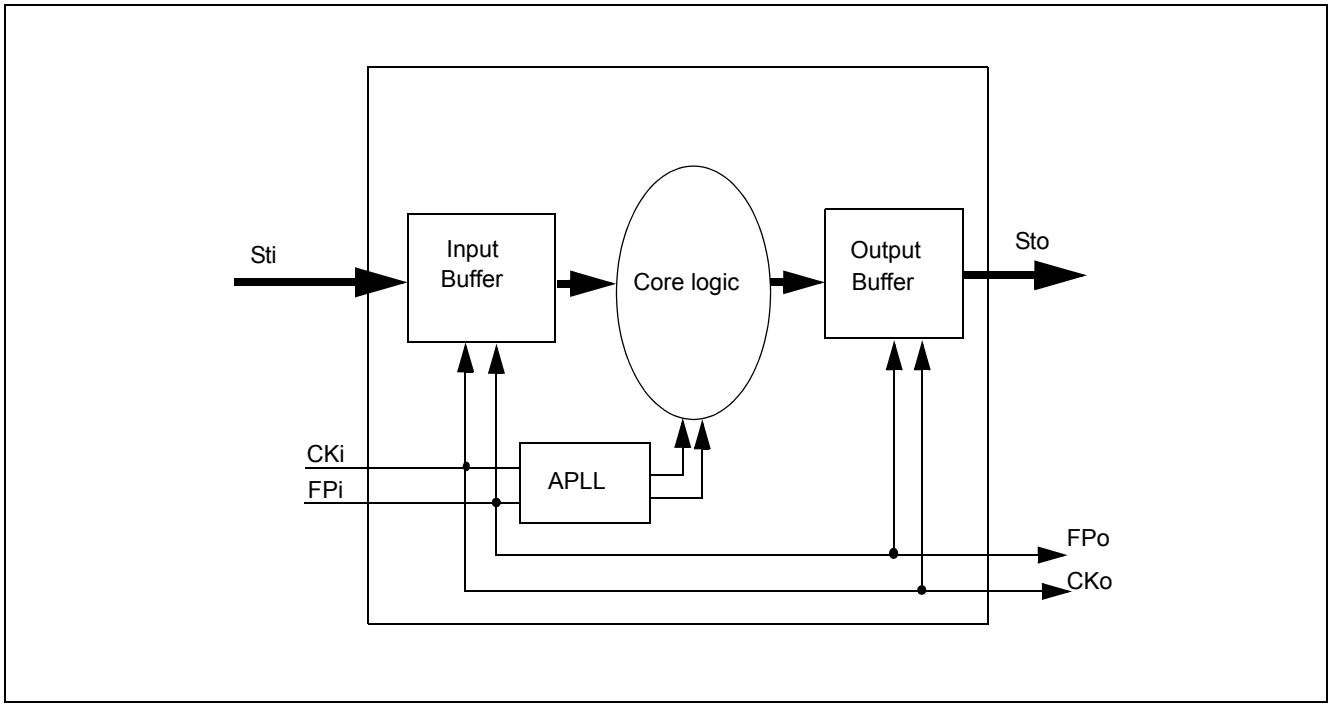

Figure 6 - Divided Slave Mode Internal Timing Block Diagram

Regardless of the jitter on the CKi clock, the output data stream Sto will not move relative to CKi because the Sto is clocked out with CKi.

This mode could be used in case where Sto is fed to another device as shown in Figure 9, timed by the same clock fed to CKi and sensitive to jitter between its input clock and data stream. Divided Slave mode should be used in applications where jittery timing master is used with Zarlink mid capacity switches running as timing slaves.

In this mode the maximum input and output data rate is limited by frequency of the clock fed to CKi and can not be higher than CKi

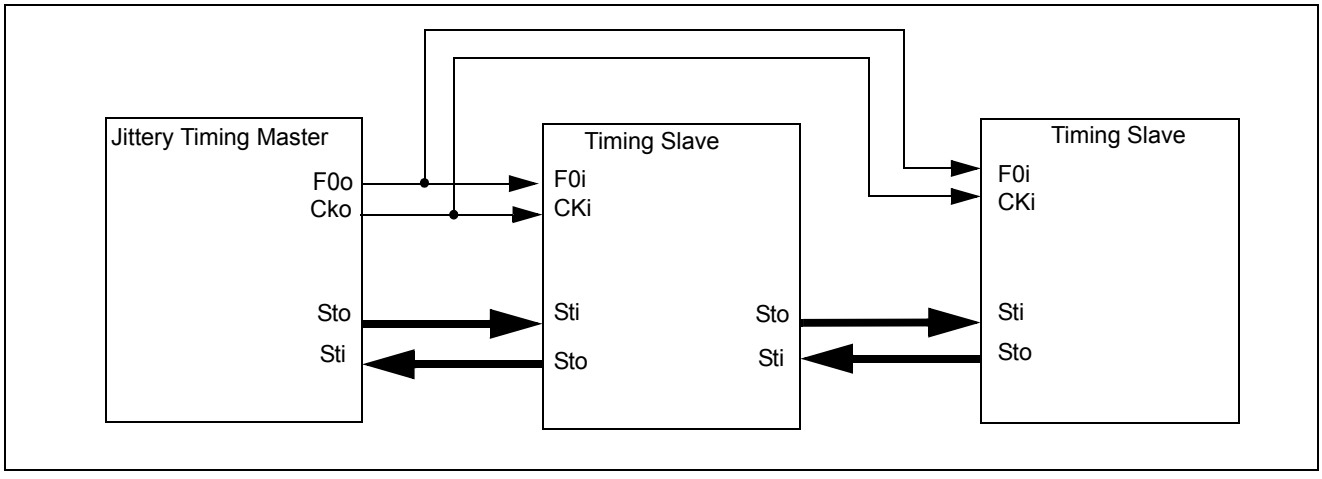

Figure 7 - Typical Application of Divided Slave Mode

5.0 Conclusion

Jitter tolerance is highly critical in modern digital switches where point to multi point data streams operate at rates up to 32.768 Mbps and where they are required to interoperate with older devices. Zarlink's mid capacity digital switches with one master and two slave timing modes offer excellent flexibility in systems where high jitter tolerance and low jitter generation is required.

This document describes typical timing master and slave operations in telecommunication systems. It describes the internal operation of Zarlink's new mid-density TSI switches with integrated DPLL. It also shows how these switches can be used in timing master and slave applications to reduce cost and improve flexibility.

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