Applications of the MT90220/221 Support for ATM over Fractional T1/E1

Application Note

June 2003

1.0 Introduction

Although the MT90220/221 was not designed to support ATM over Fractional T1/E, limited support for Fractional T1/E1 can be achieved with external circuitry.

This special mode is taking advantage of the facts that:

- the internal timeslot counter is PCM block for each T1/E1 link is reset each time a Frame Pulse signal is received
- each TX and RX PCM blocks are independent.

External circuitry is required to control the TX and/or RX PCM clock signal(s) to enable clocking of the serial data only during the number of timeslots to be used for the Fractional T1/E1 channel.

By controlling the position of the Frame Pulse within a Frame, it is possible to move the Fractional T1/E1 channel within the original T1/E1 frame. What needs to be done is to generate a frame pulse with some delay with respect to the basic T1/E1 Frame boundary. The delay has to be aligned with the timeslot boundary (multiple of 8 clock cycles). See Figure 1 for an example of two Fractional T1 channels; frame, clock and data signal positions, with respect to the T1 signal position.

The MT90220/221 PCM interface has to be programmed as follows:

- T1 PCM Generic mode,
- 2.048MHz clock, either positive or negative polarity
- Frame pulse with positive or negative frame pulse polarity
- grouped timeslot, using the first 24 timeslots of the 32 timeslots frame TDM I/F format
- all the PCM ports to be part of a Fractional T1/E1 have to have the same clock source

As external digital switch can be used to re-map the timeslots of the Fractional T1/E1 channels between the MT90220/221 and the T1/E1 Framers.

2.0 Limitations

- The Fractional T1/E1 channel is mapped to a continuous block of timeslots, starting at the frame pulse position.
- Only the T1 Generic Mode, grouped timeslot was fully verified.
- The DSTo output is not in High Impedance mode when the clock is stopped. This implies that external buffers with high impedance control are required if two or more DSTo outputs are wired or to be connected to a single T1/E1 framer.
- If no external buffer is implemented, a digital switch can be used to re-map the timeslots between the MT90220/221 and the framers. The use of a switch provides full support for the ATM over Fractional T1/E1 as defined in the IMA specification.

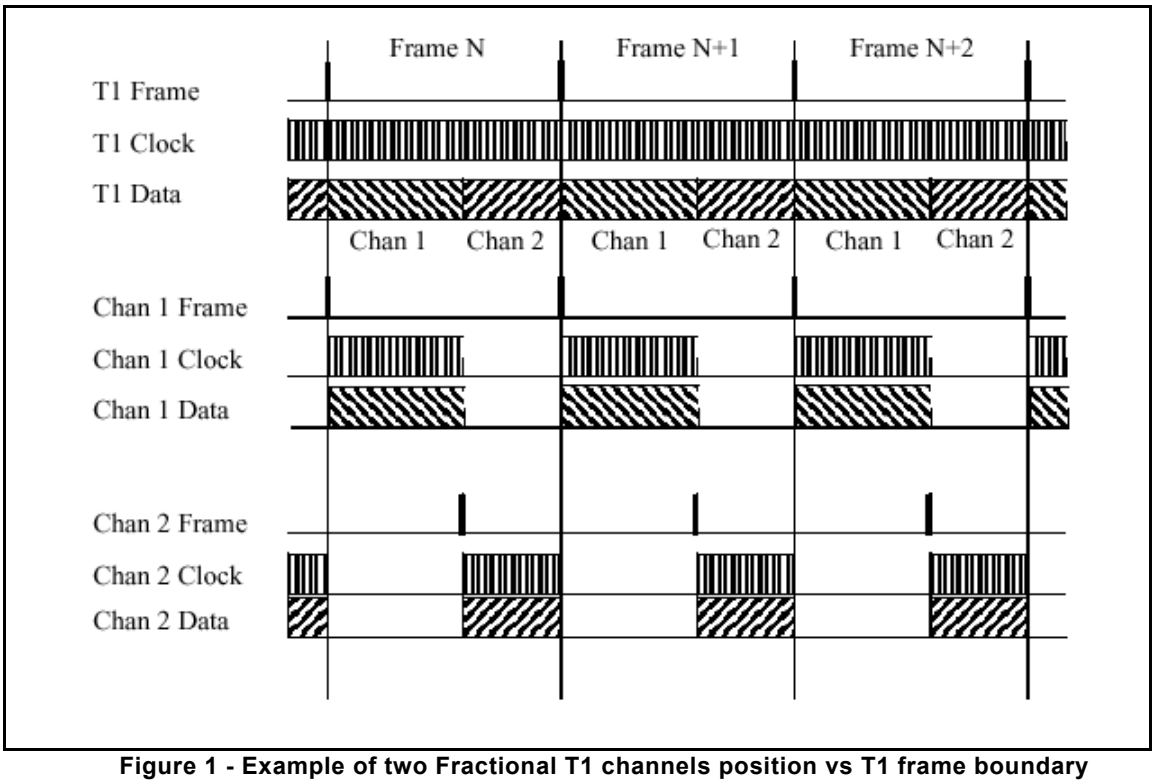

Figure 1 - Example of two Fractional T1 channels position vs T1 frame boundary

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE