

Contents

April 2003

1.0 Introduction

2.0 Why TDM Ring

3.0 Applications

3.1 Termination of DS3 Link

3.2 Maximizing the Flexibility in Grouping TDM Links

4.0 Ring Architecture

4.1 Pin-out

4.1.1 Tx Port

4.1.2 Rx port

4.2 Tx/Rx Link Connection

4.3 Ring Tx/Rx Link Registers

5.0 Ring Master

6.0 Ring Delay

1.0 Introduction

MT90224 is the second generation Inverse Multiplexing for ATM (IMA) device from Zarlink Semiconductor. Inheriting the architecture of first generation products, MT90224 is end-to-end

compatible with MT90220/221, but with the following enhancement:

- Single chip supporting 16 TDM links and 8 IMA groups
- Versatile TDM interface including T1, E1 fractional T1/E1 or DSL
- Utopia level 2 port
- A TDM ring for cascading multiple chips

This document discusses the application and operation of TDM ring.

2.0 Why TDM Ring

The main purpose of TDM ring is to allow the creation of an IMA group with links physically located on different MT90224 chips. The ring works like a cross-connect switch by which any TDM link of one IMA chip can be routed to any other chip in the ring, as shown in Figure 1.

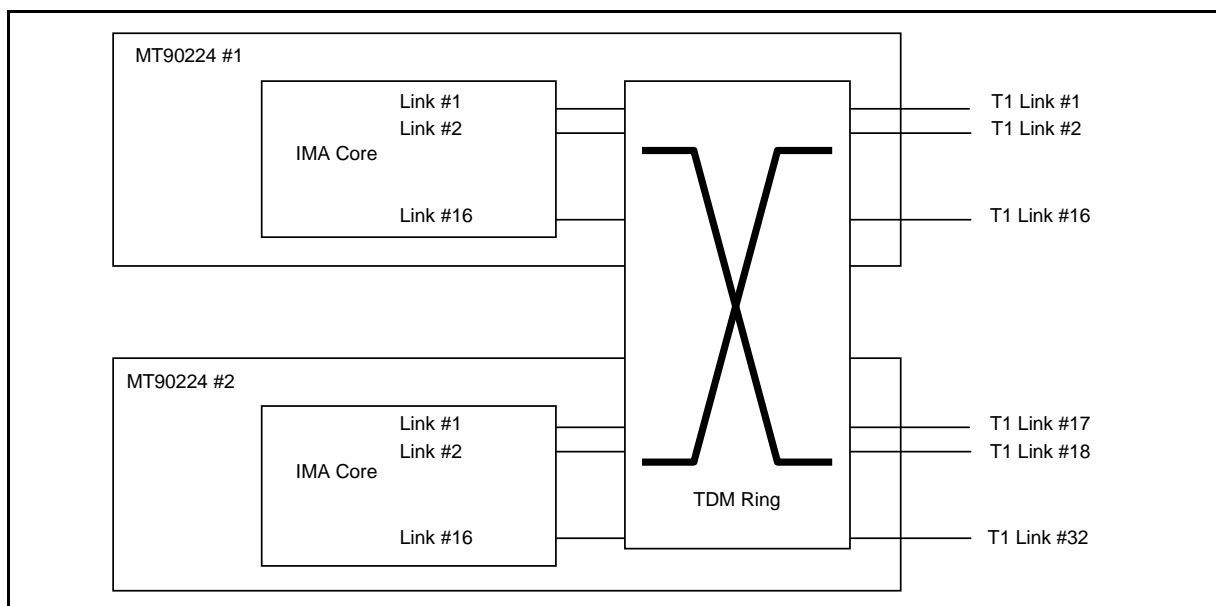


Figure 1 - TDM ring is like a cross-connect switch

3.0 Applications

There are several ways to take advantage of the TDM ring on MT90224. Two examples are shown below.

3.1 Termination of DS3 Link

Two MT90224 devices are needed to handle all 28 T1 links de-multiplexed from a DS3. Half of the links will be physically connected to the first MT90224, and the other half to the second MT90224. With the usage of TDM ring, it is possible to group T1 links from both MT90224 chips.

Without the presence of TDM ring, it would cost an external cross-connect switch to gain such flexibility.

3.2 Maximizing the Flexibility in Grouping TDM Links

With the presence of TDM ring, IMA core function inside one MT90224 becomes a resource not only available to those links physically connected to this particular device, but also available to all links attached on the TDM ring. Now the bandwidth is scalable and its usage can be maximized through the sharing of IMA resource and TDM link resource among the devices in the ring.

4.0 Ring Architecture

4.1 Pin-out

For each MT90224 device, TDM ring circuit consists of 10 output pins as Tx port and 10 input pins as Rx port.

4.1.1 Tx Port

TxRingClk	Ring clock output. It is used for clocking out TxRingData and aligning the TxRingSync. It is the same frequency of system clock, and is connected to the RxRingClk of the next MT90224 in the ring. If TDM ring is not used this output is in high impedance.
TxRingSync	Synchronization output. It is used for retrieving both data and control information from the TxRingData[7:0]. It is a clock signal at the half frequency of TxRingClk, and is connected to the RxRingSync of the next MT90224 in the ring. If TDM ring is not used this output is in high impedance.
TxRingData[7:0]	Data bus that contains transmit data and control information necessary for the ring to function. It is connected to the RxRingData of the next MT90224 in the ring. If TDM ring is not used this outputs are in high impedance.

4.1.2 Rx port

RxRingClk	Ring clock input. It is used for clocking in the RxRingData and RxRingSync. It is connected to the TxRingClk of the preceding MT90224 in the ring. There is an internal weak pull-up on this input.
RxRingSync	Synchronization input. It is connected to the TxRingSync of the preceding MT90224 in the ring. There is an internal weak pull-up on this input.
RxRingData[7:0]	Data input. It is connected to the TxRingData of the preceding MT90224 in the ring. There are internal pull-ups on these inputs.

4.2 Tx/Rx Link Connection

As shown in Figure 2, TDM ring is located between TC (transmission convergence) layer and physical layer inside MT90224. Specifically, it is attached between ICMCS (ICP Cell Modifier and Cell Scrambling) block and P/S (Parallel-to-Serial) circuit for transmit direction, and between CD (Cell Delineation) block and S/P (Serial-to-Parallel) circuit for receive direction.

Cells generated by ICSMS can be routed to P/S of another device via TDM ring, which is called Tx link connection (shown by solid gray line in Figure 2). Similarly, cells received from Rx links can also be routed to CD block of another device in the ring. This is called Rx link connection (dashed gray line in Figure 2).

Cells coming in from Utopia port are treated the same until they get out of ICMCS blocks, where they will either go to local Tx links or TDM ring. Cells arrive at CD blocks are all treated the same afterwards, regardless whether they are from TDM ring or local Rx links.

4.3 Ring Tx/Rx Link Registers

There are 32 TDM Ring Link registers (16 for Tx and 16 for Rx) for link connection.

Again, take Figure 2 as an example, to make a Tx link connection shown as gray solid line, one needs to:

1. Select a ring address (0 to 31) that is not currently being used. For example, address 9.
2. On MT90224_1, address 0x0190 (Ring Tx Link register for Tx link 15):
 - Set bit 11 to select ring mode
 - Assign ring address 9 to bits 10:6
3. On MT90224_2, address 0x0181 (Ring Tx Link register for Tx link 0):
 - Set bit 5 to select ring mode
 - Assign ring address 9 to bits 4:0

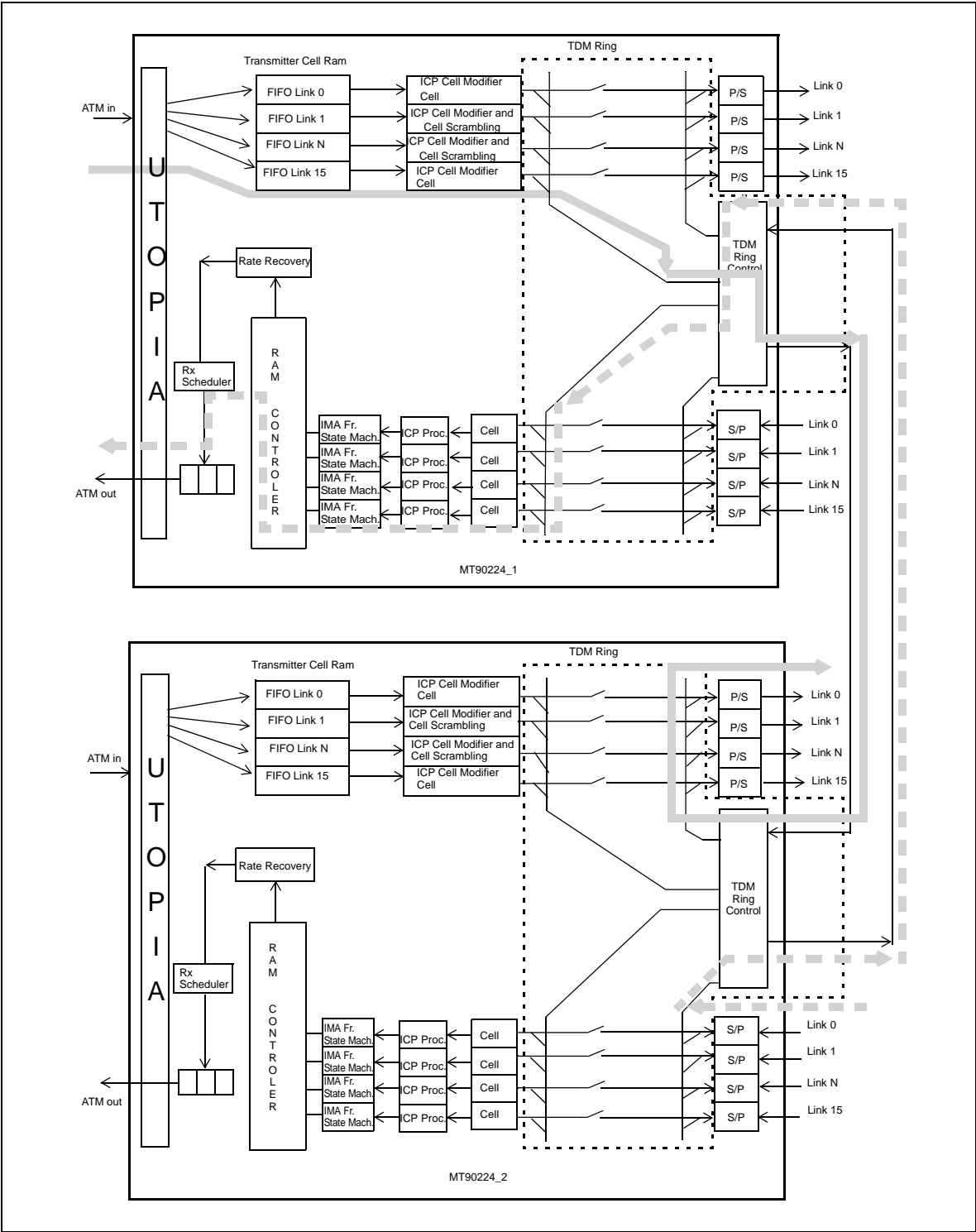


Figure 2 - Link Connection through TDM Ring

The same procedure can be applied to make an Rx link connection (dashed gray line) by programming Ring Rx Link registers, but a different ring address must be assigned.

Tx link connection and Rx link connection works independently, therefore, it is possible to establish asymmetrical operation, where the number of Tx link connections and the number of Rx link connections are not the same.

Up to 32 links, in each of the Tx and Rx, can be put onto the TDM ring. Each link must have a unique address. When those links are received at Rx port of the ring, MT90224 will scan all link addresses to see if they match any enabled address in its Ring Tx/Rx Link registers. Any link that matches a local address will be terminated and dropped off the ring. The rest will be transparently passed over to Tx port of the ring, where they will be multiplexed with the locally generated new links and sent to the next device on the ring. Such a case is illustrated in Figure 3.

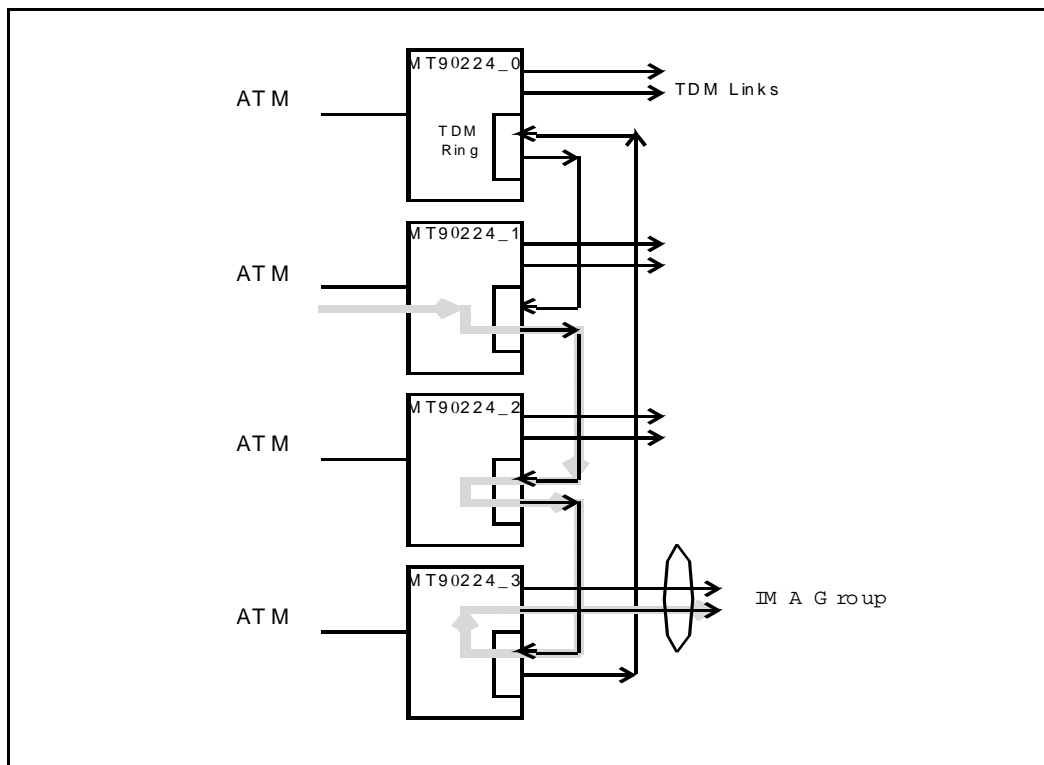


Figure 3 - Multiple MT90224 Connected in a TDM Ring

If a connection traverses multiple devices, only the registers on source and destination devices need to be programmed. Devices in between them will pass it through transparently.

5.0 Ring Master

In a TDM ring, only one of the devices must be configured as the ring master. Ring master is selected through Ring Control Register (0x180). The ring clock comes from the system clock of the ring master. It is important that system clocks of all the MT90224 devices in the ring must be synchronous, that is, they must be of the same frequency but they can be with different phase.

Ring master is responsible for initialization and maintenance of the ring. Set bit 1 in Ring Control register for more than 1ms will initialize the ring. Maintenance is performed by ring master without any user intervention.

6.0 Ring Delay

Delay is introduced when data passes through the TDM ring. For Tx link connection, it becomes a critical factor because data byte must arrive at destination Tx link in time before its timeslot is gone. For example, at E1 link, one byte is transmitted out every 3.9us; hence the total delay caused by TDM ring must not exceed 3.9us.

Total ring delay consists of two types: bypass delay and process delay. Bypass delay is introduced by MT90224 to all data that passes through it. It is the time when data comes into Rx ring until it gets out of Tx ring. The bypass delay of the whole ring is approximately equal to:

$$\text{bypass_delay} = \text{number_of_devices_in_the_ring} * 6_ring_clock_cycles$$

The process delay, however, is introduced by source device only when a link is to be inserted into the ring. It is the time a link has to wait before it can find a free slot on the ring. This delay time is affected by the load on the ring. In the worst case, we have:

$$\text{process_delay} = \text{number_of_links_in_the_ring} * 4_ring_clock_cycles.$$

Total delay is obtained by summing up bypass_delay and process_delay.

Given that ring clock cycle is 20ns, maximum number of links that can be in a ring is 32, and maximum allowed delay is 3.9us, we can conclude that the number of MT90224 devices in a ring is 11 in this case.

As a general rule, it is recommended that the maximum number of MT90224 devices connecting to a TDM ring be no more than 6.

In above calculation, the propagation delay around the ring is assumed to be negligible when compared with ring clock cycle. If that's not the case, propagation delay should also be considered as part of total delay.



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
