

Contents

December 2010

1.0 Introduction

2.0 Power Supply Decoupling and Layout Practices

1.0 Introduction

This document details the recommended power supply decoupling and device layout practices for the ZL30130, ZL30131, ZL30138, ZL30321, ZL30132, ZL30133, ZL30134, ZL30136, ZL30142, ZL30143, ZL30145, ZL30146, ZL30342, ZL30343 and ZL30347.

2.0 Power Supply Decoupling and Layout Practices

Jitter levels on the ZL30130, ZL30131, ZL30138, ZL30321, ZL30132, ZL30133, ZL30134, ZL30136, ZL30142, ZL30143, ZL30145, ZL30146, ZL30342, ZL30343 and ZL30347 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins as shown in Figure 1 for the 100 pin ZL30130, ZL30131, ZL30138, ZL30321, ZL30143, ZL30343, ZL30347, Figure 2 for 64 pin ZL30132, ZL30133, ZL30134, ZL30136, ZL30142, ZL30145, ZL30146, ZL30342 and Figure 3 for the 256 pin ZL30321.

The following common layout practices are recommended for improved power rail noise rejection.

- Each power island should have a bulk cap of at least 10 μF with very low ESR. Ceramic provides the lowest ESR but tantalum may also be acceptable. These capacitors are used to filter low frequency (up to several hundreds KHz) noise that originate from switching power supplies. If the switching power supply is not filtered with large bulk capacitances (100 μF or more), then the 10 μf capacitors used for 1.8 V core voltage supplies (AV_{CORE} and V_{CORE}) should be replaced with low ESR 100 μF ceramic or tantalum capacitors.
- A 0.1 μF decoupling cap (ceramic X5R or X7R) must be allocated for each power pin and placed as close as possible to the via connected to the power pin. The smallest available package size should be used. Each decoupling cap should be connected directly to only one power pin, and should not share vias to power or ground with other caps.
- Priority should be given to placement of decoupling caps in nearest proximity to AV_{DD} and AV_{CORE} pins.
- AV_{CORE} pins B7 and H2 in Figure 1 and pins B6 and F1 in Figure 2 draw 25 mA each. This requires the series resistor to dissipate at least 1.25 mW of power.
- Two "power islands" should be created for the device, one for 3.3 V and the other for 1.8 V. A power island is a local copper area, separated from the main power plane by a series passive component. Its purpose is to provide improved isolation from noise on the board power planes. Ferrite beads provide additional suppression of digital switching noise generated by other integrated circuits connected to the main power planes. A recommended bead is Murata BLM21AG102SN1 or similar. Note that beads have some DC resistance which increases the minimum required supply voltage for the device (by about 1% for the above bead).

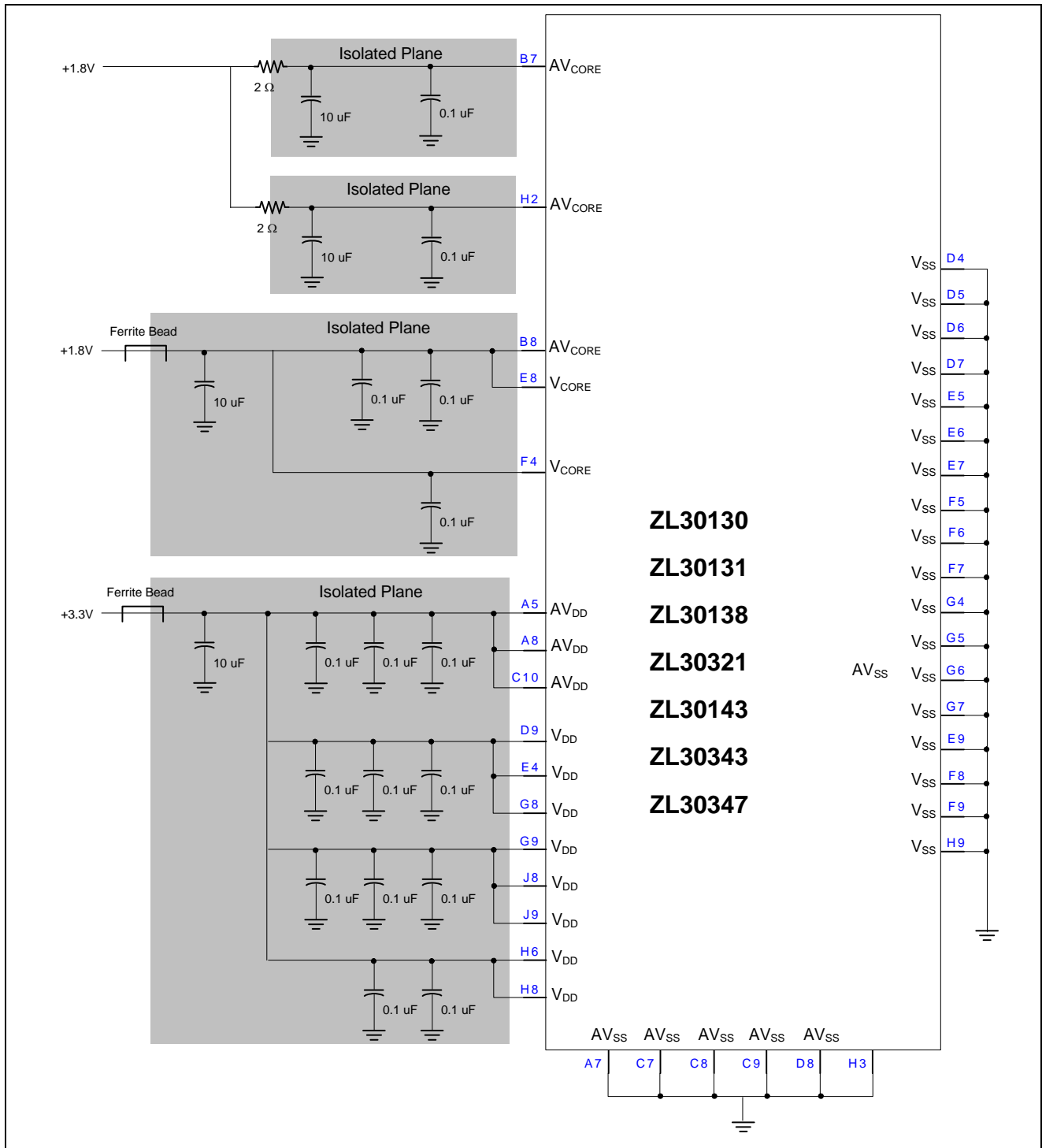


Figure 1 - Power Supply Decoupling for the 100 pin ZL30130, ZL30131, ZL30138, ZL30321, ZL30143, ZL30343 and ZL30347

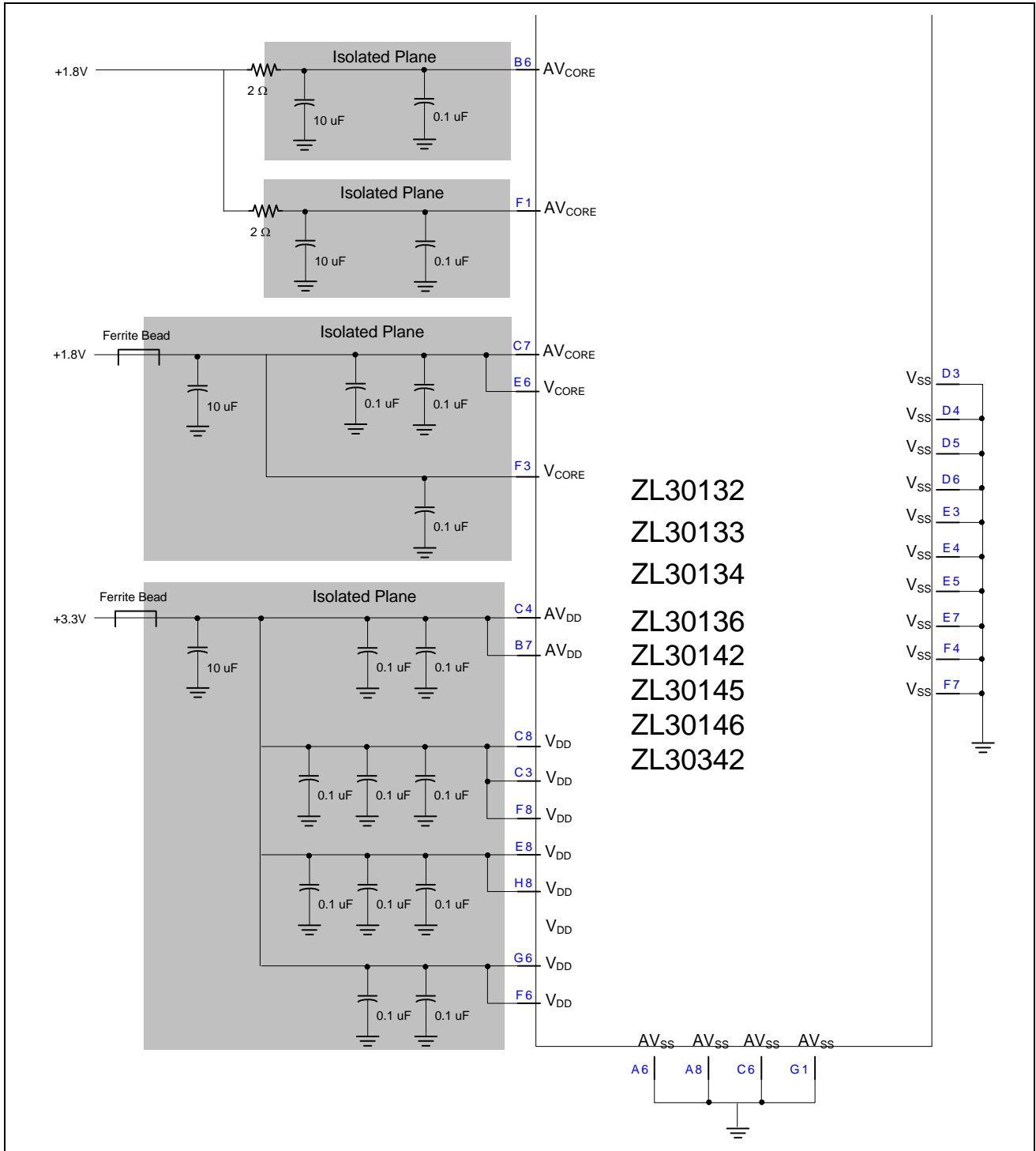


Figure 2 - Power Supply Decoupling for the 64 pin ZL30132, ZL30133, ZL30134, ZL30136, ZL30142, ZL30145, ZL30146 and ZL30342

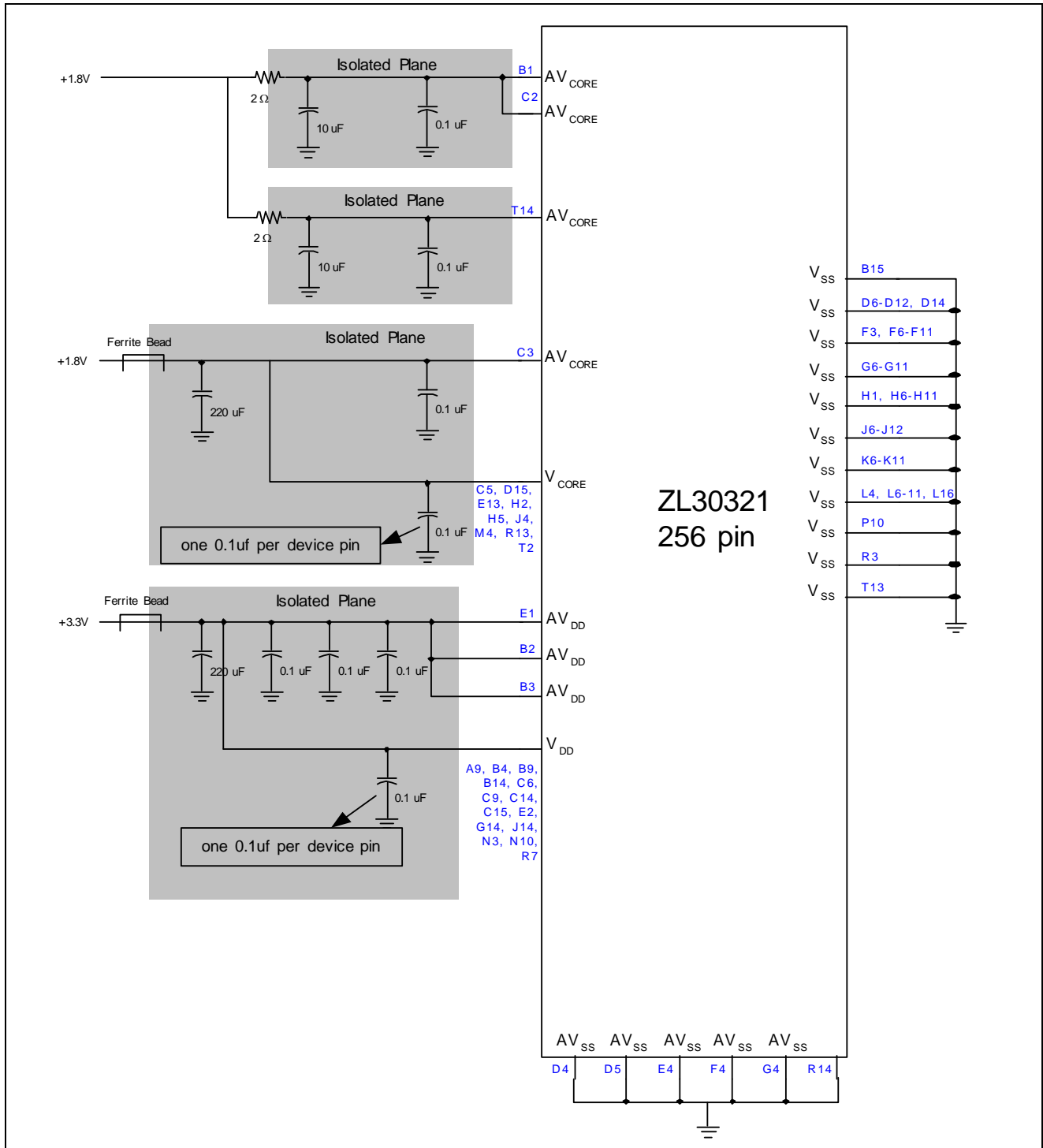


Figure 3 - Power Supply Decoupling for the 256 pin ZL30321



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a license under the Philips I²C Patent rights to use these components in an I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL, the Zarlink Semiconductor logo and the Legerity logo and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Zarlink Semiconductor Inc.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
