ZLAN-199

Applications of the ZL3011x/12x Programming Custom Input References

Application Note

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Contents

1.0 Introduction

The ZL3011x/12x family of DPLLs can automatically detect and monitor a number of common telecom input clock frequencies at their REF inputs. These frequencies include:

2 kHz, 8 kHz, 64 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 Mhz, 38.88 MHz, and 77.76 MHz.

While the device will only automatically detect and qualify these frequencies, the ZL3011x/12x can synchronize to a 2 kHz clock or any n * 8 kHz frequency up to 77.76 MHz.

This application note will examine how to program the DPLL to qualify and synchronize to a custom defined input reference.

2.0 Reference Configuration

The ZL3011x/12x allows the use to define 2 separate custom input reference definitions (CustomA and CustomB), and either of these custom definitions may be applied to any of the devices REF inputs. The ref_freq_mode_0 (address 0x66h) and ref_freq_mode_1 (address 0x67h) registers can be programmed to set each individual REF input (REF0...REF7) to either the default auto_frequency detect or either of the custom configurations. When a REF input is set to one of the custom configurations it will not recognize the pre-set auto detect frequencies as valid input references, only clocks running at the programmed custom frequency will be declared valid and available for synchronization.

3.0 Custom Input Definition

Registers 0x67h to 0x70h are used to define the CustomA configuration and addresses 0x71h to 0x7Ah are used to define the Custom B configuration. In addition to the input frequency the custom definitions require the user to program the upper and lower limits of the different references monitoring circuit available in the ZL3011x/12x.

3.1 Input Frequency

The nominal input frequency for the 2 custom input configurations are programmed via a 14 bit multiplier (n) in the ZL3011x/12x's register map, where,

$$\mathrm{DesiredInputFrequency} = n \times 8\mathrm{kHz}$$

Valid values for n range from 0 to 0x25F8h. When n = 0, input frequency = 2 kHz. For custom configuration A, the multiplier is defined in registers custA_mult_0 and custA_mult_1 (addresses 0x67h and 0x68h), while the custom B multiplier is defined in registers custB_mult_0 and custB_mult_1 (addresses 0x71h and 0x72h).

3.2 Reference Monitoring

The ZL3011x/12x has 4 main circuits that monitor the input references to ensure accuracy and phase regularity. New references are qualified using these reference monitoring circuits before they are available for use as the synchronization source, they are also continuously monitored to ensure they remain suitable for use by the PLL. The 4 reference monitoring circuits are the PFM (precise frequency monitor), the SCM (single cycle monitor) and CFM (coarse frequency monitor) and the GST (Guard Soak Timer). When operating in the auto frequency detect mode (i.e. not using the custom configuration), the user must define the PFM range for each individual references (via the oor_ctrl registers at addresses 0x16h, 0x17h, 0x18h, 0x19h). The qualification and disqualification times of the GST must also be programmed via the gst_qualif_time register at 0x1Ch. In the custom configuration, these parameters are programmed the same way, using the same registers. In auto frequency detect mode the SCM and PFM limits are predefined, but in the custom configuration these limits must be programmed by the user.

3.2.1 SCM

The SCM (Single Cycle Monitor) monitors each reference clock cycle to detect phase irregularities or a missing clock edge. The Period limits for the SCM can be programmed between 0 and 850 ns, and they correspond to the lowest and highest acceptable clock period for each cycle of the input reference. Unless your application has a specified limits for a single cycle period deviation, it is recommended to set the device to signal a SCM failure if any single period deviates from nominal by more than 50%. The SCM limits for the customA configuration are set using the custA_scm_low (0x69h) and custB_scm_high (0x6Ah) registers. The SCM limits for the customB configuration are set using the custB_scm_low (0x73h) and custB_scm_high (0x74h) registers. The SCM monitor is clocked by an internal 300 MHz clock, therefore to program the registers, the following equations should be followed;

$$\mathrm{SCMlowerlimit} = a \times \frac{1}{300\mathrm{MHz}}$$

$$\mathrm{SCMupperlimit} = b \times \frac{1}{300\mathrm{MHz}}$$

where a = the decimal value in custA_scm_low or custB_scm_low register, and b = the decimal value in custA_scm_high or custB_scm_high register.

For low speed input references less than 1.544 MHz, the SCM counter does not provide enough range to reliable perform its function. Therefore for custom inputs of less than 1.544 Mhz the device should be set to mask all SCM failures on references using the custom configurations. This can be done via the ref_mon_fail_mask registers (0x0Ch, 0x0Dh, 0x0Eh, 0x0Fh).

3.2.2 CFM

The CFM monitor monitors the reference frequency over a longer measurement period and is designed to quickly detect large changes in frequency.

The measurement period can be programmed to be from 1 to 256 clock cycles of the input reference via the custA_cfm_cycle (0x6Fh) and custB_cfm_cycle(0x79h) registers.

$$\mathrm{CFMreferencemonitoringcycles} = c + 1$$

where c = the value of the custA_cfm_cycle (0x6Fh) or custB_cfm_cycle(0x79h) register. Since the SCM counter does not provide sufficient range for input frequencies that are less than 1.544 MHz, the CFM should be programmed to act as a single cycle monitor by setting the #CFM reference monitoring cycles to 1 (c=0). Multiple cycle measdurements are not required for these slower frequencies.

The CFM monitor is sampled using an internal 80 MHz clock, for higher speed input references the CFM monitor may not see enough input clock cycles per 80 MHz sample in order to provide accurate, reliable results, therefore it may be necessary to first divide down the high speed input reference before it is fed to the CFM circuit. This can be accomplished via the custA_div (0x70h) and custB_div (0x7Ah) registers. Setting bit 0 = 1 in these registers will divide the input reference by 4 before it is sent to the CFM circuitry. It is recommended that references greater than 19.44 MHz be divided down.

The Period limits for the CFM can be programmed between 0 and 819.1875 us, and they correspond to lowest and highest acceptable period for (c+1) input clock cycles. Typically, unless your application has specific requirements, it is recommended to set the device to signal a CFM failure if the measurement period deviates from nominal by more than 3%. The CFM limits for the customA configuration are set using the custA_cfm_low (0x6Bh and 0x6Ch) and custA_cfm_hi (0x6Dh and 0x6Eh) registers. The SCM limits for the customB configuration are set using the

custB_cfm_low (0x75h and 0x76h) and custB_scm_high (0x77h and 0x78h) registers. To program the registers, the following equations should be followed

$$CFMlowerlimit = d \times \frac{1}{80MHz}$$

$$CFMupperlimit = e \times \frac{1}{80MHz}$$

where d = the decimal value of the custA_cfm_low (0x6Bh and 0x6Ch) or custB_cfm_low (0x75h and 0x76h) registers, e = the decimal value of the custA_cfm_hi (0x6Dh and 0x6Eh) or custB_cfm_low (0x77h and 0x78h) registers.

4.0 Example

The following example application calls for a 25 MHz input reference to be applied to the REF0 and REF1 inputs of a ZL30116:

Input Selection

Custom A Input reference = Ref0 and Ref1

Input Frequency

n * 8kHz = 25MHz

n = 3125 = C35h

SCM limits

SCM limits = +/-50%

SCM lower Period limit = 1/2(nominal 25 MHz clock period)

= 1/2(40 ns) = 20 ns

= a * 1/300 MHz

a = 6 = 6h

SCM Upper Period limit = 1.5(nominal 25 MHz clock period)

= 1.5(40 ns) = 60 ns

= b * 1/300 MHz

b = 18 = 12h

CFM Limits

Since input frequency > 19.44 MHz, the divide by 4 circuit is enabled. Therefore the input frequency for the CFM circuit = 6.25 MHz.

As a general rule the measurement period should be between 10 and 30usec therefore,

CFM reference monitoring cycles = c + 1 = 128

c = 127 = 7Fh

CFM limits of +/-3%

CFM lower Period limit = 0.97(period of 128 6.25 MHz clock cycles)

= 0.97(20.48 us) = 19.865 us

= d * 1/80 MHz

d = 1589.248 = 1589 = 635h

CFM Upper Period limit = 1.03(period of 128 6.25 MHz clock cycles)

= 1.03(20.48 us) = 21.0944 us

= e * 1/80 MHz

e = 1687.552 = 1688 = 698h

Register Programming

Address	Register Name	Value	Comments
65h	ref_freq_mode_0	**00000101 = 05h**	Sets REF0 and REF1 to customA configuration
67h	custA_mult_0	**00110101 = 35h**	
68h	custA_mult_1	**00001100 = 0Ch**	14 bit n*8 kHz multiplier = C35h
69h	custA_scm_low	**00000110 = 06h**	Lower SCM period Limit = Nominal - 50%
6Ah	custA_scm_high	**00010010 = 12h**	Upper SCM period Limit = Nominal - 50%
6Bh	custA_cfm_low_0	**00110101 = 35h**	
6Ch	custA_cfm_low_1	**00000110 = 06h**	Lower CFM limit = Nominal -3%
6Dh	custA_cfm_hi_0	**10011000 = 98h**	
6Eh	custA_cfm_hi_1	**00000110 = 06h**	Upper CFM limit = Nominal +3%
6Fh	custA_cfm_cycle	**01111111 = 7Fh**	# CFM reference monitoring cycles = 128
70h	custA_div	**00000001 = 01h**	Enables divide by 4 circuit for CFM circuitry

Table 1 - Programming a Custom 25 MHz Input to REF0 and REF1

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