ZLAN-178

Synchronizer Power Supply Decoupling and Layout Practices

Application Note

November 2007

Contents

1.0 Introduction

This document details the recommended power supply decoupling and device layout practices for the ZL30100, ZL30101, ZL30102, ZL30105, ZL30106, ZL30109 and ZL30111 64 pin synchronizers; and the ZL30108, ZL30110 and ZL30112 32 pin synchronizers.

2.0 Power Supply Decoupling for 64 Pin Devices

Jitter levels on the ZL30100, ZL30101, ZL30102, ZL30105, ZL30106, ZL30109 and ZL30111 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins as shown in Figure 1 and as described in Section 4.0.

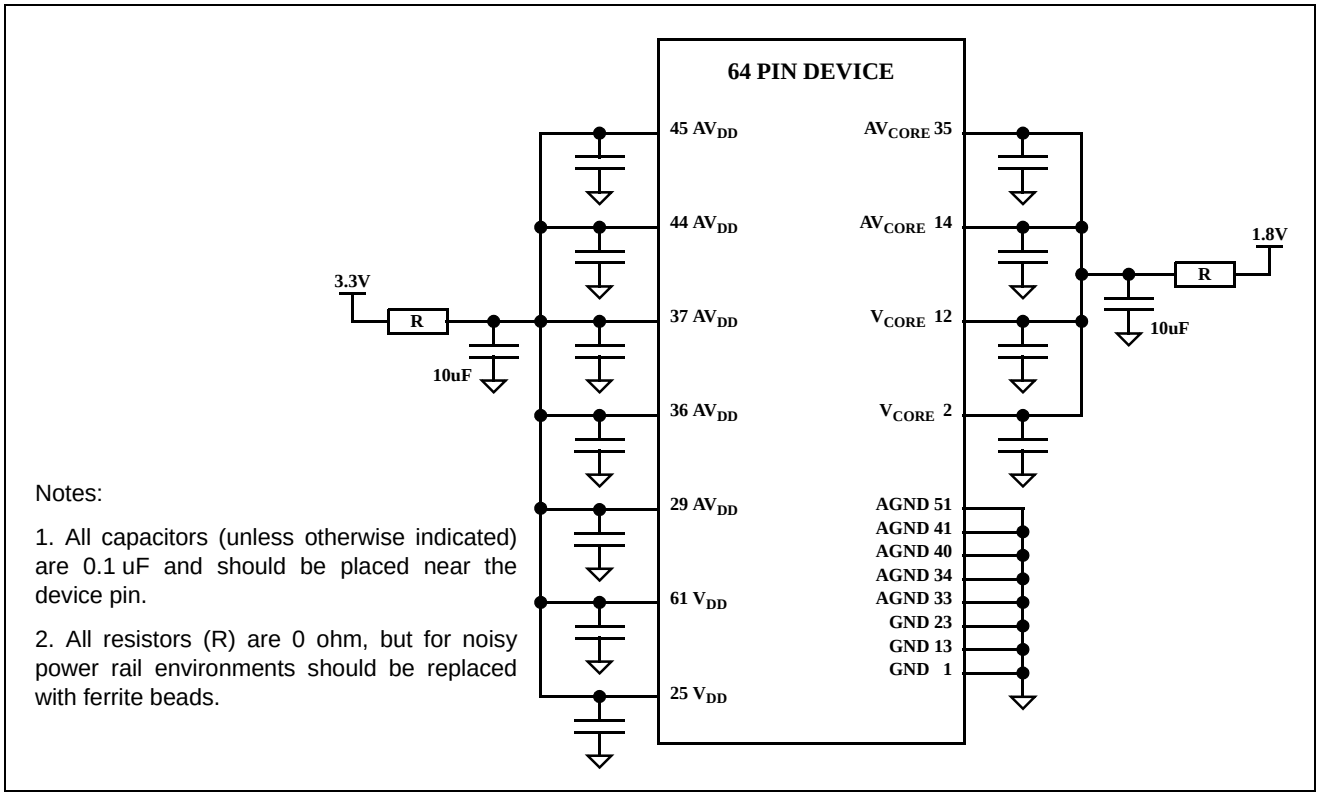


Figure 1 - Recommended Power Supply Decoupling

3.0 Power Supply Decoupling for 32 Pin Devices

Jitter levels on the ZL30108, ZL30110 and ZL30112 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins as shown in Figure 2 for ZL30108 and ZL30112 and in Figure 3 for ZL30110.

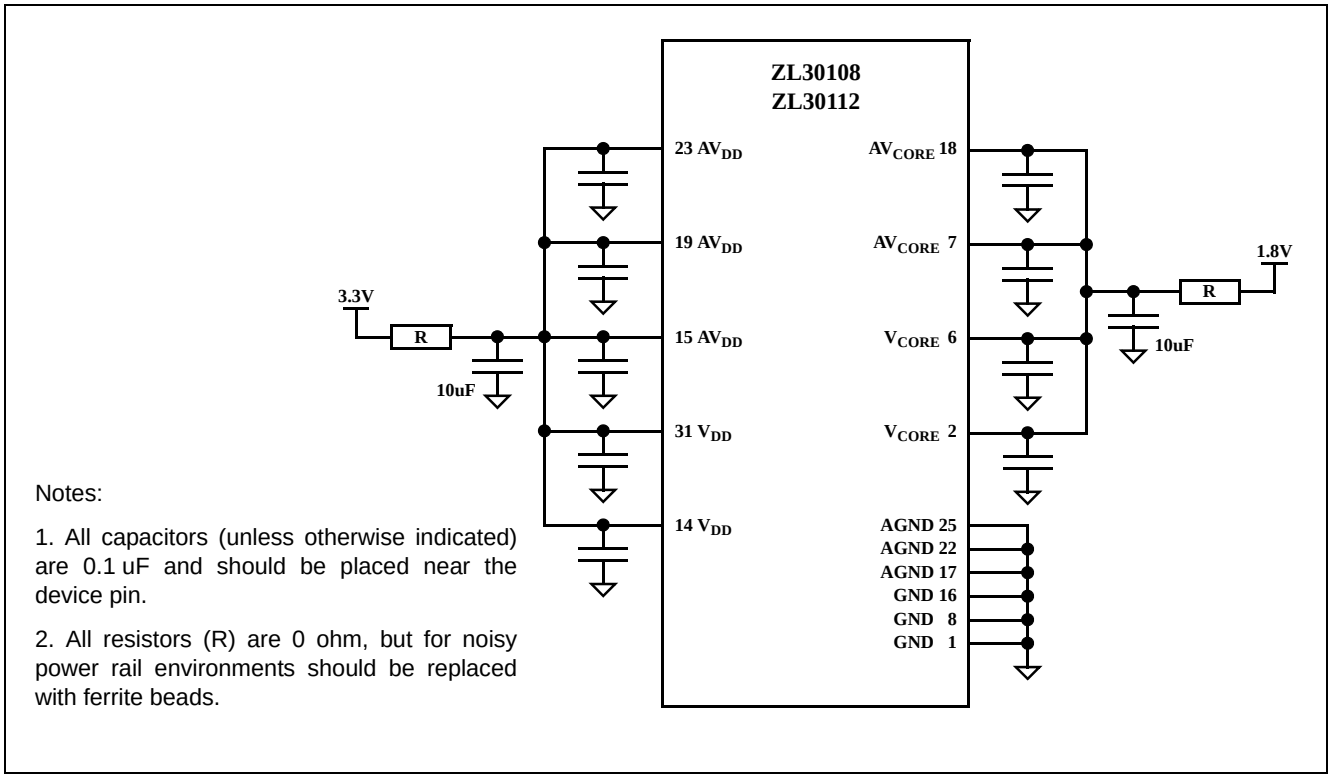
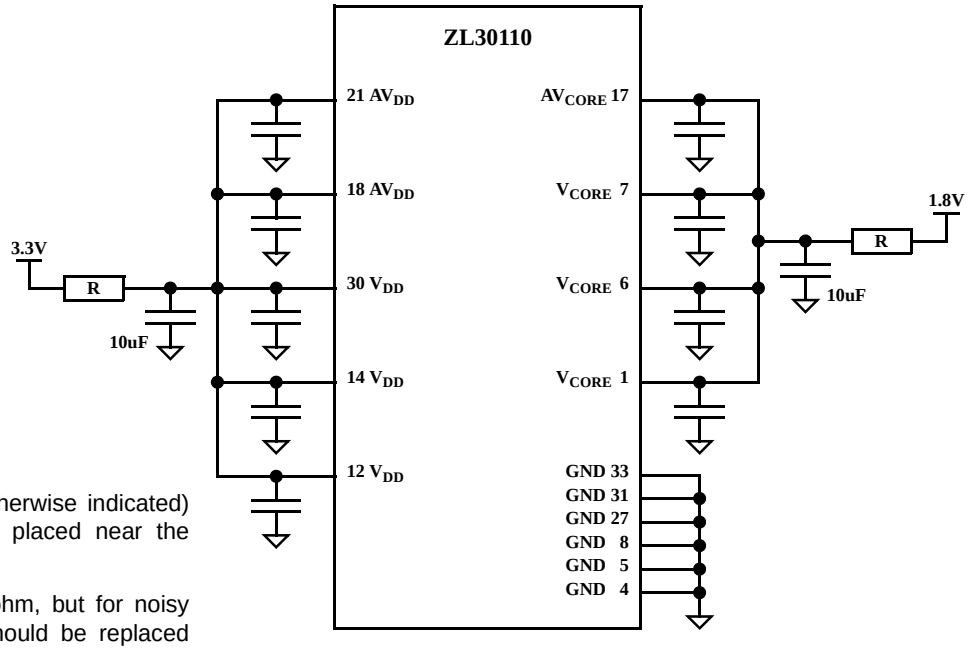


Figure 2 - Recommended Power Supply Decoupling for ZL30108 and ZL30112



Notes:

1. All capacitors (unless otherwise indicated) are 0.1 uF and should be placed near the device pin.

2. All resistors (R) are 0 ohm, but for noisy power rail environments should be replaced with ferrite beads.

Figure 3 - Recommended Power Supply Decoupling for ZL30110

4.0 Common Recommended Layout Practices

The following common layout practices are recommended for improved power rail noise rejection.

- Two "power islands" should be created for the device, one for 3.3 V and the other for 1.8 V. A power island is a local copper area, separated from the main power plane by a series passive component. Its purpose is to provide improved isolation from noise on the board power planes. Ferrite beads provide additional suppression of digital switching noise generated by other I.C.'s connected to the main power planes. A recommended bead is Murata BLM21A102S or similar. Note that beads have some resistance which increases the minimum required supply voltage for the device (by about 1% for the above bead).
- Each power island should have a bulk cap of at least 10 uF with very low ESR. Ceramic provides the lowest ESR but tantalum may also be acceptable.
- A 0.1 uF decoupling cap (ceramic X5R or X7R) must be allocated for each power pin and placed as close as possible to the pin. The smallest available package size should be used. Each decoupling cap should be connected directly to only one power pin, and should not share vias to power or ground with other caps.
- Priority should be given to placement of decoupling caps in nearest proximity to AVDD and AVCORE pins.
- The optimal placement for each 0.1 uF decoupling cap is on the same side of the board as the DPLL device, between the power pin and the via connecting to the local power plane. Placement of all caps on the opposite side of the board is acceptable.
- Ground vias should be placed very close to the device ground pins to minimize inductance between the device pins and the ground plane.