SLIC FAMILY FUNCTIONAL DESCRIPTION

Zarlink's SLIC device family has grown and includes device operating characteristics and options not previously available. Current offerings also include new choices of power management and DC feed control to address needs of major telephony markets. Although certain features may be unique to a specific SLIC device type, all Zarlink SLICs are based on and contain the same functional blocks. The following sections describe, in detail, the operation of each of these blocks.

Two-Wire Interface

The function of the two-wire interface is to provide DC current and to send voice signals to a telephone apparatus connected to the linecard with a two-wire line. The two-wire interface also receives the returning voice signals from the telephone transmitter.

The typical two-wire interface (see Figure 1) consists of two current mode line-driver amplifiers, line-voltage sensing circuits with AC/DC pass separation, and a loop-current sensing circuit.

The current mode amplifiers driving the A(TIP) and B(RING) pins are controlled by two input signals, I_{LI} and I_{MI}. I_{LI} controls the longitudinal (common mode) current, and I_{MI} controls the metallic (differential) current.

The two-wire currents are:

$$I_{AX} = K_1(I_{LI} + I_{MI}) \text{ and } I_{BX} = K_1(I_{LI} - I_{MI})$$

Where: K_1 is the internal current mode amplifier gain.

I_{MI} is equal to the current into the Receive Summing Node (RSN), which is the terminating point for the external networks controlling two-wire impedance, receive gain, battery feed, and metering gain (in metering versions). These networks are described in detail later. I_{LI} controls the longitudinal line current to obtain the optimum common mode DC operating point for the current mode amplifiers.

The voltage sense signal (V_{ACMET}) that goes to the signal transmission block is the AC metallic component of the A and B voltages.

Two voltage sense signals ($|V_{DCMET}|$ and V_{LONG}) go to the power feed controller block. V_{DCMET} is the DC metallic component of the A and B voltages. V_{LONG} is the longitudinal component of the A and B voltages.

An external capacitor (C_{HP}), connected between HPA and HPB, separates the AC and DC components of the metallic voltage. Because the time constant could be too long during polarity reversal or pulse dialing, the two-wire interface can have a shorting circuit that decreases the time constant during these events.

The loop-current sensing circuit produces a current (I_D) that is proportional to the magnitude of the loop current and is output to the RD pin. An external resistor and filter capacitor connected to RD converts this current to a filtered voltage for use by the off-hook detector.

Note: *This describes the two-wire interface for most of Zarlink's SLIC devices. Minor differences may exist on certain device types, but all follow this general format and operation.*

Signal Transmission

Figure 2 provides more detail of the SLIC transmission path. This path is split between the signal transmission block and the two-wire interface block.

The AC line voltage is sensed by differential amplifiers between the A and HPA leads, and between the HPB and B leads. The outputs of these amplifiers are equal to the AC metallic components of the line voltages. These voltages are summed and buffered by the op amp G_{TX}. G_{TX} in dB is specified in each data sheet under two- to four-wire gain accuracy. For metering applications, G_{TX} is typically –6.02 dB to avoid overload during metering signal transmission. Longitudinal voltages are rejected by the differential amplifiers and only affect V_{TX} to the extent of the longitudinal balance specification.

The balance return signal on V_{TX} exhibits 180° phase shift with respect to V_{RX}. This allows the two-wire AC input impedance to be programmed by means of an external impedance that is connected between RSN and V_{TX} (see Figure 2). This impedance may be a complex R-C network and should be K_1 times the desired two-wire input impedance minus K_1 times the fuse resistors. This means resistors become K_1 times larger and capacitors become K_1 times smaller. Note that any external stray capacitance between V_{TX} and RSN must be included in Z_T when precise computations for output impedance, gain, transhybrid loss, or return loss are being made.

$$Z_T = K_1 \bullet G_{TX}(Z_{2WIN} - 2R_F)$$

Where: Z_{2WIN} = desired two-wire impedance

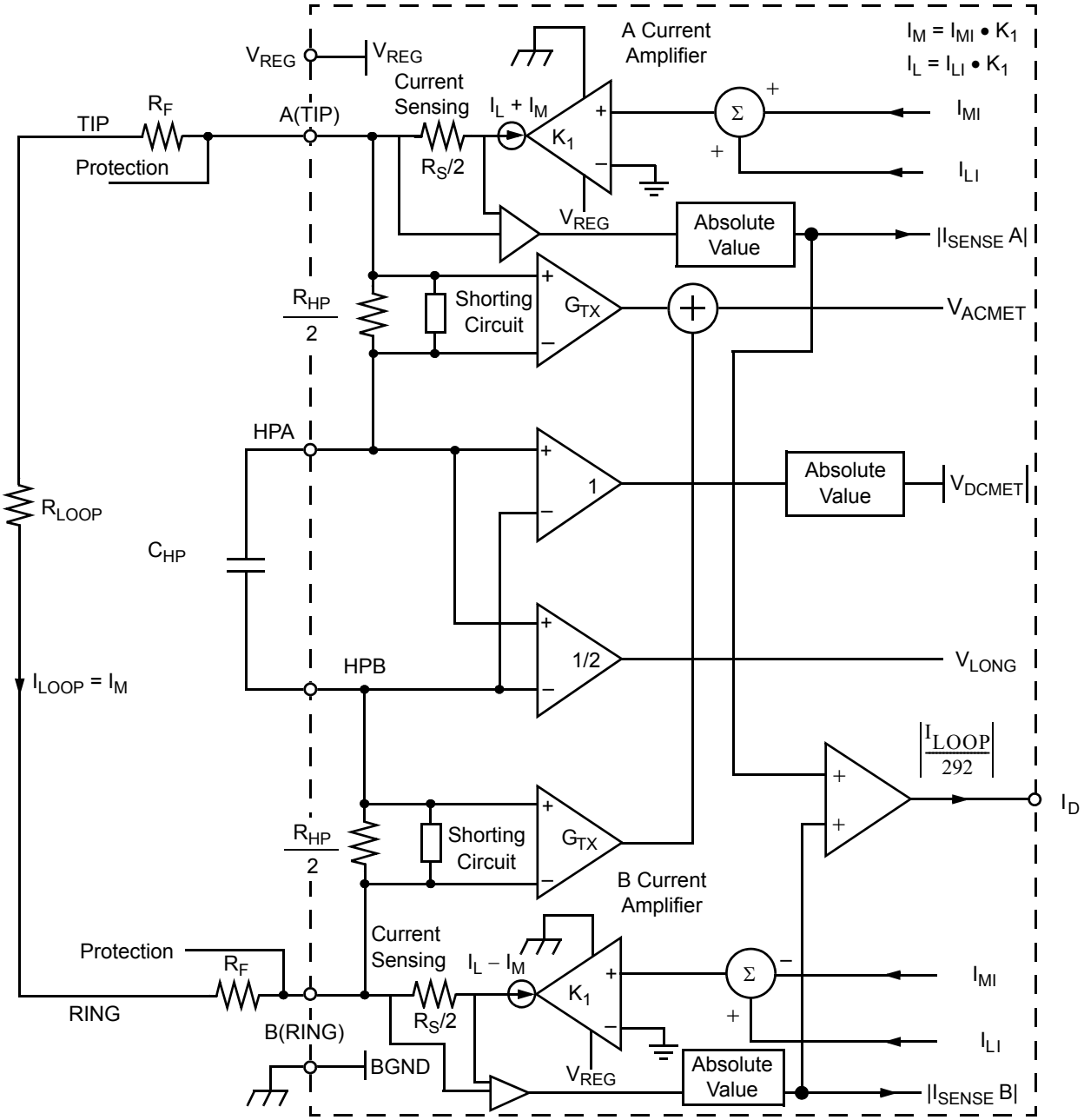


Figure 1. Two-Wire Interface (Typical)

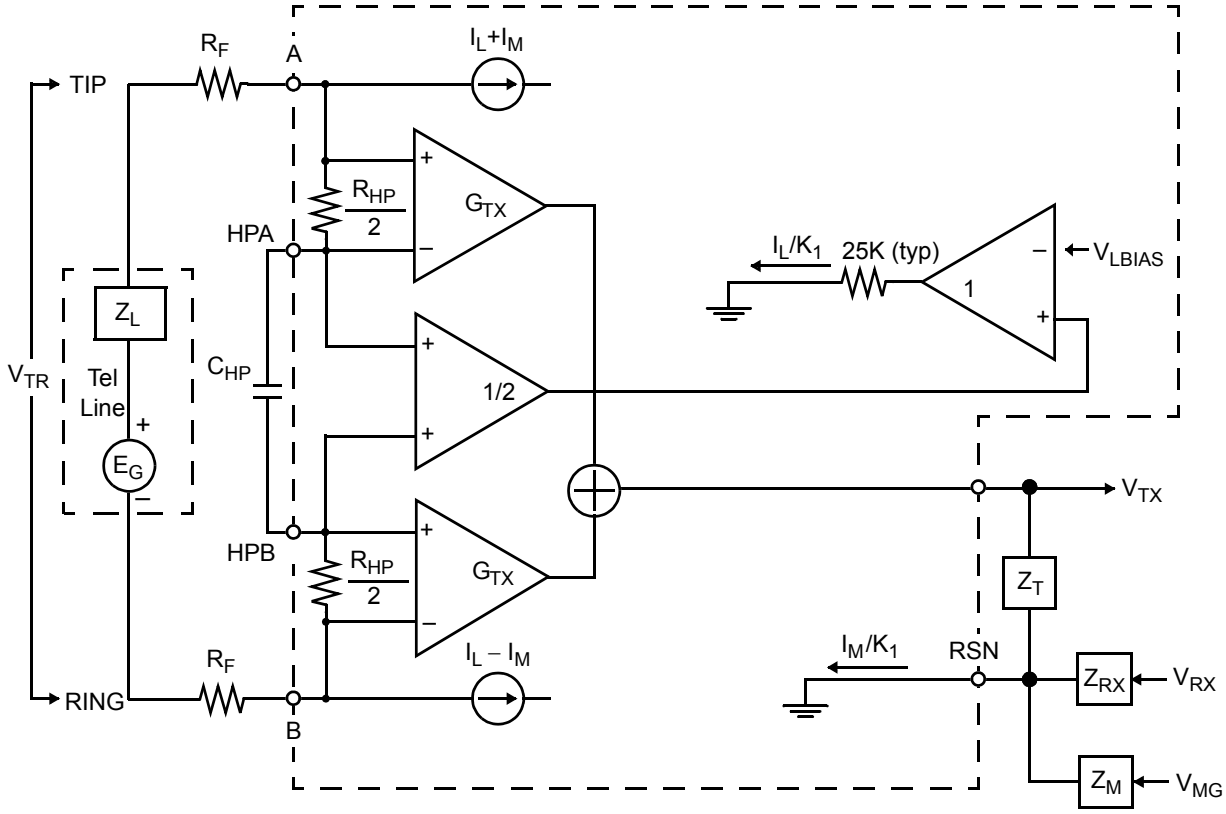
The four-wire output is found on the V_{TX} terminal, and the four-wire input terminal is V_{RX} (see Figure 2b). Both of these ports are referenced to analog ground (AGND).

Because the fuse resistors are outside the feedback loops, they influence the effective gains. These gains are as follows:

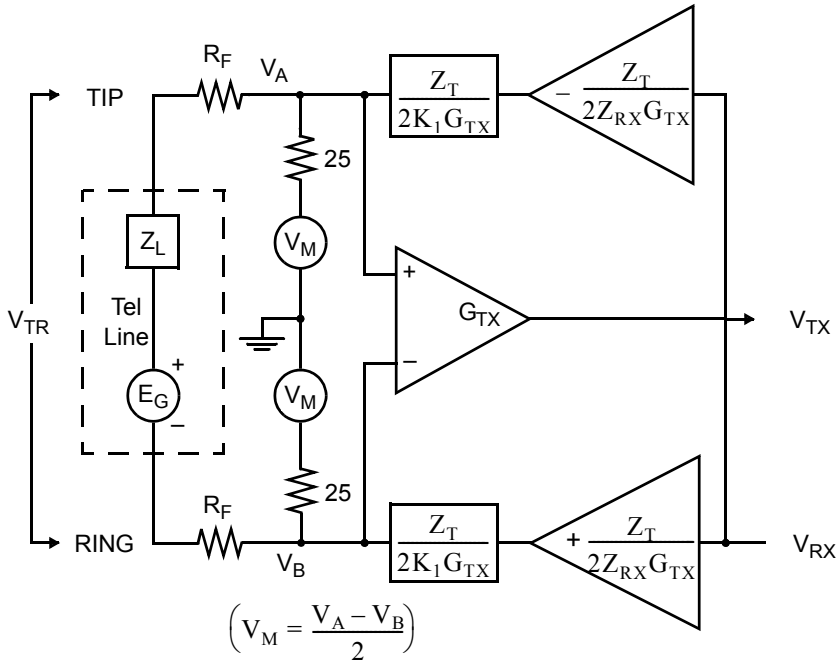
$$G_{42L} = \frac{V_A}{V_{RX}}[E_G = 0] = -\frac{Z_L}{Z_{RX}} \bullet \frac{K_1 Z_T}{Z_T + K_1 G_{TX}(Z_L + 2R_F)}$$

$$G_{24} = \frac{V_{TX}}{V_A}[V_{RX} = 0] = \frac{\frac{Z_T}{K_1}}{2R_F + \frac{Z_T}{K_1 G_{TX}}}$$

$$G_{44L} = \frac{V_{TX}}{V_{RX}}[E_G = 0] = -\frac{Z_T}{Z_{RX}} \frac{(Z_L + 2R_F)}{Z_L + 2R_F + \frac{Z_T}{K_1 G_{TX}}}$$



a. Detailed Model



b. Simplified Model (AC Only for Conceptual Purposes)

Figure 2. SLIC Transmission Model

The dynamic performances of K_1 (the current amplifier gain) and G_{TX} (the transmit voltage amplifier gain) are modeled by the following S-domain transfer functions:

$$K_1(S) = |K_1| \quad \frac{1}{1 + 1.15 \bullet 10^{-8} \bullet [R_S + Z_{AB}(S)] \bullet S}$$

$$G_{TX}(S) = \frac{|G_{TX}|}{1 + \frac{1}{R_{HP}\, C_{HP}\, S}} \bullet \frac{1}{1 + 4.5 \bullet 10^{-7} S}$$

Where: K_1 = Current amplifier DC gain
Z_{AB} = Load between the A and B pins
G_{TX} = Two- to four-wire transmit path midband gain
R_{HP} = Internal resistance, typically 424K
R_S = Current sensing resistance

These functions are useful for the prediction of system return loss and echo cancellation performance. The value of K_1 can be found in each device's data sheet referred to as the current gain. G_{TX} in dB is specified in each data sheet under two- to four-wire gain accuracy. C_{HP} sets the low frequency limit of the voice band response.

The transmission circuit also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage (V_{LBIAS}) which comes from the power feed controller. Longitudinally, the SLIC devices typically appear as 25 Ω resistors from A and B to V_{LBIAS}. The longitudinal feedback does not affect metallic signals.

In metering versions, metering signals are injected by adding an additional current into summing point RSN through an external impedance, Z_M.

Power Feed Controller

The power feed controller has three sections: (1) the battery feed circuit; (2) the polarity reversal circuit; and (3) the bias circuit. These are shown in Figure 3.

The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. The polarity reversal circuit provides the capability to reverse the loop current for pay telephone keypad disable and other applications. The bias circuit provides a reference voltage, which is offset from the subscriber line voltage. The reference voltage can control the switched mode regulator (switching regulator versions only, described later), which minimizes SLIC power consumption by providing the minimum supply voltage needed by the line drivers for proper operation. The reference voltage also can control the switching point for automatic battery switching SLIC devices.

V_{DCMET} is the DC component of the voltage between A and B. When C_{HP} is 0.33 μF, the low-pass filter formed by R_{HP} and C_{HP} attenuates frequencies above 1.2 Hz. The loop current is equal to K_1 times the current into the Receive Summing Node (RSN), which is equal to the voltage on RDC divided by R_{DC1} + R_{DC2}. The values of the programming resistors, R_{DC1} and R_{DC2}, should be kept somewhat equal in order to minimize the size of C_{DC}.

In constant current feed versions, the battery feed circuit produces a voltage at the RDC pin whose magnitude is equal to 2.5 V, and whose sign depends on the feed polarity desired (negative for normal polarity and positive for reverse polarity). The net result is a constant current feed with the feed current given by the following equation:

$$I_{FEED} = \frac{2.5K_1}{R_{DC1} + R_{DC2}}$$

For example, if K_1 is 1000 and a loop current of 40 mA is desired:

$$R_{DC1} + R_{DC2} = \frac{2.5 \bullet 1000}{40} = 62.5K$$

In this example, values of R_{DC1} and R_{DC2} of 31.25K could be used.

For resistance feed versions, the battery feed produces a voltage at the RDC pin whose magnitude is equal to (50 – $|V_{DCMET}|$)/20, and whose sign depends on the feed polarity desired (negative for normal polarity and positive for reverse polarity). The net result is an apparent open circuit voltage of 50 V and a feed resistance, R_{FEED}, equal to 20(R_{DC1} + R_{DC2})/K_1; thus, the feed resistance is programmable, but the apparent open circuit voltage is not. Including the fuse resistors R_F, the total feed resistance is then:

$$R_{FEED} = 2R_F + \frac{20(R_{DC1} + R_{DC2})}{K_1}$$

For example, if K_1 = 1000, and a feed resistance of 840 Ω is desired using 20 Ω fuse resistors:

$$R_{DC1} + R_{DC2} = \frac{1000\ (840 - 2 \bullet 20)}{20} = 40K$$

In this example, values of R_{DC1} and R_{DC2} of 20K could be used.

All SLIC devices have an anti-saturation guard that prevents the output amplifiers from saturating under long loop high resistance conditions, which maintains AC transmission by preventing clipping. Some of the SLIC devices implement multiple anti-saturation regions that may track the battery voltage or may operate at pre-determined fixed thresholds. Battery-independent anti-saturation noise performance is normally identical to that of normal loop feed, however, on some devices, anti-saturation that tracks the battery voltage may provide an additional path for battery-referenced noise entering the transmission path.

As an example, most switching regulator SLICs have two anti-saturation regions. In these SLICs, when the V_{AX} to V_{BX} voltage reaches a threshold of approximately 30 V (exact voltage depends on SLIC version), the Anti-sat 1 region of operation is entered. In this region, the feed synthesis loop gain is greatly increased, thereby reducing the output resistance to a much lower value. The output voltage then rises at a slower rate with increasing loop resistance, thereby keeping the amplifier out of saturation. All transmission specifications are met in the Anti-sat 1 region.

If the line voltage increases further to greater than approximately 5 to 15 V (exact voltage depends on SLIC version) below V_{BAT}, the SLIC goes into the Anti-sat 2 region where the loop gain is further increased and the output resistance decreased. In this region, the voltage rises very slowly, with increasing loop resistance, and the DC feed of the SLIC looks almost like a constant voltage source. The transmission specifications in the Anti-sat 2 region may be somewhat degraded.

Some of the SLIC devices implement a battery-dependent anti-sat scheme, where a pin (CAS pin) on the SLIC is provided to filter noise that may originate from the battery source. The size of the C_{CAS} capacitor connected to the CAS pin affects the amount of filtering, and therefore affects V_{BAT} PSRR performance. Load lines and equations describing all regions of operation are provided in each device data sheet.

To obtain polarity reversal, the input decoder and control circuit send a signal that reverses the sign of the voltage on the RDC pin. During reversal, sense resistors R_{HP} are shunted to reduce the time constant formed by R_{HP} and C_{HP}. This allows the polarity reversal time to be controlled only by C_{DC} and its parallel combination of R_{DC1} and R_{DC2}. A typical polarity transition time is 1.5 ms. In the previous example for a resistance feed version SLIC, R_{DC1} and R_{DC2} were computed to be 20K. The value of C_{DC} should then be 0.15 μF.

The longitudinal control loop operates by deriving an internal reference voltage V_{LBIAS}. This voltage is given by:

$$V_{LBIAS} = \frac{-(|VDCMET| + BIAS)}{2}$$

The additional BIAS is added to provide enough “headroom” for the amplifiers to always operate in the linear region. The value of BIAS varies depending on the SLIC type. Any longitudinal voltages appearing on the line are shunted to V_{LBIAS} via a 25 Ω resistance. Normal transmission performance is maintained provided the resulting current is less than the specified longitudinal current capability. The V_{REF} output is fed to the switching regulator (switching regulator SLICs only), which adjusts V_{REG}, the voltage supplying the line output amplifiers, until (for most devices) it is equal to twice V_{LBIAS}.

Power Management

The operation of the power-feed controller in most Zarlink SLIC devices results in the A pin maintaining a fairly constant voltage below Battery Ground, while the voltage on the B pin varies depending on the DC resistance of the loop. This means that as the loop length decreases, the voltage dropped across the B current amplifier and the corresponding power dissipation increases. Zarlink has implemented a number of techniques to take advantage of this characteristic to minimize the on-chip and in some cases, total system power dissipation.

Switching Regulator

The first technique is to implement a switching regulator function on-chip with a few external components (see Figure 4). The power-feed controller generates a reference voltage V_{REF}, which is the minimum voltage required to feed the output line amplifiers and is equal to twice V_{LBIAS}. The switching regulator adjusts V_{REG}, the operating voltage for the output amplifiers, to equal V_{REF}. The efficiency of the switching regulator (>80%) minimizes both the on-chip power dissipation and the system power dissipation. This is particularly important for short loops operating at high currents, which otherwise cause high power dissipation.

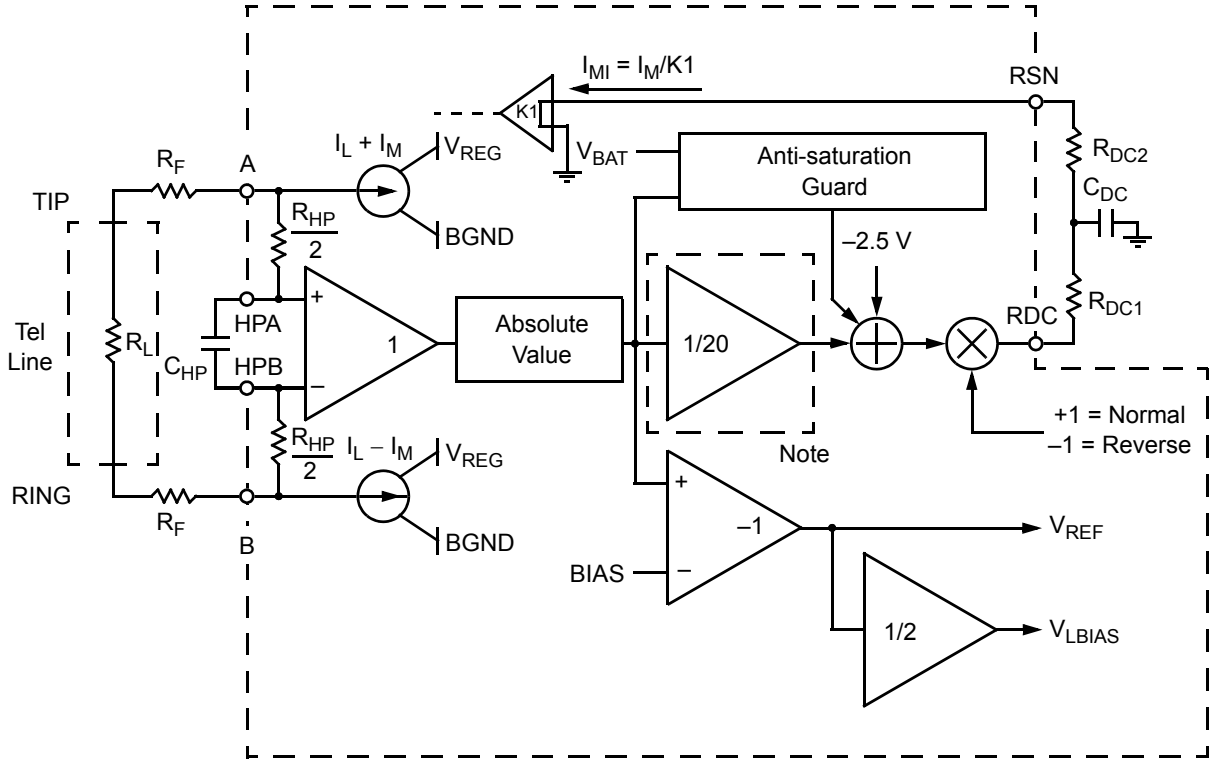
A 250 to 300 kHz clock is required at input CHCLK to operate the switching regulator. The switch control tells the switch to disconnect the L pin from V_{BAT} at the beginning of each CHCLK cycle, and connect it for a time that depends upon the difference between V_{REF} and V_{REG}. During this time, the current through the inductor decreases. A comparator senses when V_{REG} falls below V_{REF} and the inductor is again switched to V_{BAT}. The result is that the average value of V_{REG} is always held equal to the value of V_{REF}. The filter capacitor, C_{FIL}, between V_{REG} and BGND smooths out the ripple caused by the inductor switching action.

The regulator is a high-gain feedback circuit, and therefore requires the stabilization network formed by R_{CH}, C_{CH1}, and C_{CH2} between V_{REG} and CHS.

The design and layout of the external switching regulator circuitry is very important. Fast switching currents can occur in the catch diode, D_1, and in the V_{BAT} filter capacitor, C_{BAT}. These must be low inductance components with short leads. Capacitor C_{FIL} must have low effective series resistance at high frequencies. A stable, voltage-insensitive capacitor, such as a metallized polyester type, should be used.

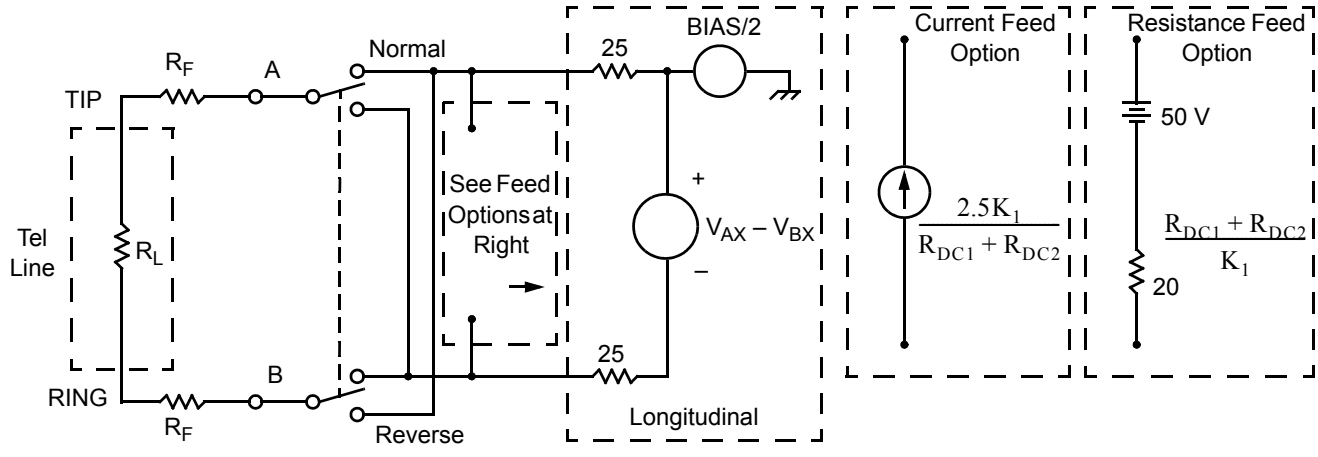
The connections from the diode to the L pin, from CBAT to the VBAT pin, and from the diode to C_{BAT} must all be short, low-inductance connections. The L pin is subject to very fast voltage transients as the switch turns on

and off, so all of the connections to this pin must be isolated from sensitive signals by means of traces connected to BGND. All of the external components in the regulator circuit must have voltage ratings in excess of the maximum battery voltage. In addition, the diode must have a reverse recovery time of less than 4 ns. All the switching-regulator SLIC devices in a system should be synchronized to a common clock to prevent intermodulation products and crosstalk in the voice band. For systems that include coding, the clock should be synchronous to the sampling frequency.



Note:
The 1/20 operational amplifier is only present in constant resistance feed versions of the SLIC.

a. Detailed Model



b. Simplified Model

Figure 3. SLIC Power Feed Controller

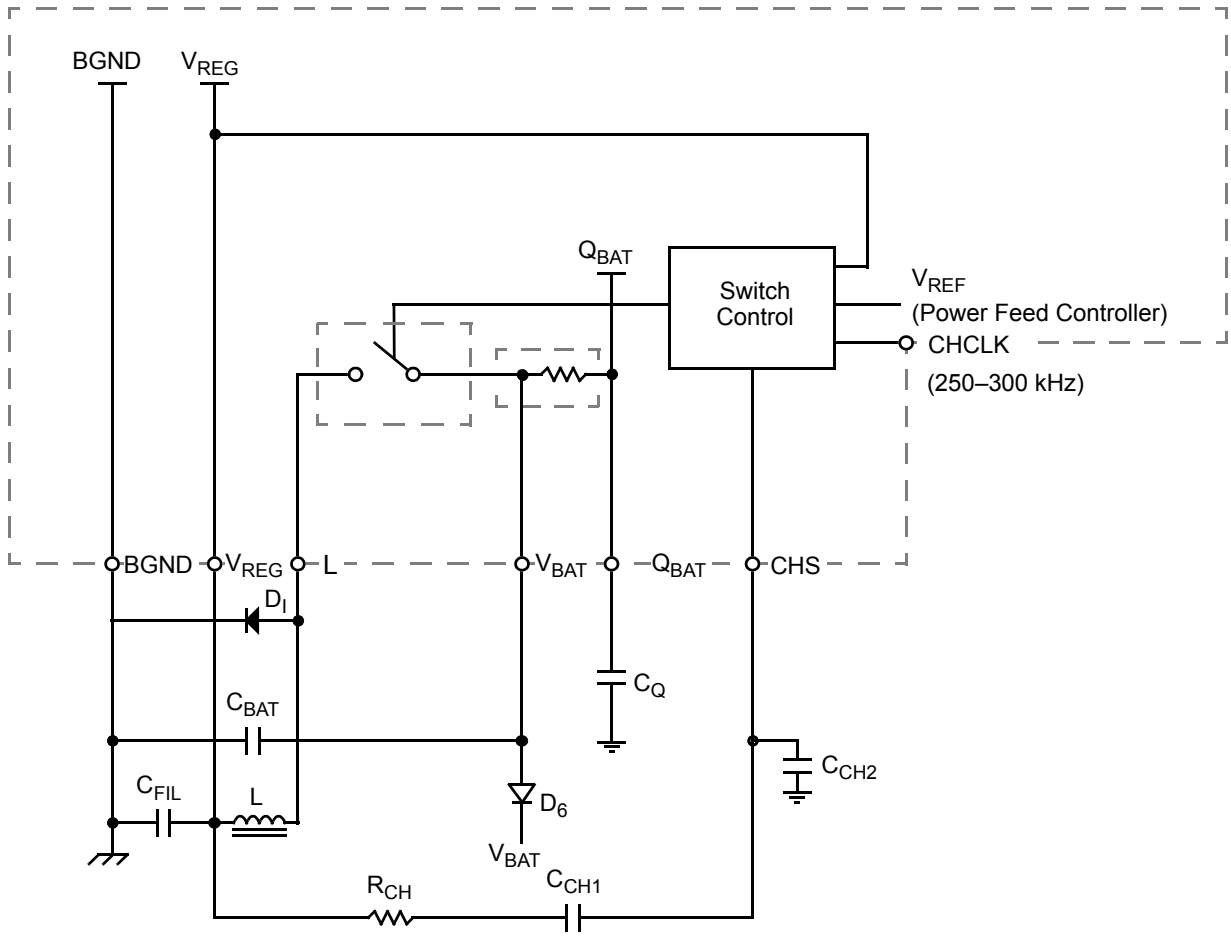
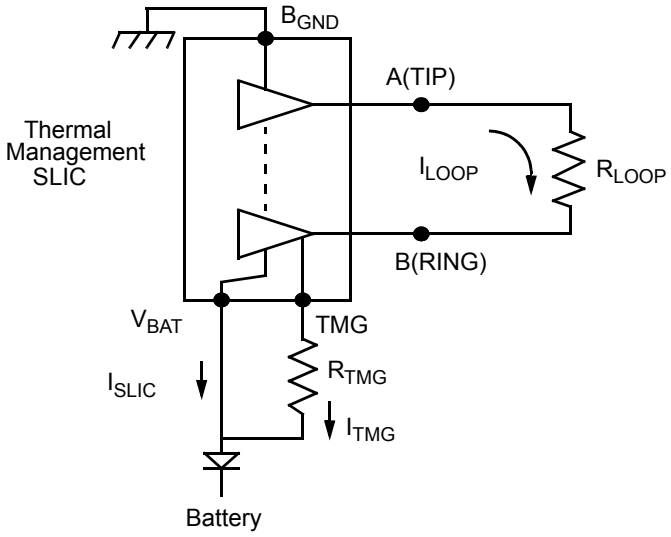


Figure 4. SLIC Switching Regulator

Thermal Management

This power management technique offloads thermal energy from the SLIC to an external resistor, R_{TMG}. The circuit configuration is shown in Figure 5. An external resistor is used to share some of the loop current with the B-leg current amplifier, especially on short lines. This limits the on-chip power dissipation and allows a low cost plastic package to be used while reducing external component count compared to the switching regulator solution. The R_{TMG} resistor is normally selected so that with the programmed loop current being fed into a short circuit loop from the nominal battery, all of the loop current is supplied by R_{TMG}. Equations to calculate this resistance and the resulting power dissipation in the SLIC and R_{TMG} are provided in the individual data sheets.

This feature operates in Normal and Reverse Polarity Feeding states for most SLIC devices. However, some SLIC devices only support thermal management in the Normal Polarity state. Refer to the specific data sheets.



Notes:

1. *A(TIP) lead remains at a relatively constant voltage (a few volts below ground) while B(RING) lead becomes more negative as loop resistance increases.*
2. *External resistor (R_{TMG}) shares loop current (I_{LOOP}) with SLIC.*
3. *Internal circuit and R_{TMG} resistor choice ensures maximum loop current is fed through R_{TMG} at shortest loop conditions.*
4. *The TMG connection is inside the SLIC's current sense loop, so as more current to the loop is provided through TMG, the current from the B lead amplifier is reduced, as is the SLIC's power dissipation.*
5. *The diagram shows scheme functionality. Fault control and other function switching are not shown.*

Figure 5. Simplified SLIC Thermal Management

Battery Switching

The third power management technique is battery switching operation. This technique allows both the device and system power dissipation to be minimized.

This solution provides for high on-hook voltage across the line, for on-hook recognition or to ensure operation with MTU's, while allowing low off-hook power dissipation by switching to a lower battery voltage.

Input Decoder and Control

The input decoder and control block provides a means for a microprocessor or SLAC™ IC to control such system functions as line activate, OHT, ringing, and polarity reversal.

The input decoder and control block has TTL-compatible inputs, which set the operating states of the SLIC. C3–C1 inputs are common to most versions and can select up to eight operating states. Other inputs are available for relay drivers as provided by certain SLICs.

E0 and E1 control the function of the $\overline{\text{DET}}$ output. 1 summarizes the available SLIC operating states for most devices.

Up to three detectors are implemented on-chip to support the necessary signaling functions. The status of these detectors is reported through a single output, $\overline{\text{DET}}$. Three control signals determine what information is provided at this output.

A signal from the state decoder selects between the ring trip comparator and loop detect/ground key (see 1). The E1 input selects between loop and ground key. Finally, the active high E0 input (when the SLIC is so equipped) enables the $\overline{\text{DET}}$ output, which is an open collector with an internal pull-up. The individual device data sheets should be used to determine which control lines are available with a given device/package option and to determine the polarity of E1.

Table 1. SLIC Decoding and State Description (most devices)

		Amplifier Output *		$\overline{\text{DET}}$ Output		
State	**Two-Wire State**	**A(TIP)**	**B(RING)**	**E1/$\overline{\text{E1}}$ See SLIC Data Sheet**		**Ring Relay Active**
0	Open Circuit	High-Z	High-Z	Ring trip	Ring trip	No
1	Ringing	High-Z	High-Z	Ring trip	Ring trip	Yes
2	Active	Near BGND	Near V_{BAT}	Loop detector	Ground key	No
3	OHT (On-Hook TX)	Near BGND	Near V_{BAT}	Loop detector	Ground key	No
4	Tip Open	High-Z	Near V_{BAT}	Loop detector	—	No
5	Standby	Near BGND	Near V_{BAT}	Loop detector	—	No
6	Active Polarity Reversal	Near V_{BAT}	Near BGND	Loop detector	Ground key	No
7	OHT Polarity Reversal	Near V_{BAT}	Near BGND	Loop detector	Ground key	No

Notes:

Open Circuit: *When the SLIC is in the Open Circuit state, both the A(TIP) and B(RING) power amplifiers are switched off and present high impedance to the line. The Open Circuit state has the lowest power dissipation. Loop detectors are inoperative in this state. This function is useful for allowing line-powered relays to collapse, denying power to out-of-service lines, as well as allowing clearing of line faults.*

Ringing*: When the SLIC is in the Ringing state, the ring relay driver (RINGOUT) is activated, and the ring-trip detector is readable at $\overline{\text{DET}}$. Also, the A(TIP) and B(RING) are both open circuits. While the SLIC is in the Ringing state, signal transmission is inhibited.*

Active*: In states where normal, Active operation is indicated, the standard battery convention applies; A(TIP) is near ground and sources current. B(RING) is near V_{BAT} and sinks current. During Active state operation, all signal transmission and loop supervision functions operate, and the off-hook detector or ground-key detector is gated to $\overline{\text{DET}}$.*

OHT*: The OHT (On-Hook Transmission) operating state is the SLIC's low-power mode in which the battery feed circuit limits the DC loop current to typically 0.5 (value depends on SLIC version) times the Active state short circuit current limit. In this state, the off-hook detector works normally, and all signal transmission functions operate normally. Previously, this OHT state was designated the Disable state in earlier Zarlink SLIC documentation.*

Tip Open*: When the SLIC is in the Tip Open state, the A(TIP) power amplifier is switched off so that it presents a high impedance to the line. This mode is provided to facilitate ground-start signaling.*

Standby: *The Standby state (on SLICs so equipped; see specific data sheets) is used for supervision purposes only. The A and B amplifiers are completely turned off (similar to the Open Circuit state) and DC feed through the loop is provided by an internal resistive feed network. Loop detect functions operate normally, but signal transmission is not enabled. This allows for monitoring off-hook transitions while maintaining lowest possible power consumption.*

Active Polarity Reversal*: When the SLIC is in Active Polarity Reversal state, the normal battery feed convention is reversed, with B(RING) approaching ground and sourcing current, while A(TIP) approaches battery and sinks current. While A(TIP) and B(RING) are in transition, the off-hook function is meaningless because the loop current must pass through zero.*

OHT Polarity Reversal*: This state is similar to the OHT state, except that the DC feed polarity is reversed.*

** With no DC loading, on-hook condition*

Off-Hook Detector

The first and most important loop monitoring function, provided on all SLIC devices, is off-hook detection. The block diagram of this detector is shown in Figure 6.

The two-wire interface produces a current equal in magnitude to the loop current divided by K_S, and sends it out on the RD pin. An external resistor and capacitor (R_D and C_D) connects the RD pin to the detector reference. The value of the voltage across resistor R_D is the current leaving the RD pin times the value of R_D. The off-hook detector outputs a logic Low when this voltage rises above a threshold voltage of typically 1.25 V.

The value of R_D required for a desired off-hook line current threshold is then (see SLIC data sheet for proper numerator value):

$$R_D = \frac{K_S \bullet V_T}{I_{THRESH}}$$

where K_S = 292 and V_T = 1.25 V

The value of C_d for a typical on-hook to off-hook time constant of 0.5 ms should satisfy the following relation:

$$R_D C_D = 0.5 \text{ ms}$$

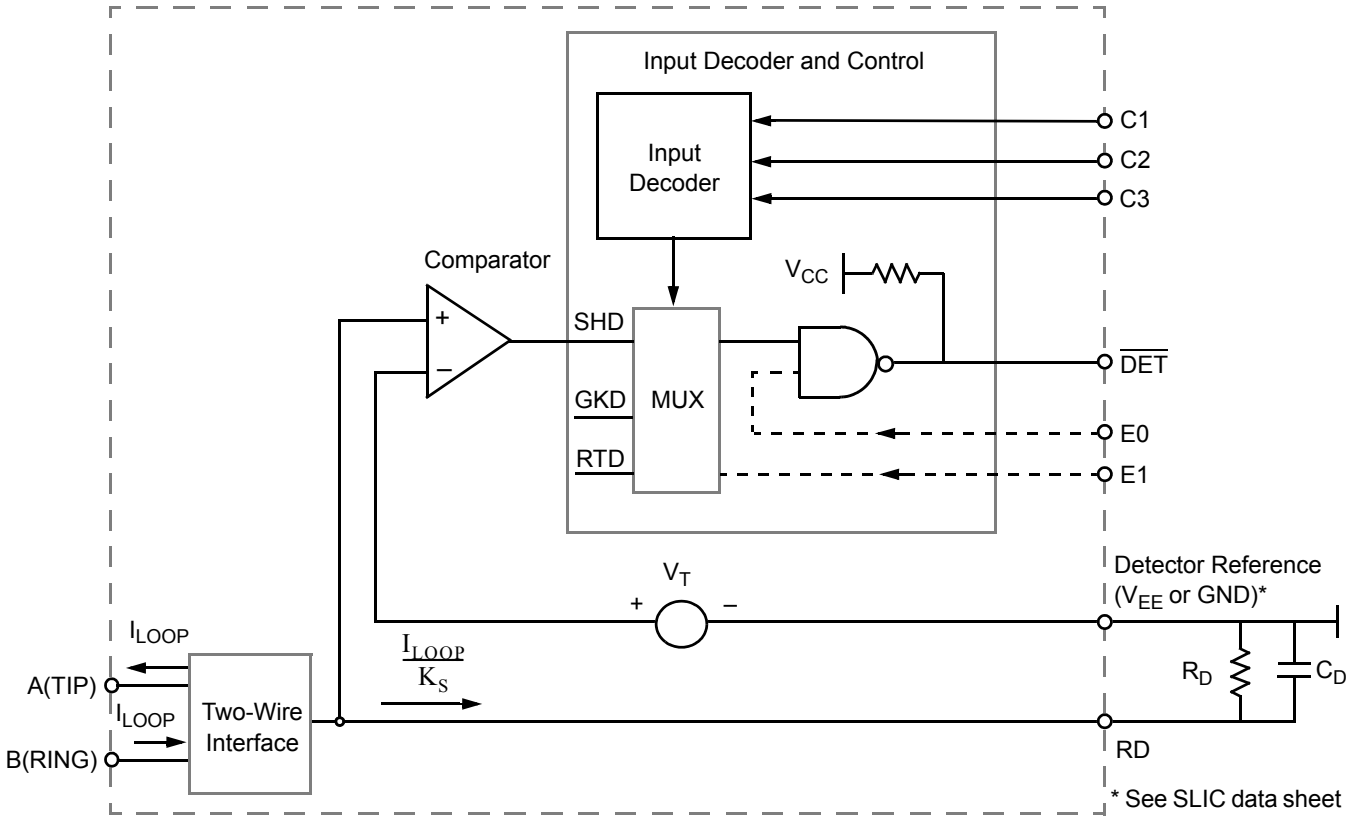


Figure 6. Signaling Off-Hook Detection

Ground-Key Detector

The Ground-Key Detector (see Figure 7) compares the longitudinal control current (I_{LI}) to an internally generated threshold current, I_{LT}. The current flowing in the earth loop is proportional to the longitudinal control current. When the current in the earth loop exceeds the threshold value, the ground-key signal forces the $\overline{DET}$ output Low when selected by E1.

On some SLIC versions, a ground key filter pin is provided. This allows attenuation of AC longitudinal currents and produces a more reliable detect output. The minimum GKFIL capacitor is 3.3 nF. It forms a low-pass transfer function with an on-chip 36 kΩ resistor. Larger capacitance values can be used to achieve the desired AC rejection.

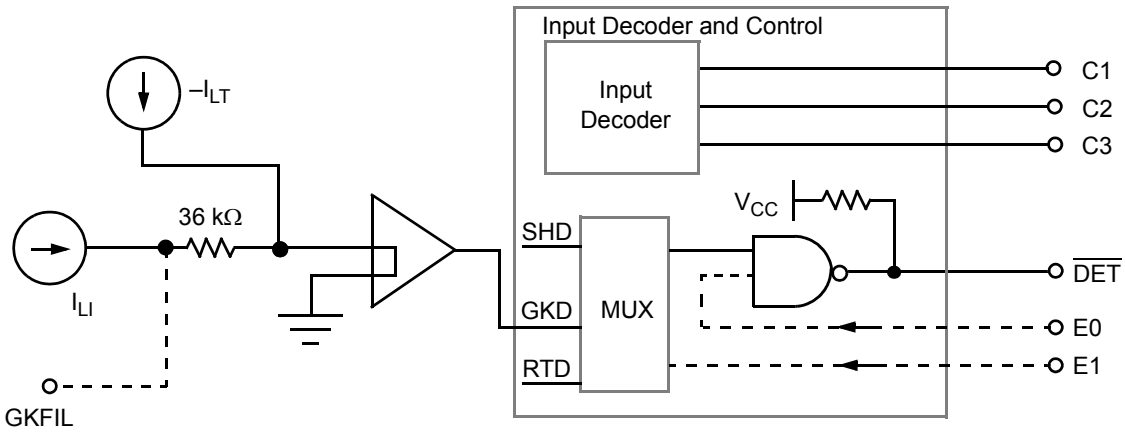


Figure 7. Ground-Key Detector

Ringing Circuit

A generalized ringing circuit is shown in Figure 8. In common applications, the circuit can be simplified as shown later. During ringing, the ring relay driver is activated and the A(TIP) and B(RING) leads are placed in the Open Circuit state. The ring feed source is connected by the ring relay to the line through ring feed resistors R_1 and R_2.

When an off-hook condition occurs, the bridging resistors R_{B1}, R_{B2}, R_3, and R_4, and filter capacitors C_{RT1} and C_{RT2} cause the voltage on DB to go positive with respect to DA and the detector ($\overline{DET}$) output goes Low.

If R_{LMAX} is the maximum line resistance that is to be detected as an off-hook, the bridging resistors should be chosen such that:

$$\frac{R_{B1}}{R_3} = \frac{R_{B2}}{R_4} = \frac{(R_{LMAX} + R_{FEED})}{(R_{LMAX} + R_1)}$$

Where: $R_{FEED} = R_1 + R_2$

The capacitors reduce the effective amplitude of the ringing signal by a factor of $1/|1+j2\pi f_r t|$.

Where: $t = \frac{R_3 R_{B1} C_{RT1}}{R_3 + R_{B1}} + \frac{R_4 R_{B2} C_{RT2}}{R_4 + R_{B2}}$

For f_r = 20 Hz ringing, C_{RT} should be chosen to give a value of t = 50 ms. This reduces the ringing by a factor of 6.4 and allow detection within two ringing cycles.

For balanced ringing, the ringing voltage splits between the ground and battery sides. The resistors should be balanced, (i.e., $R_1 = R_2$, $R_{B1} = R_{B2}$, and $R_3 = R_4$). A single capacitor of half the value between DA and DB can replace the capacitors C_{RT1} and C_{RT2}.

For unbalanced ringing on the ground side, use equal networks with $R_1 = R_2$, $R_{B1} = R_{B2}$, $R_3 = R_4$, and $C_{RT1} = C_{RT2}$.

For unbalanced ringing on the battery side, the following simplification can be made. The positive side of the ringing supply is grounded and R_1 is replaced by a short circuit. In this case, the R_4, R_{B2}, and C_{RT2} network can be combined with other channels into a ringer threshold because the voltage on the DA pin is independent of line conditions.

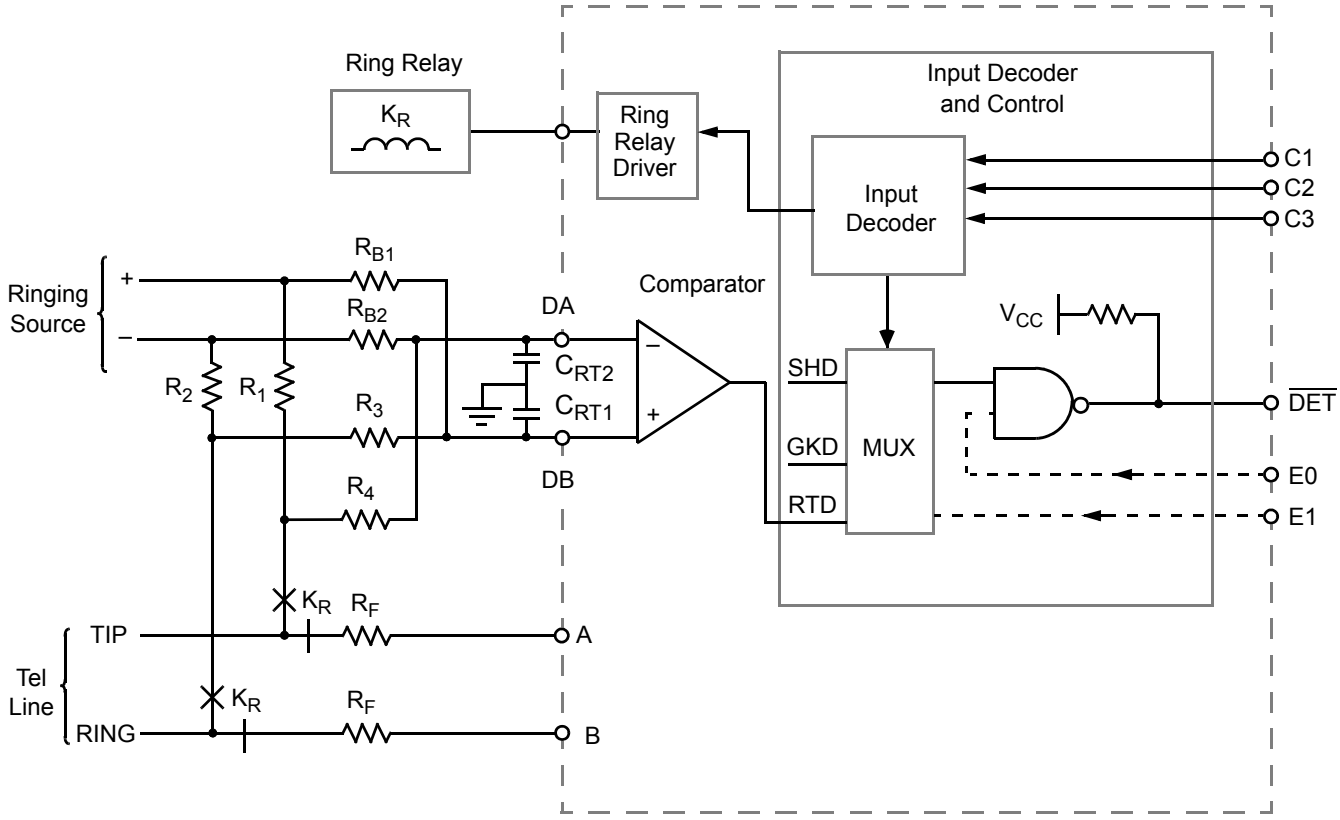


Figure 8. Ringing Circuit

Ringing SLICs

ZarInk offers some SLICs, such as the Le79R79, which integrate ringing onto the chip. These devices do not require an external ringing source and do not require a ringing relay to switch the ringing signal on or off. In these devices, the same amplifiers that drive the tip and ring leads are used to generate the ringing voltage right on the SLIC device itself.

Ring Relay Driver

A ring relay driver is provided on all versions (except ringing SLIC devices) and is active only in the Ringing state. The relay driver configuration varies between parts.

For some devices, the driver is an internal transistor with the collector sourced to BGND and the emitter as the driver output. This allows relays connected to a negative supply, typically V_{BAT}, to be operated. A diode to V_{BAT} is integrated into the design.

Other versions have the collector of an internal NPN transistor (emitter grounded) brought out to a separate pin. This allows +5 V relays to be used, and in this case, an integral 7 V Zener between the transistor collector and ground suppresses voltages generated when the relay is released. Some of these devices may not have the internal Zener snubber allowing up to 12 V relays to be used, and may require an external catch diode. Consult individual data sheets for exact configurations.

Test Relay Driver

Additional relay drivers are provided on some SLIC devices. Different configurations are available, depending on the specific SLIC type, allowing for direct operation of test relays, or to connect optional test loads.

Application Examples

The Zarlink SLIC Family offers a high degree of versatility for analog loop-line circuit applications including Central Office, DLC, FITL, and PBX systems. In this section, typical single-channel and multiple-channel applications are described.

Figure 9 shows a detailed schematic of a basic single-line circuit using one SLIC and one-half of an Am79C02 DSLAC™ device.

In the receive path, the DSLAC device processes digital PCM voice data into analog signals and inputs them to the SLIC RSN pin through resistor R_{RX}. In the transmit path, the analog output at the SLIC VTX pin is processed by the DSLAC device and output in serial-digital format to the PCM interface. R_{RX} sets the receive gain and R_T is used to synthesize the AC two-wire output impedance. Both R_T and R_{RX} can be complex to achieve optimized parameters over the voice band.

In the control path, when the line goes off-hook, the SLIC pulls its collector $\overline{DET}$ output down and enables the DSLAC device serial control data I/O pins, DIN and DOUT (see Figure 10). The microprocessor also recognizes the off-hook and typically sends a response, such as an Active state or ring relay release command, back to the SLIC, via the DSLAC device DIN pin and the C3–C1 data bus.

The C4 line also is addressed in the same manner to enable or disable the test relay driver. The E0 and E1 pins are addressed directly by the microprocessor as shown.

Figure 11 shows a detailed schematic of a basic single-line circuit using one Am79M5XX series SLIC and one half of an Am79C02 DSLAC device. The dashed connection lines in the schematic show the wiring of the various relay, $\overline{DET}$ enabling, and ground-key options available. The TESTOUT, C4, E0, or E1 pins may or may not be present, depending on the version used.

The Metering Filter block represents an external 12 or 16 kHz low-pass or notch filter to reduce the metering level in the transmit path before it can overload the SLAC IC input. A suggested metering filter circuit, shown in Figure 12, is a notch filter centered at 12 or 16 kHz. This filter has enough attenuation at the metering frequency and does not require an additional cancellation circuit.

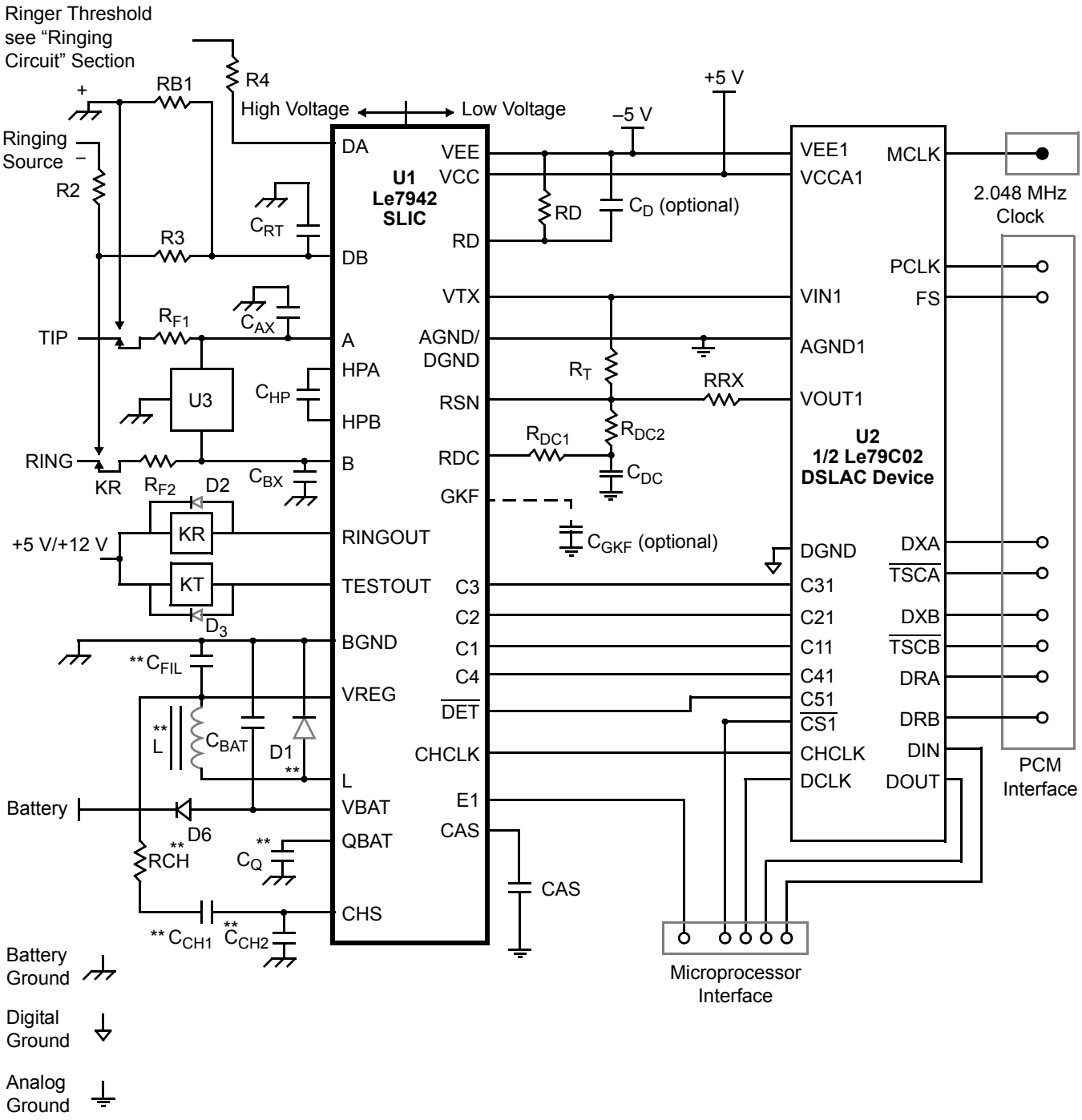
It is a common practice to plug linecards into a powered backplane. To assure reliable operation of the linecard, certain precautions must be taken. Monolithic silicon circuits are built with P and N doped regions on a substrate, and rely upon the proper voltages to be applied to these regions to provide isolation and bias of circuit elements. Typically, the substrate is attached to the most negative voltage, which is V_{BAT} at about –48 V. When voltages are applied in the improper order or with unlimited current, large currents may flow through the substrate to devices and conductors, causing damage. This may cause an instant failure of the part, or degradation over a few seconds or even weeks. To assure that no damage happens to the SLIC, the following recommendations should be followed:

- **Ensure that ground is always connected before any of the other power supply voltages.** Zarlink SLICs are not sensitive to the order the other supply voltages are applied, as long as ground is connected first. A common practice is to use longer edge fingers on card edge connectors or longer contacts in plug connectors for connections that must be made first. If this method is not practical, a means to switch –5 V (V_{EE}) and –48 V (V_{BAT}) with the application of +5 V and ground eliminates the concern of negative supplies being applied first. This also prevents negative voltages from being applied to pins C3–C1, which can trigger internal trimming

SCR's. It is possible that +5 V will be connected before ground, but typically this is not an issue.

- **Provide current limiting to the –5 V (V_{EE}) supply at the pc board level.** If –5 V is connected before V_{BAT}, there is a conduction path through the substrate to charge the V_{BAT} capacitor, which can cause internal damage. A 2 Ω resistor in series with the –5 V (V_{EE}) supply and the V_{EE} connections of the SLICs should limit current to a safe level.
- **Add a Zener diode between the SLIC V_{EE} supply and ground.** This prevents the V_{EE} bus from pulling outside safe limits during transient application of power through capacitive conduction paths. This Zener conducts in the positive direction to prevent V_{EE} from going positive, and in the reverse (Zener) direction to keep the voltage from becoming too negative. The diode should be placed on the SLIC side of the 2 Ω resistor recommended above.
- **Provide current limiting to the –48 V (V_{BAT}) supply at the pc board level.** On switching regulator SLICs, the V_{BAT} voltage rate of rise must be limited as stated on the SLIC data sheet to prohibit excessive internal current from charging the Q_{BAT} capacitor, which could damage the part. On nonswitching regulator SLICs, the current limiting prevents transient voltages and currents from causing potential problems. A 1 Ω resistor in series with the V_{BAT} supply should provide the necessary current limiting. A capacitor in the SLIC side of the resistor forms a time constant, which helps limit the rise time.
- **Ensure that all SLIC grounds (BGND, AGND, and DGND) have a voltage difference between them that is less than the maximum specified on the data sheet.** If the grounds are connected together on the PC board, this is not a problem, but if they connect to separate pins on the card edge connector, it is possible for one ground connection to occur before the others, causing maximum limits to be exceeded. Maximum BGND with respect to AGND/DGND is typically ±100 mV to +1 V/–3 V.
- **For further details on this subject, please request a copy of the "Telephone Linecard Powering Considerations with Monolithic SLIC Devices" application note.**

Contact any local Zarlink sales office for the availability of additional, more detailed application notes.



*** The parts marked by a double asterisk (**) are not needed for 24 V battery operation without using switching regulator. For use without the switcher, delete the noted parts and connect together: VBAT, CHS, QBAT, L, and VREG pins.*

Figure 9. Single Channel of a Dual Channel Subscriber Line Circuit with Switcher Components

Table 2. Parts List — Single Channel Subscriber Line System (See Figure 9 for Circuit)

U1	Le7942 SLIC***
U2	Le79C02 DSLAC device***
K_R, K_T	Relay, 2C contacts, 1500 V rating
L	Inductor, 1 mH, 5%**
D1	Diode, 100 V, 100 mA, 4 ns**
U3	Dual transient suppressor
D2, D3, D6	Diode 100 V, 100 mA, 10 ns
R_{F1}, R_{F2}	Resistor, fuse, 20 Ω to 50 Ω
R2	Resistor, 800 Ω, 3%, 3 W (Ring feed resistor)*
R_{B1}	Resistor, 1 MΩ, 1%, 1/4 W
R3	Resistor, 825K, 1%, 1/4 W
R4	Resistor, 452K, 1%, 1/4 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W**
R_D	Resistor, 35.4K, 1%, 1/4 W (sets off-hook threshold)*
R_T	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX}	Resistor, 100K, 1%, 1/4 W (sets two-wire impedance)*
R_{DC1}, R_{DC2}	Resistor, 7.14K, 1%, 1/4 W (sets loop current)*
R_{TMG}	Resistor 1700 Ω, 5%, 2 W (Am7943)
C_{RT1}	Capacitor, 0.1 μF, 20%, 100 V
C_{DC}	Capacitor 0.47 μF, 20%, 10 V
C_{HP}	Capacitor, 0.33 μF, 20%, 100 V
C_{CAS}	Capacitor, 0.15 μF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2200 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.47 μF, 10%, 100 V, metallized polyester**
C_{BAT}	Capacitor, 0.47 μF, 20%, 100 V
C_Q	Capacitor, 0.33 μF, 20%, 100 V**
C_{CH1}	Capacitor, 0.015 μF, 10%, 50 V, X7R ceramic**
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic**
C_D	Capacitor, 0.01 μF, 20%, 10 V (sets off-hook filtering)*
C_{GKF}	Capacitor, 3300 pF, 10%, X7R ceramic

Notes:

* *The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.*

** *The parts marked by a double asterisk (**) are not needed for 24 V battery operation without a switcher.*

*** *Obsolete; no longer in production. Please contact your Zarlink sales representative for another solution.*

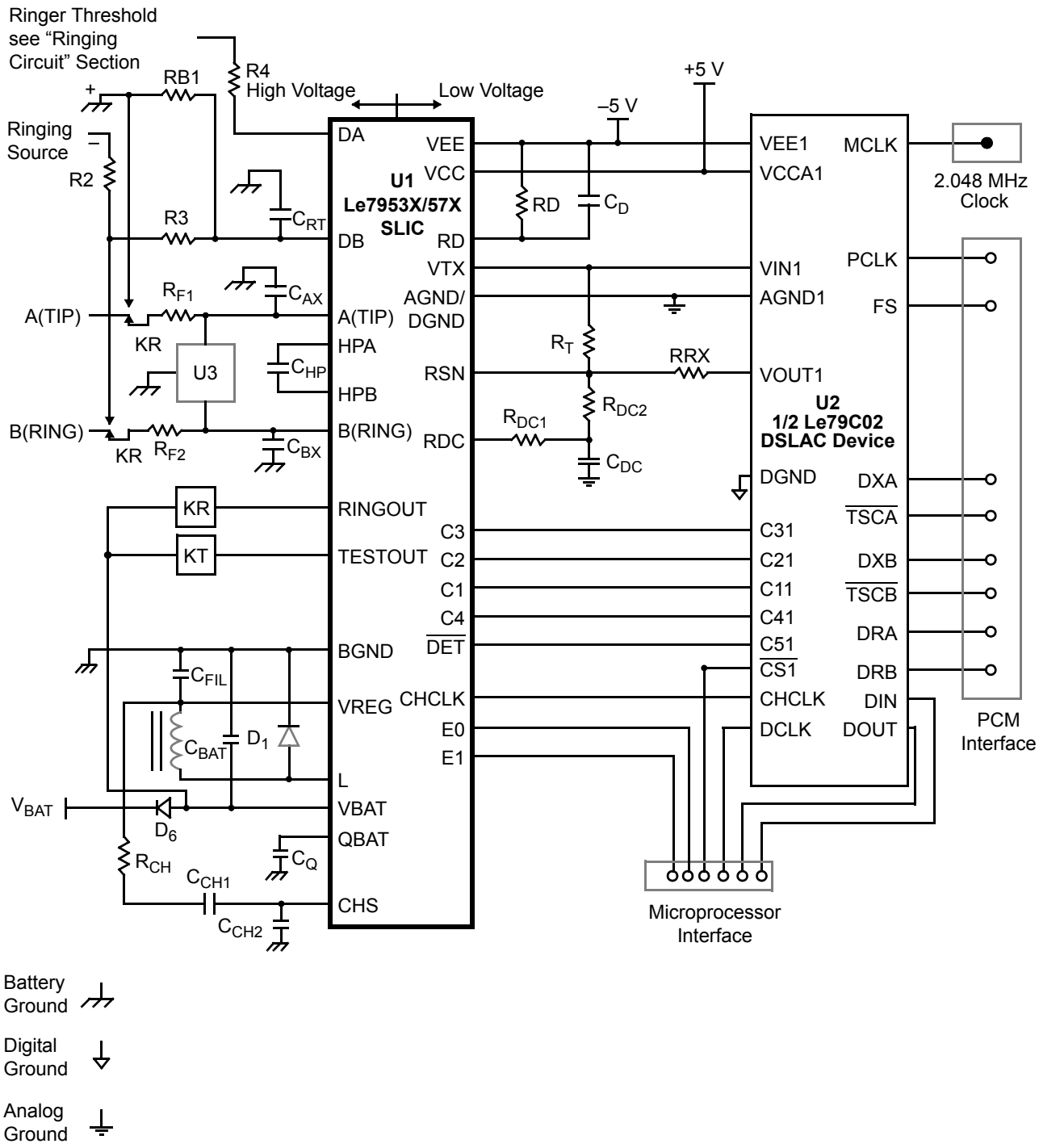


Figure 10. Single Channel of a Dual Channel Subscriber Line Circuit

Table 3. Parts List — 1/2 of a Dual Channel Subscriber Line System (see Figure 10 for Circuit)

U1	Le7953X** or Le7957X SLIC**
U2	Le79C02 DSLAC device**
K_R, K_T	Relay, 2C contacts, 1500 V rating
L	Inductor, 1 mH, 5%
D_1	Diode, 100 V, 100 mA, 4ns
U_3	Dual transient suppressor
D_6	Diode 100 V, 100 mA, 10 ns
R_{F1}, R_{F2}	Resistor, fuse, 50 Ω*
R_2	Resistor, 800 Ω, 3%, 3 W (Ring Feed Resistor)*
RB_1	Resistor, 1 meg, 1%, 1/4 W
R_3	Resistor, 8.25K, 1%, 1/4 W
R_4	Resistor, 452K, 1%, 1/4 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W
R_D	Resistor, 51.1K, 1%, 1/4 W (sets off-hook threshold)*
R_{DC1}, R_{DC2} (Le7953X)	Resistor, 31.25K, 1%, 1/4 W*
R_{DC1}, R_{DC2} (Le7957X)	Resistor, 20K, 1%, 1/4 W*
R_T	Resistor, 560K, 1%, 1/4 W*
R_{RX}	Resistor, 560K, 1%, 1/4 W (sets receive gain)*
C_{RT}	Capacitor, 0.047 μF, 20%, 100 V
C_{DC}	Capacitor, 0.15 μF, 10%, 10 V
C_{HP}	Capacitor, 0.33 μF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2200 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.15 μF, 10%, 100 V metallized polyester
C_{BAT}	Capacitor, 0.47 μF, 20%, 100 V
C_Q	Capacitor, 0.33 μF, 20%, 100 V
C_{CH1}	Capacitor, 0.015 μF, 10%, 50 V, X7R ceramic
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic
C_D	Capacitor, 0.01 μF, 20%, 10 V (sets off-hook filtering)*

Note:

** The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.*

*** Obsolete; no longer in production. Please contact your Zarlink sales representative for another solution.*

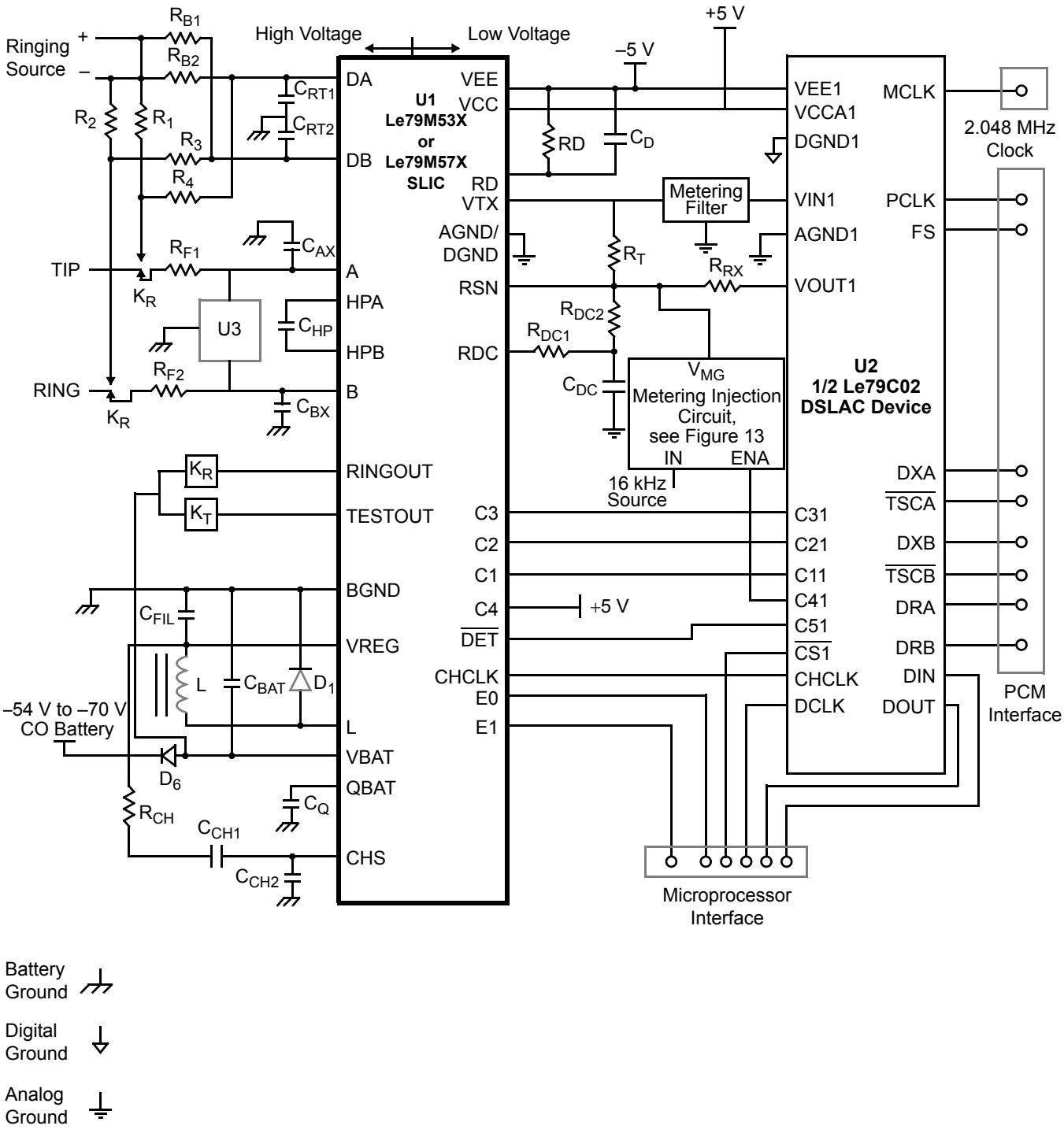


Figure 11. Single Channel of a Dual Channel Metering Subscriber Line Circuit

Table 4. Parts List — 1/2 of a Dual Channel Metering Subscriber Line System (See Figure 11 for Circuit)

U1	Le79MXXX SLIC**
U2	Le79C02 DSLAC Device**
K_R, K_T	Relay, 60 V coil, 2C contacts, 1500 V rating
L	Inductor, 1 mH, 5%
D_1	Diode, 100 V, 100 mA, 4 ns
U_3	Dual transient suppressor
D_6	Diode 100 V, 100 mA, 10 ns
R_{F1}, R_{F2}	Resistor, fuse, 20 Ω
R_1, R_2	Resistor, 400 Ω, 3%, 3 W (Ring Feed resistors)*
RB_1, RB_2	Resistor, 249K, 1%, 1/4 W
R_3, R_4	Resistor, 205K, 1%, 1/2 W
R_{CH}	Resistor, 1.3K, 1%, 1/4 W
R_D	Resistor, 51.1K, 1%, 1/4 W (sets off-hook threshold)*
R_T	Resistor, 286K, 1%, 1/4 W (sets two-wire impedance)*
R_{RX}	Resistor, 560K, 1%, 1/4 W (sets receive gain)*
R_{DC1}, R_{DC2} (Le79M53X)	Resistor, 31.25K, 1%, 1/4 W (sets 40 mA loop current)*
R_{DC1}, R_{DC2} (Le79M57X)	Resistor, 20K, 1%, 1/4 W (sets 800 Ω resistive feed)*
C_{RT1}, C_{RT2}	Capacitor, 0.43 μF, 20%, 100 V
C_{DC}	Capacitor 0.1 μF, 20%, 10 V
C_{HP}	Capacitor, 0.33 μF, 20%, 100 V
C_{AX}, C_{BX}	Capacitor, 2.2 pF, 20%, 100 V
C_{FIL}	Capacitor, 0.47 μF, 10%, 100 V, metallized polyester
C_{BAT}	Capacitor, 0.47 μF, 20%, 100 V
C_Q	Capacitor, 0.33 μF, 20%, 100 V
C_{CH1}	Capacitor, 0.015 μF, 10%, 50 V, X7R ceramic
C_{CH2}	Capacitor, 560 pF, 10%, 100 V, X7R ceramic
C_D	Capacitor, 0.01 μF, 20%, 10 V (sets off-hook filtering)*

Note:

** The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.*

*** Obsolete; no longer in production. Please contact your Zarlink sales representative for another solution.*

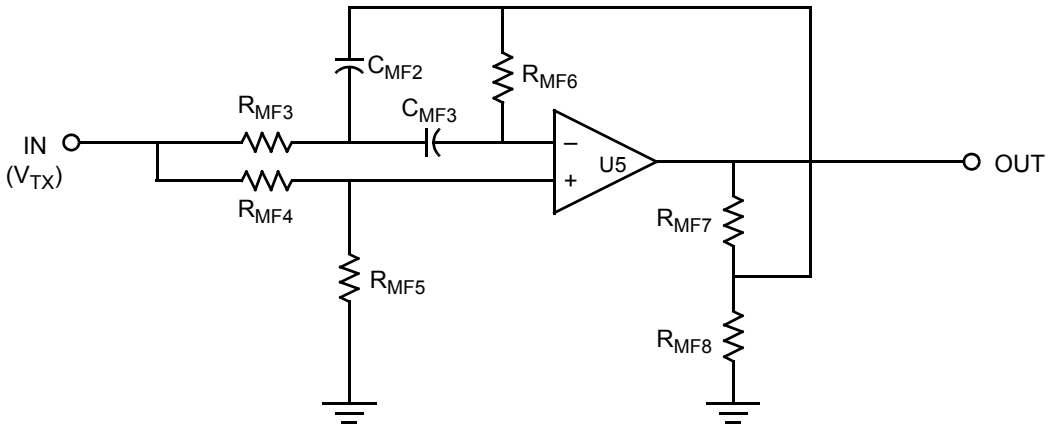


Figure 12. 16 kHz Metering Notch Filter

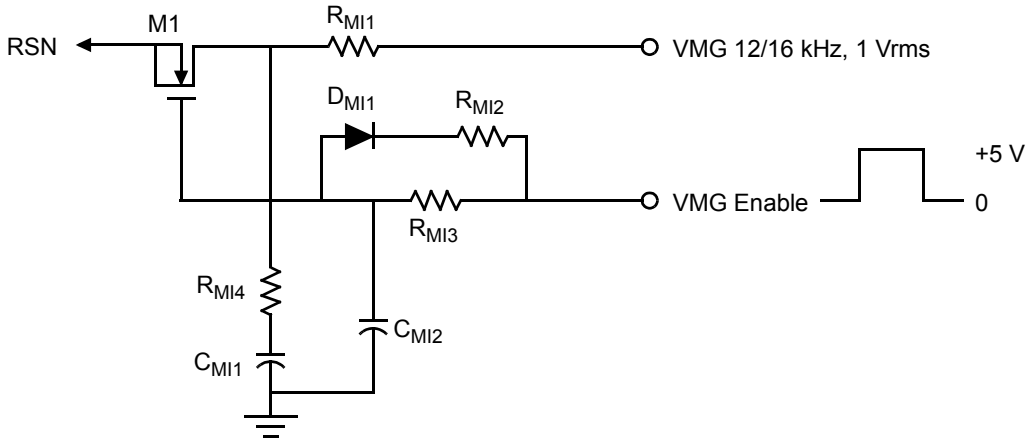


Figure 13. Metering Injection Circuit

Table 5. Parts List for Le79M53X/Le79M57X Metering Notch Filter (See Figure 12 for Circuit)

	FNOTCH		
	12 kHz	16 kHz	
R_{MF3} Resistor	5.07K	4.0K	1%, 1/4 W*
R_{MF4} Resistor	5.39K	5.58K	1%, 1/4 W*
R_{MF5} Resistor	22.0K	22.0K	1%, 1/4 W*
R_{MF6} Resistor	37.9K	27.9K	1%, 1/4 W*
R_{MF7} Resistor	2.17K	2.25K	1%, 1/4 W*
R_{MF8} Resistor	8.84K	8.84K	1%, 1/4 W*
C_{MF2} Capacitor	1.0 nF	1.0 nF	5%, 10 V*
C_{MF3} Capacitor	1.0 nF	1.0 nF	5%, 10 V*

Table 6. Parts List for Metering Injection Circuit (See Figure 13 for Circuit)

R_{MI1} (5.1 V metering)	Resistor, 3.62K, 1%, 1/4 W*
R_{MI1} (2.2 V metering)	Resistor, 8.33K, 1%, 1/4 W*
R_{MI2}	Resistor, 200K, 1%, 1/4 W*
R_{MI3}	Resistor, 300K, 1%, 1/4 W*
R_{MI4}	Resistor, 300 Ω, 1%, 1/4 W*
C_{MI1}	Capacitor, 220 nF, 10%, 10 V*
C_{MI2} (16 kHz metering)	Capacitor, 39 nF, 10%, 10 V*
C_{MI2} (12 kHZ metering)	Capacitor, 51 nF, 10%, 10 V*
M1	N Channel MOS transistor, 2N7000, 2N7002 or equivalent
D_{MI1}	Diode, 100 V, 100 mA, 10 ns

Note:
The parts marked by an asterisk (*) are user programmable. The values shown can be altered to suit the application.

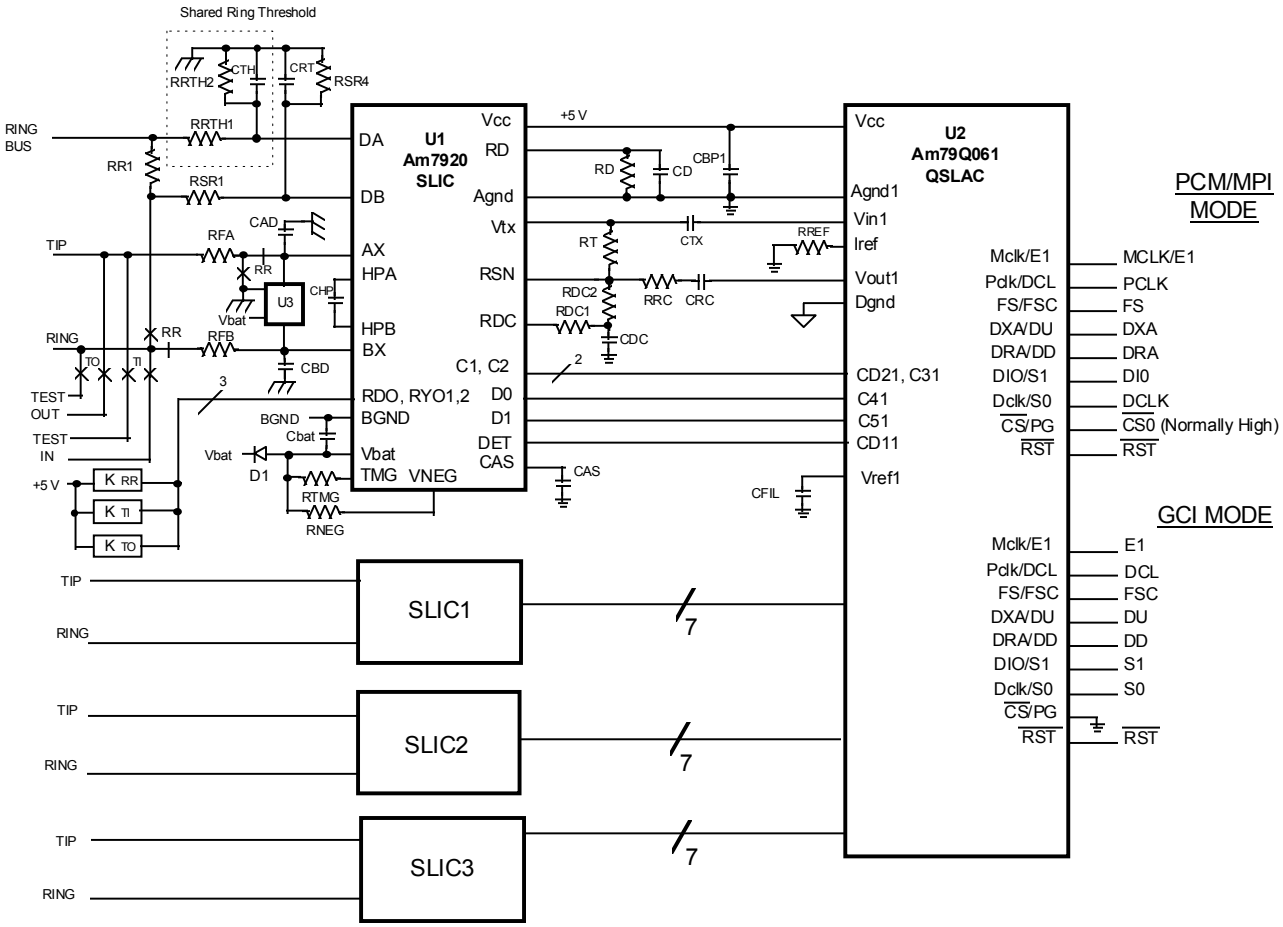


Figure 14. Le7920 SLIC/QSLAC Device Application Circuit

Table 7. Parts List — 1/4 of a Four Channel Subscriber Line System (see Figure 14 for Circuit)

U1	Le7920
U2	Le79Q061 QSLAC™ device**
K_{RR}, K_{TI}, K_{TO}	Relay, 2C contacts, 1500 V rating
D_1	Diode, 100 V, 100 mA
U_3	Teccor PO640SA transient suppressor
R_{F1}, R_{F2}	Resistor, fuse, 50 Ω*
RR1	Resistor, 400 Ω, 3%, 3 W (Ring Feed Resistor)*
RSR1, RRTH1	Resistor, 1 meg, 1%, 1/4 W
RSR4	Resistor, 5.5K, 1%, 1/4 W (shared between all 4 SLICs; use 2.2M if not shared)
RRTH2	Resistor, 400K, 1%, 1/4 W (shared between all 4 SLICs; use 1.6M if not shared)
RTMG	Resistor, 1K, 5%, 1/2 W
R_D	Resistor, 37.4K, 1%, 1/4 W (sets off-hook threshold)*
R_{DC1}, R_{DC2}	Resistor, 16K, 1%, 1/4 W*
R_T	Resistor, 200K, 1%, 1/4 W*
RRC	Resistor, 124K, 1%, 1/4 W (sets receive gain)*
CRT, CTH	Capacitor, 0.068 μF, 20%, 50 V
C_{DC}	Capacitor, 0.27 μF, 10%, 50 V
C_{HP}	Capacitor, 0.27 μF, 20%, 100 V
CAD, CBD	Capacitor, 2200 pF, 20%, 100 V
CAS	Capacitor, 0.1 μF, 10%, 100 V
C_{BAT}	Capacitor, 0.01 μF, 20%, 100 V
CFIL, CRC, CTX, CBP1	Capacitor, 0.1 μF, 10%, 50 V
C_D	Capacitor, 0.01 μF, 20%, 10 V (sets off-hook filtering)*

Note:

** The parts marked by an asterisk (*) are user-programmable. The values shown can be altered to suit the application.*

*** Replaced by the Le58QL061 QLSLAC™ device.*

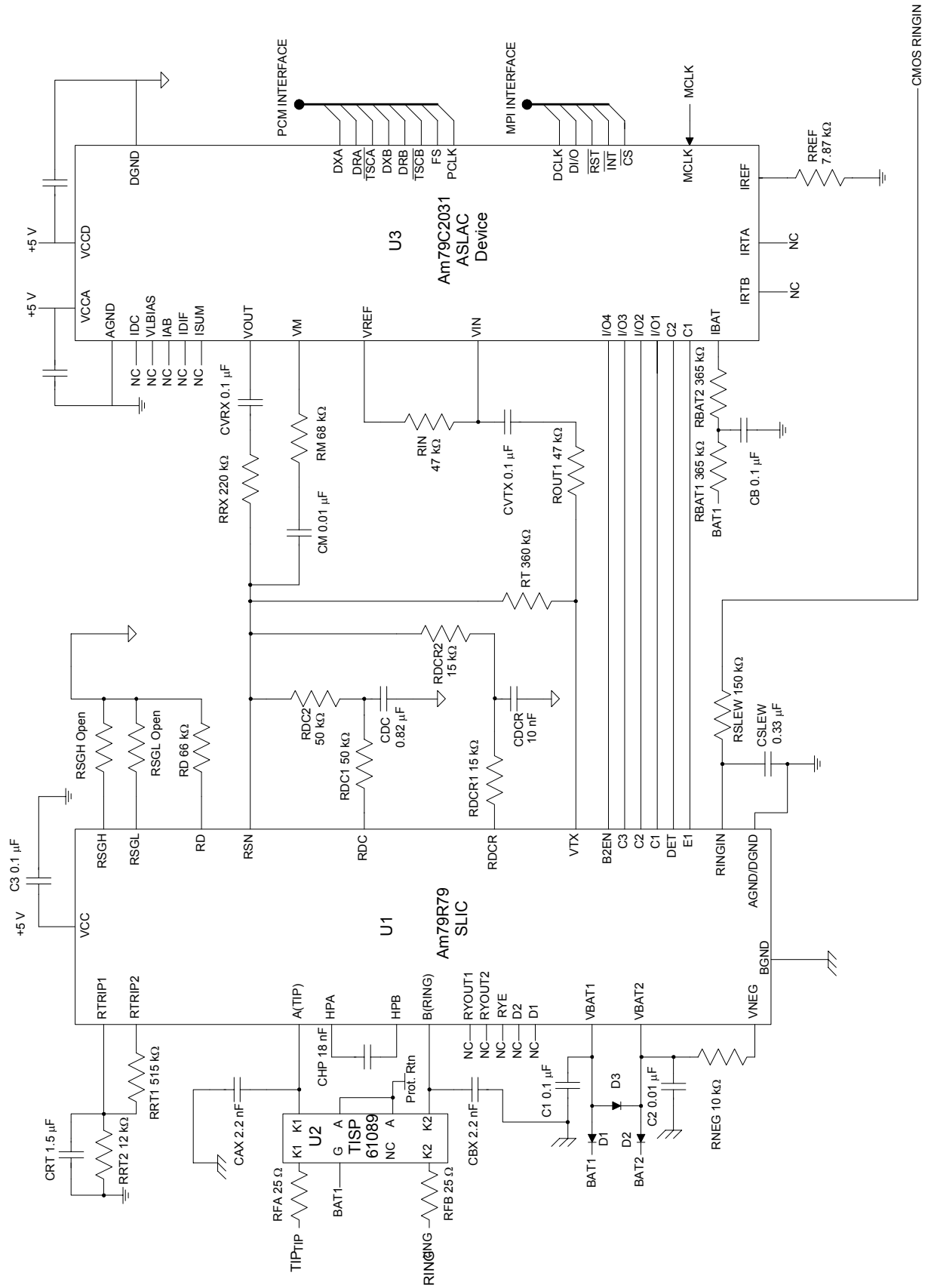


Figure 15. Single Channel Ringing Subscriber Line Circuit

Table 8. Parts List – Single Channel Ringing Subscriber Line Circuit

D1	1N400X	
D2	1N400X	
D3	1N400X	
C1	0.1 μF, 20%, 100 V	Vbat1 dependent
C2	0.01 μF, 20%, 100 V	Vbat1 dependent
C3	0.1 μF, 20%, 10 V	Supply decoupling
C4	0.1 μF, 20%, 10 V	Supply decoupling
C5	0.1 μF, 20%, 10 V	Supply decoupling
CAX	2.2 nF, 20%, 100 V	EMI suppression
CBX	2.2 nF, 20%, 100 V	EMI suppression
CRT	1.5 μF, 10%, 10 V	Application dependent
CHP	18 nF, 20%, 100 V	
CDC	820 nF, 20%, 5 V	Application dependent
CDCR	10 nF, 20%, 5 V	Application dependent
CM	10 nF, 20%, 5 V	Application dependent
CSLEW	0.33 μF, 20%, 5 V	Application dependent
CVTX	0.1 μF, 20%, 5 V	
CVRX	0.1 μF, 20%, 5 V	
CB	0.1 μF, 20%, 100 V	
RFA	25 Ω, 2%, 2 W	Value and rating application dependent
RFB	25 Ω, 2%, 2 W	Value and rating application dependent
RRT1	515 kΩ, 1%, 1/8 W	Application dependent
RRT2	12 kΩ, 1%, 1/8 W	
RD	66 kΩ, 1%, 1/8 W	Application dependent
RDCR1	15 kΩ, 1%, 1/8 W	Application dependent
RDCR2	15 kΩ, 1%, 1/8 W	Application dependent
RDC1	50 kΩ, 1%, 1/8 W	Application dependent
RDC2	50 kΩ, 1%, 1/8 W	Application dependent
RT	360 kΩ, 1%, 1/8 W	Application dependent
RRX	220 kΩ, 1%, 1/8 W	Application dependent
RM	68 kΩ, 5%, 1/8 W	Application dependent
ROUT1	47 kΩ, 1%, 1/8 W	Application dependent
RIN	47 kΩ, 1%, 1/8 W	Application dependent
RBAT1	365 kΩ, 1%, 1/8 W	
RBAT2	365 kΩ, 1%, 1/8 W	
RREF1	7.87 kΩ, 1%, 1/8 W	
RNEG	10 kΩ, 10%, 1/4 W	
RSLEW	150 kΩ, 1%, 1/8 W	Application dependent
U1	Le79R79	
U2	TISP61089	
U3	Le79C2031	

DOCUMENT REVISION HISTORY

Revision A

- Originally, this document was printed in the SLIC Introduction chapter of the “Linecard Products for the Public Infrastructure Market Databook” (PID 18503B), pgs. 1-7–1-32.
- The document was again released on the "Communication Products CD-ROM” (PID 21812B) as the SLIC Functional Description.”
- In this document, the first equation under the Ringing Circuit heading, currently on pg. 12, in the last revision contained the following information:

$$\frac{R_{B1}}{R_1} = \frac{R_{B2}}{R_4} = \frac{(R_{LMAX} + R_{FEED})}{R_{LMAX}}$$

  The equation has been changed to:

$$\frac{R_{B1}}{R_3} = \frac{R_{B2}}{R_4} = \frac{(R_{LMAX} + R_{FEED})}{(R_{LMAX} + R_1)}$$

Revision A to B

- Updated OPNs (Ordering Part Numbers) throughout the document

Revision B1 to B2

- Added new headers/footers due to Zarlink purchase of Zarlink on August 3, 2007

For more information about all Zarlink products visit our Web Site at

www.zarlink.com