Minimizing the Number of External SSRAM Chips on Zarlink Packet Processors

Application Note

Issue 2 December 2002

Contents

1.0 Scope

This application note is applicable to the following Zarlink products: MT90502, MT90503, MT92210 and MT92220. Throughout this document, they will be collectively referred to as Packet Processors.

2.0 Introduction

All Zarlink Packet Processors have one or more SSRAM[1] banks that connect to ZBT[2] type SSRAM chip(s). The address bus on each bank is typically 19 bits wide, making 512Kx18 the largest size of SSRAM chip that can be used. Normally multiple SSRAM chips have to be used in order to achieve the maximum capacity of the SSRAM bank.

Each Packet Processor's SSRAM banks are listed in Table 1, along with the bank size and maximum supported chip size. Essentially, at least two SSRAM chips are needed to achieve the maximum allowed bank size.

For the obvious reasons of board space, power and probably cost, it is desirable to reduce the amount of SSRAM chips on each bank without compromising the total size. This becomes achievable when 2MBytes or even larger SSRAM devices are made available in the market. If we could use a single 1Mx18 SSRAM chip to replace two 512Kx18 SSRAM chips, then SSRAM chip count is reduced by half on most of the banks shown in Table 1.

1. Synchronous Static RAM
2. Zero Bus Turnaround

Device	Bank	Maximum size of the bank (bytes)	Maximum size of single SSRAM chip	Minimum SSRAM chips to achieve maximum bank size
MT90502	Bank A	2M	1M (512K x 18)	2
	Bank B	2M	1M (512K x 18)	2
MT90503	Control	1M	512K (256K x 18)	2
	Data	4M	1M (512K x 18)	4
MT92210	Bank A	2M	1M (512K x 18)	2
	Bank B	2M	1M (512K x 18)	2
	Bank C	2M	1M (256K x 36)	2
MT92220	Bank A	2M	1M (512K x 18)	2
	Bank B	2M	1M (512K x 18)	2
	Bank C	2M	1M (256K x 36)	2

Table 1 - SSRAM Chip Count for Maximum Size

3.0 Using Larger-Than-Supported SSRAM

Although it is not directly supported, a larger SSRAM chip, such as 1Mx18, may be used to replace two 512Kx18 chips. This can be done by decoding the two chip select signals and converting them to a single chip select signal and an upper address line. Figure 1 and Figure 2 show the configuration for two 512Kx18 SSRAMs and one 1Mx18 SSRAM, respectively. Although the Data Memory bank on the MT90503 is given as the example, the same idea is applicable to all other banks.

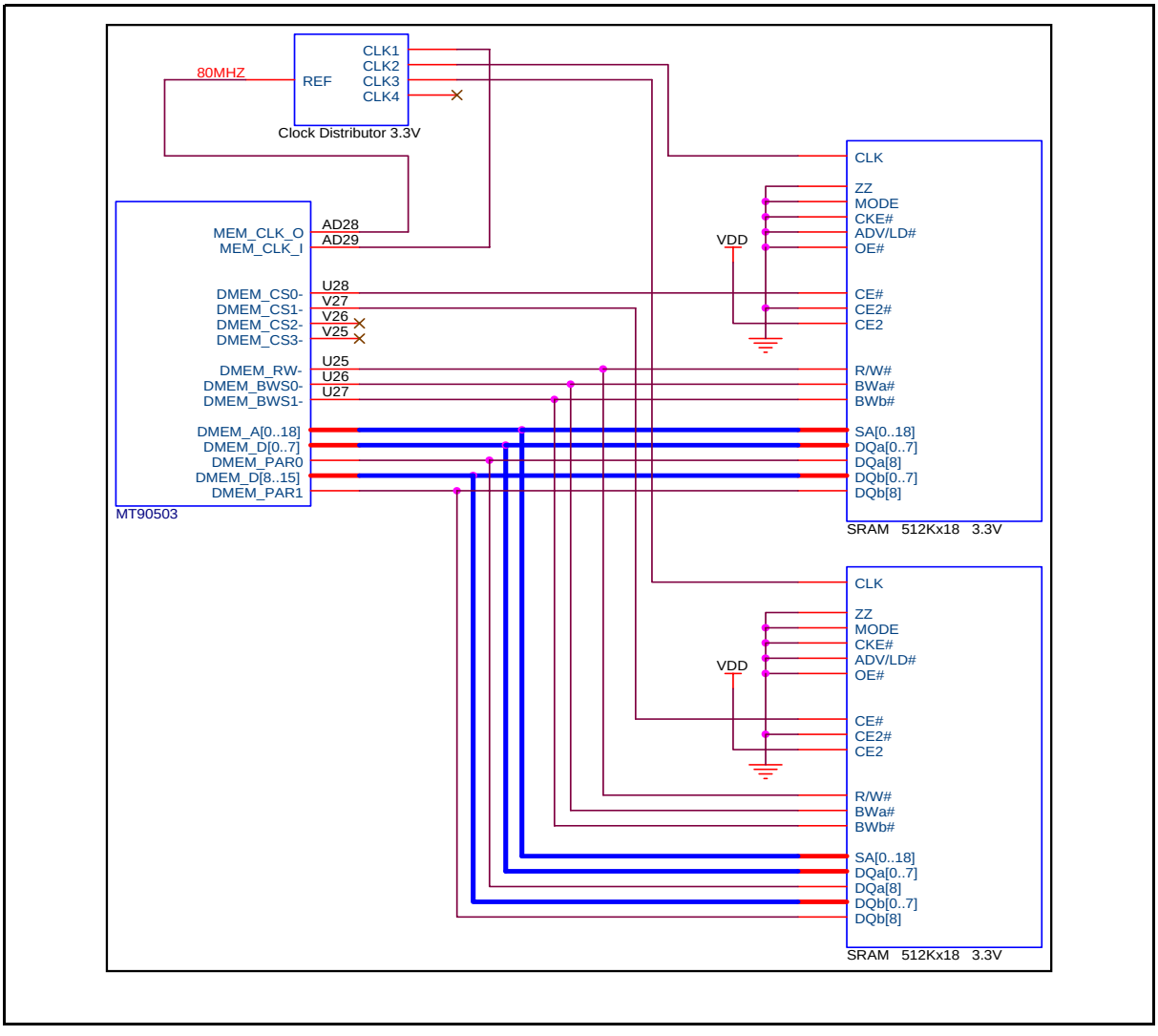

Figure 1 - Two 512Kx18 SSRAM for 2MBytes Memory

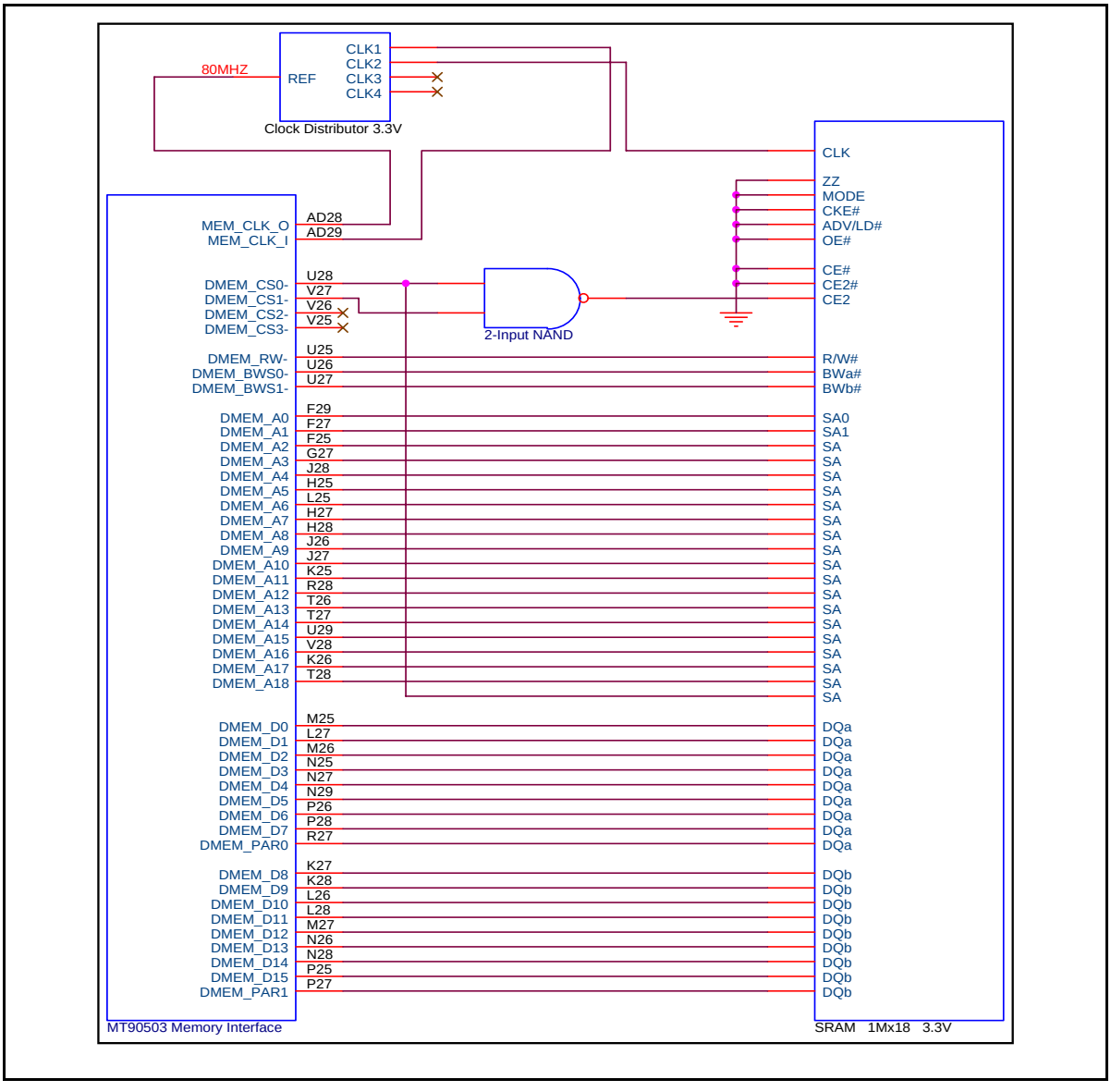

Figure 2 - A single 1Mx18 SSRAM for 2MBytes Memory

4.0 Electrical Timing Analysis

Inserting a NAND gate into the path between the Packet Processor and the SSRAM memory will inject delay on Chip_Select signal that will adversely affect the setup time required by the SSRAM chip. The timing parameters of interest are the output-to-output clock skew from the clock distributor, the propagation delay through the NAND gate, the setup time requirements of the SSRAM chip and the clock to signal valid time from the Packet Processors. The total delay on Chip_Select in the worst case must not exceed one clock cycle time, which is device and application specific.

Component	Part Number	Parameter	Value (ns)	Condition
Zero Delay Buffer	Cypress CY2308SC-1H	Output to Output skew (maximum)	0.2	All outputs equally loaded
2-Input NAND	Pericom PI74ST1G00	Propagation Delay (maximum)	1.9	C_L = 15 pF R_L = 1 MΩ Vcc = 3.3V +/- 0.3V
1Mx18 SSRAM	Cypress CY7C1372B-133	Chip Select Set-up Time (minimum)	1.5	
Packet Processors		Clock to signal valid (maximum)	8.3†	C_L = 50 pF
		Total delay	11.9	

Table 2 - Timing Analysis

† 8.3 ns for MT90502 and MT90503; 8.1 ns for MT92210 and MT92220.

Table 2 above shows the timing specifications for a selected group of external components. The worst case total delay is 11.9ns, which translates to a maximum memory clock frequency of 84MHz that the implementation shown in Figure 2 can support. An 80MHz memory clock is sufficient for all MT90502 and MT90503 operations; and is also enough for most of the MT92210/MT92220 operations. In case a higher memory clock frequency (e.g. 100MHz) is needed for a specific application on the MT92210 or the MT92220, delay could be further reduced by the following methods:

- select a faster SSRAM to reduce the set-up time
- select a faster NAND with a smaller propagation delay
- reduce the capacitive load on the Chip_Select output to decrease the signal valid time.

Please consult the respective datasheets of each of the components listed above for more details.

5.0 Conclusion

2MBytes SSRAM devices can be used with Zarlink Packet Processors to reduce the number of external SSRAM chips required. The circuit and components shown in Figure 2 and Table 2 may be used for applications with memory clock of 80MHz or less.

Device	Bank	Maximum size of the bank (Bytes)	SSRAM chip size (Bytes)	SSRAM chips to achieve maximum bank size
MT90502	Bank A	2M	2M (1M x 18)	1
	Bank B	2M	2M (1M x 18)	1
MT90503	Control	1M	1M (512K x 18)	1
	Data	4M	2M (1M x 18)	2
MT92210	Bank A	2M	2M (1M x 18)	1
	Bank B	2M	2M (1M x 18)	1
	Bank C	2M	2M (512K x 36)	1
MT92220	Bank A	2M	2M (1M x 18)	1
	Bank B	2M	2M (1M x 18)	1
	Bank C	2M	2M (512K x 36)	1

Table 3 - New SSRAM Chip Count for Maximum Size

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE