ZARLINK SEMICONDUCTOR

Introduction to Features and Design Benefits of the 512 Channel Switching Family

Application Note

Contents

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1.0 Summary

This application note introduces the key features that are offered in the ZL50010: Flexible 512-ch DX with Enhanced DPLL. In conjunction with the feature list, a typical application is shown where reduction of both cost and space occurs by replacing previous components with the new device.

More functionality is now being integrated into semiconductor devices. These new features allow the device to interact with the other system components with less contention, and simplifies the overall system design.

Designing a 512 channel TDM switching card with the ZL50010 results in a board space saving of over 86% and a cost saving of over 42% by replacing four 256 channel switches and a Stratum 4 Enhanced PLL.

2.0 Features

The ZL50010/11/12 family of switches offers a set of features that have previously only been included in high density devices. These features allow the device to interact with the other system components with less contention and simplifies overall system design.

2.1 Integrated DPLL

Integration of a Stratum 4 Enhanced DPLL enables a single device to provide the system timing and the switching functionality required. The DPLL of the ZL50010 meets the Stratum 4 Enhanced requirements from the Telcordia GR-1244-CORE standard, and includes a holdover mode, which allows the device to support the system as a timing master, or as a slave. The device accepts two separate reference signals at rates of 8kHz, 1.544MHz or 2.048MHz. These reference signals do not have to be set to the same rate. When one reference source is lost, the ZL50010 enters holdover mode and uses the internal memory that has been storing timing information for the past 32-64ms. This ensures that the switch will continue to be aligned with the lost source if the reference source is recovered. After a period of time designated by the system architect, the DPLL switches to the secondary reference source. This is a seamless transition from one source to the other. When the primary reference is recovered, the device enters holdover mode for a period of time before making a transition to the primary source.

The ZL50010/11/12 have three pairs of programmable output timing pins. These pins can be set to output timing signals at 4.096MHz, 8.192MHz, 16.384MHz or 32.764MHz and the corresponding frame pulse signals with widths of 244ηs, 122ηs, 61ηs or 30ηs. With these output signals, other devices in the system are aligned with this switch, the master timing device. To facilitate proper alignment, the programmable output timing signals can be set to have inverse polarity.

Figure 1: Integrated DPLL with Reference and Output Timing shows the accepted input reference sources from external components, such as an MT9072 framer. The clock and frame pulse signals on the output timing pins, CKo0-CKo2 and FPo0-FPo2, are generated by the part and can be used as the master timing for other devices in the system.

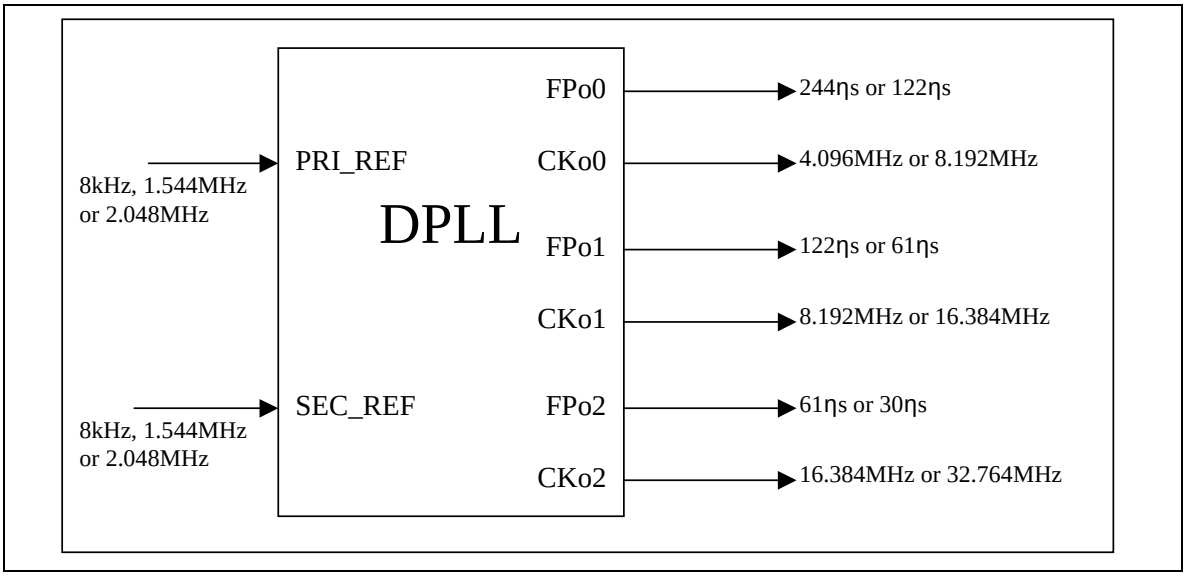

Figure 1 - Integrated DPLL with Reference and Output Timing

2.2 Rate Conversion

Peripheral components may require traffic to be input at different rates. The ZL50010 assists this by converting output traffic to be generated at a different rate than the rate it was input into the switch. The device has 16 input pins (STi0 – STi15) that can accept traffic at 2.048Mb/s, 4.096Mb/s or 8.192Mb/s. Each input pin can be configured for a different input data rate. Once the traffic goes through the switch it can be converted at the output on the 16 output data pins (STo0 – STo15) at 2.048Mb/s, 4.096Mb/s or 8.192Mb/s. Each pin can be individually configured to operate at any one of the three rates. At maximum capacity, the device can conduct switching of 512 channels on both the input and the output pins. This results in all 16 pins operating at 2Mb/s, 8 pins operating at 4Mb/s, 4 pins operating at 8Mb/s or any combination as long as the total capacity does not exceed 512 channels.

Figure 2: Per Stream Rate Conversion shows how any input stream can be configured at one of three different input data rates (2Mb/s, 4Mb/s or 8Mb/s) and can be converted to any of the three output data rates (2Mb/s, 4Mb/s or 8Mb/s).

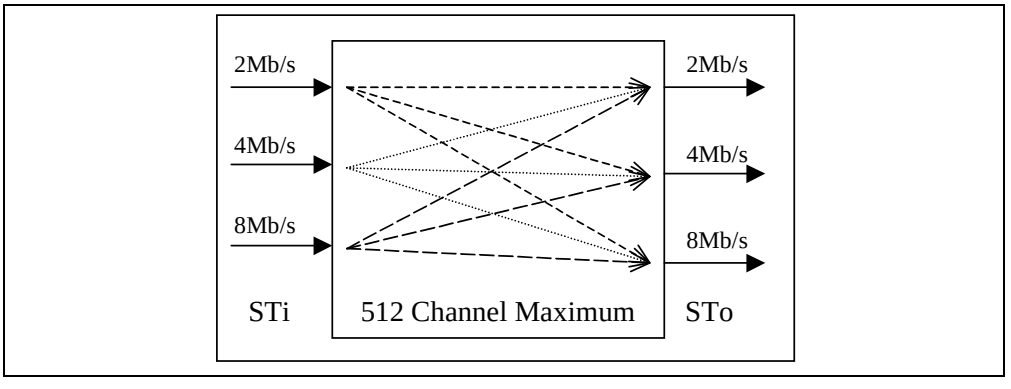

Figure 2 - Per Stream Rate Conversion

2.3 Dedicated High Impedance Lines

The ZL50010/11/12 has16 dedicated pins for serial output stream high impedance control (STOHZ0 – STOHZ15). These pins are used to enable external tri-state buffers. When an output channel is in the high impedance state, the STOHZ drives high for the duration of the corresponding output channel. When the STo channel is active, the STOHZ drives low for the duration of the corresponding output channel.

The use of these pins is applicable under three conditions. First, upon power up these pins are driven high, effectively turning off the output pins of the switch. This eliminates corruption of data when the device is applied to a backplane. Second, these pins are also used when the card is removed from the backplane. By driving these pins high, the output channels will again enter high impedance so that the card is no longer transmitting traffic in a hot swap application. Finally, multiple devices can be connected to the same backplane and share the stream. When one device requires access to the stream the high impedance is driven low, enabling output capabilities. When a different device requires the use of the backplane, all of the other devices will drive STOHZ high, disabling their output abilities.

The high impedance signals, by default, follow the timing of the output streams. This includes when the output bit advancement or output channel delay features are used. The high impedance control will follow the offset of the output signal. However, the user can further advance the high impedance control by up to four 15.2ηs steps. The advancement is useful when taking into account the turn on time of the high impedance driver as shown in figure 4.

Figure 3: High Impedance and Advancement shows how the output traffic operates when the tri-state control is utilized. With the advancement feature, the STOHZ is advanced by ¼ bit to better align the control with the system requirements.

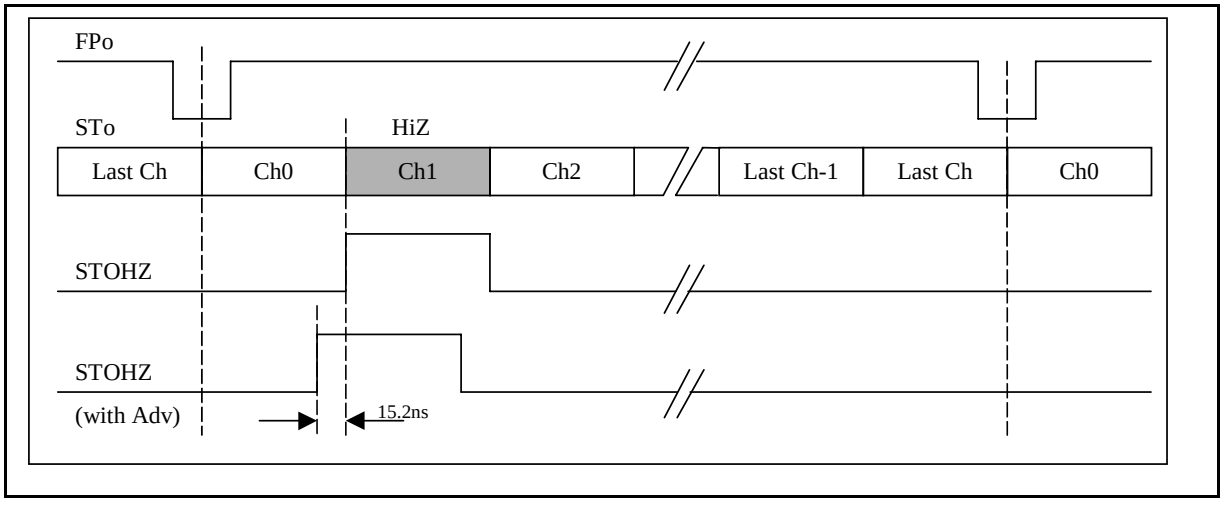

Figure 3 - High Impedance and Advancement

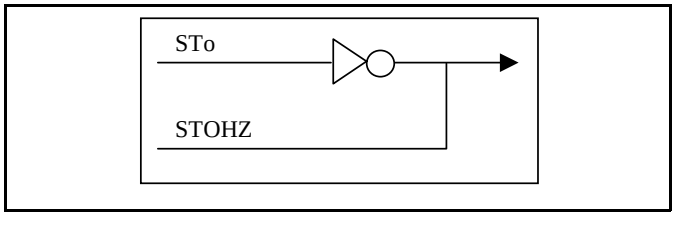

Figure 4 - STOHZ Driver

2.4 Input Bit Delay/Output Bit Advancement

Delay and advancement features have been included in the device to compensate for various delays that occur in the system. Registers settings are used to align the traffic on both the input and output pins of the switch. Both the input and output can be moved by up to 7 ¾ bits in total, with a ¼ bit resolution.

In Figure 5: Per Stream Input Delay the ZL50010 is the master timing device for the ZL500211: 256 Channel Voice Echo Cancellers, providing the required 4.096MHz clock and frame pulse signals. The voice is input into the switch from the backplane, where it is routed to the voice echo cancellers. The voice noise is removed by this part, and then returned to the switch so it can be returned to the backplane. As the voice travels from one device to another propagation delays affect the traffic. With input bit delay and output bit advancement features, the traffic will be properly aligned with the timing signals created by the ZL50010. This ensures that interoperability and loss prevention are present.

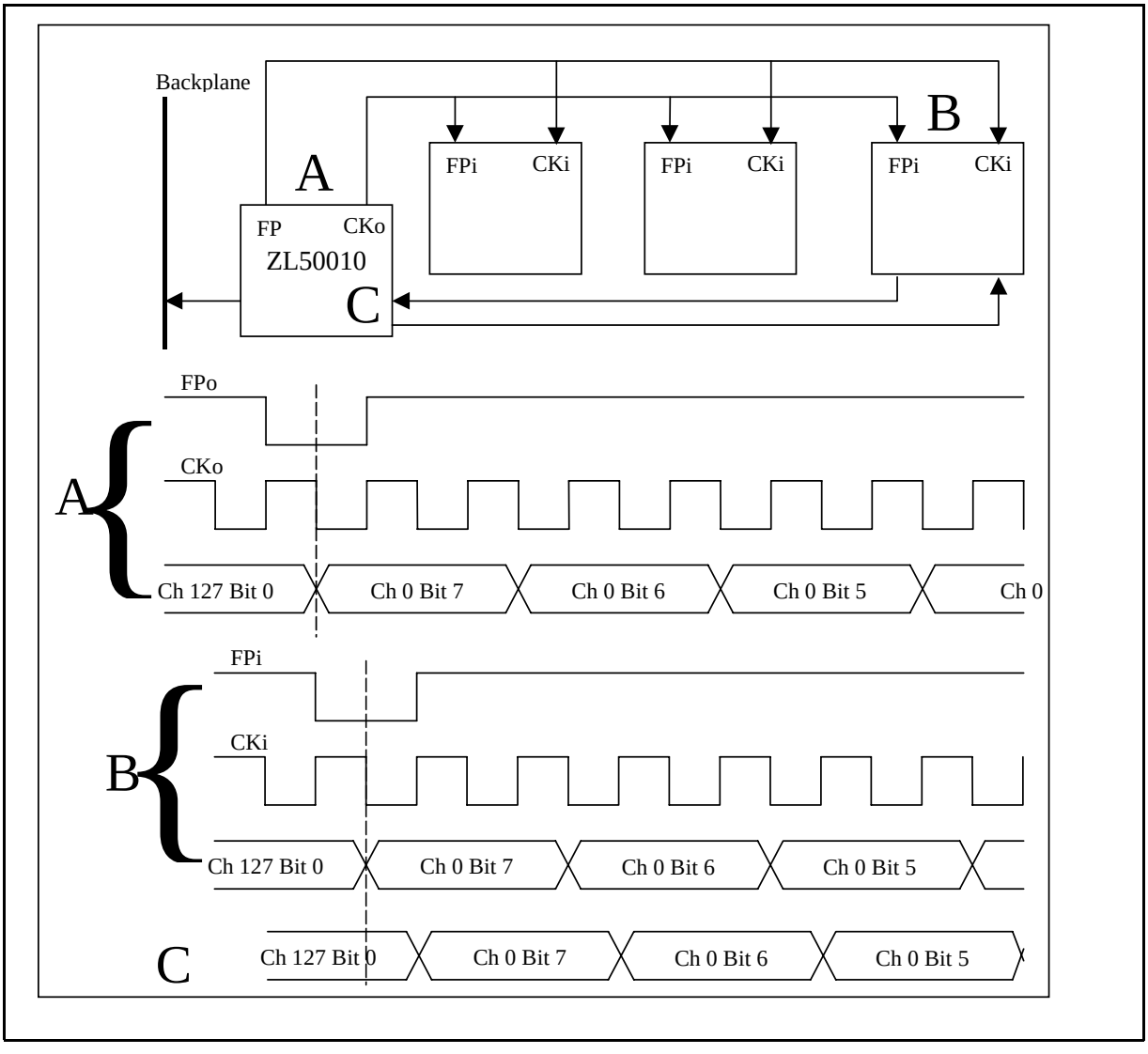

Figure 5 - Per Stream Input Bit Delay

3.0 Applications

The ZL50010 Flexible Digital Switch with Enhanced DPLL can be used in various systems. The switching capacity of 512 channel by 512 channel makes it the ideal solution for small and medium digital switching platforms which includes, but is not limited to, “Voice over IP” PBX, remote access servers, digital loop carriers and time division multiplexers.

Figure 6: Typical PBX shows an example of a PBX system. In previous designs, the MT8980 was used in a matrix style to duplicate the switching capacity of the ZL50010. As the MT8980 has a 256 channel by 256 channel switching capacity, it requires four parts to duplicate the same capacity as the ZL50010 in a non-blocking format. Also included in the system is a Stratum 4 Enhanced PLL to provide the master timing for the MT8980 switches and other devices in the system. This PLL accepts the primary and secondary reference sources from the MT9072 framers and provides the timing to the framers and the switches. Finally, there is an FPGA on the system to convert the 2Mb/s output traffic from the MT8980 matrix to an 8Mb/s rate for interfacing with the backplane.

Figure 7: PBX with ZL50010 illustrates how a single ZL50010 can eliminate six separate devices. The increased capacity of the switch enables removal of all four of the MT8980 switches. With the embedded DPLL, the Stratum 4 Enhanced PLL can be removed. And finally, the FPGA rate conversion functionality can be removed as the ZL50010 has a built-in per stream rate conversion feature.

The replacement of these devices results in very large savings, both in space and in cost. The MT8980 switches, in their smallest package measures 17.65mm by 17.65mm for a total area per part of over 311.5mm^2. When the four devices are used in a matrix style, the area is multiplied to require 1246mm^2 of total board space. This does not take trace lines into account. The ZL50010, in the smallest PBGA package has the dimensions of 13mm by 13mm, or a total area requirement of 169mm^2. This results in a total saving of over 86%, without considering the space for the PLL. Cost will also be saved. Again without taking the PLL into account, the savings on the switches alone will be over 42%.

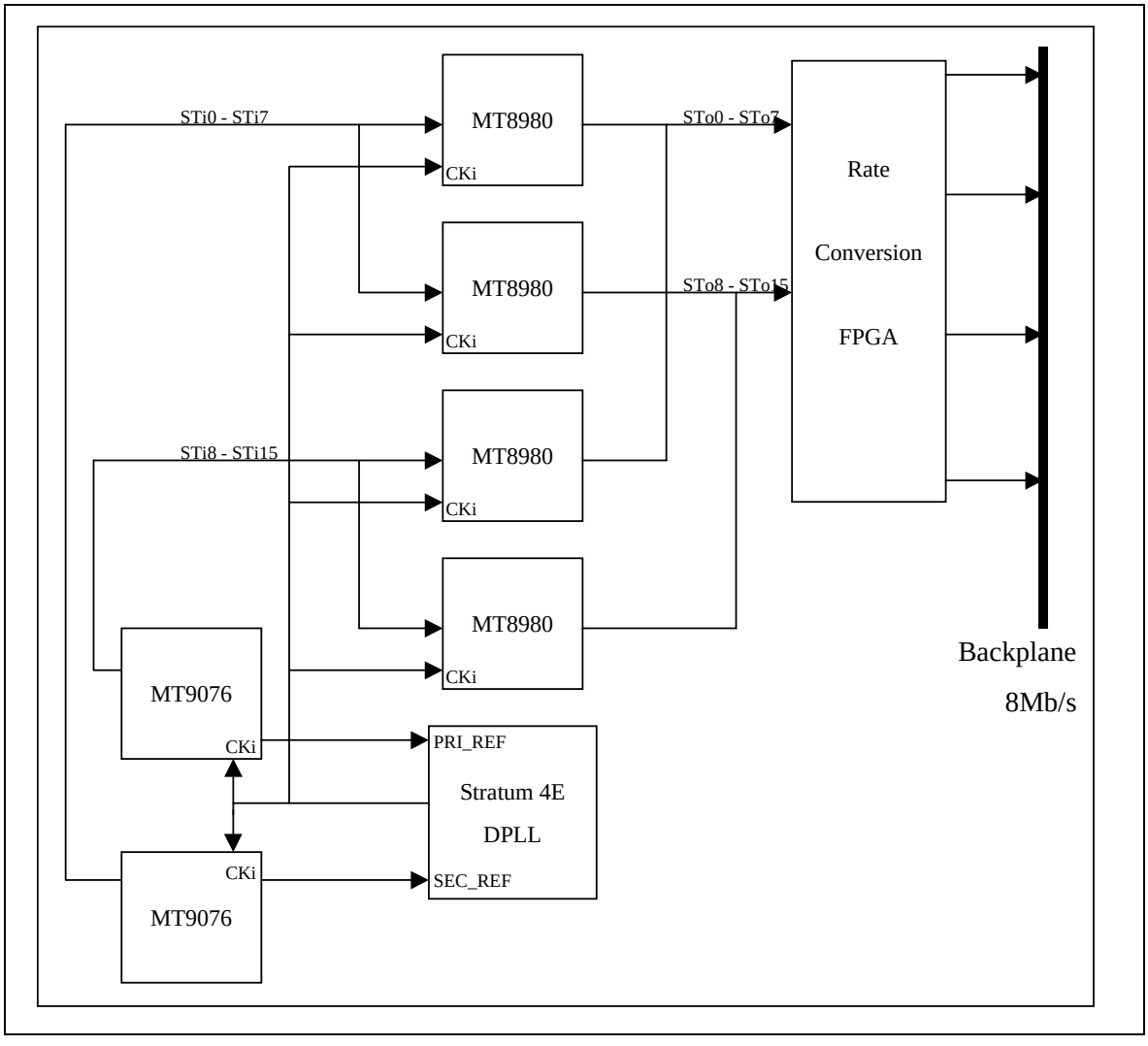

Figure 6 - Typical PBX

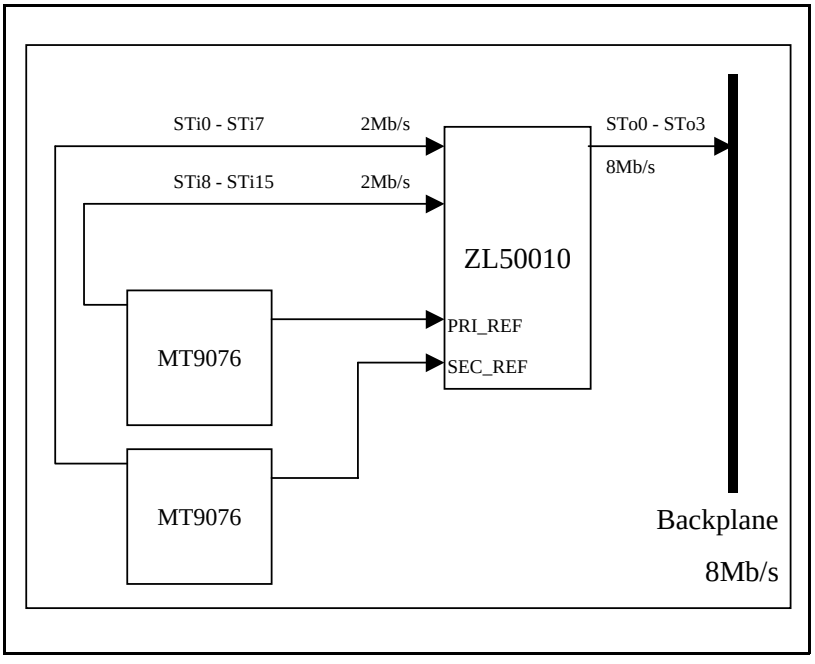

Figure 7 - PBX with ZL50010

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