

December 2004

1.0 Introduction

Traditionally, IMA (Inverse Multiplexing for ATM) is widely adopted in E1/DS1 applications. With emerging G.SHDSL (Single-pair High rate Digital Subscribe Line) standard, it is now viable to apply IMA over SHDSL lines.

This application note provides a solution of IMA over up to 16 G.SHDSL lines. It serves as a reference design of interfacing MT90224 to Metalink's MTS870 chipset.

MT90224 is the second-generation IMA device from Zarlink, which supports IMA over 16 serial bit streams running at a maximum of 2.5Mbps. It also incorporates UTOPIA Level 2 (and Level 1) bus as ATM interface.

The MTS870 chipset contains 8 channels DSL framers that support multiple modes of Symmetrical DSL like ITU G.SHDSL, the ETSI SDSL, and the ANSI HDSL2

MT90224 together with MTS870 and Metalink's AFE chipsets together provide a complete solution for IMA over G.SHDSL that meets both IMA version 1.1/1.0 specification and G.SHDSL specification.

2.0 Notification

This reference design is showing how to connect MT90224 to MTS870 chipset. In the schematic that follows, MT90224 is shown with full pinout and surrounding circuitry. Only the data interface pins on MTS870 chipset are presented to illustrate the interconnection. For detailed reference design of MTS870 chipset please contact Metalink.

The MT90224 device shown in this reference design can be replaced by MT90223 (Octal) or MT90222 (Quad), two IMA devices from the same family. Both MT90223 and MT90222 are pin and functional compatible to MT90224.

3.0 Schematics Content

- The top-level diagram is represented on the first page.
- Second and third pages contain the detailed schematics of MT90224.
- Data interface of MTS870 is shown on the fourth page.

4.0 Modes of Operation

The following modes of operation must be selected and programmed:

1. MT90224 mode: Unframed, serial bit stream mode up to 2.5 Mbit/s.
2. MT90224 Recommended register settings:

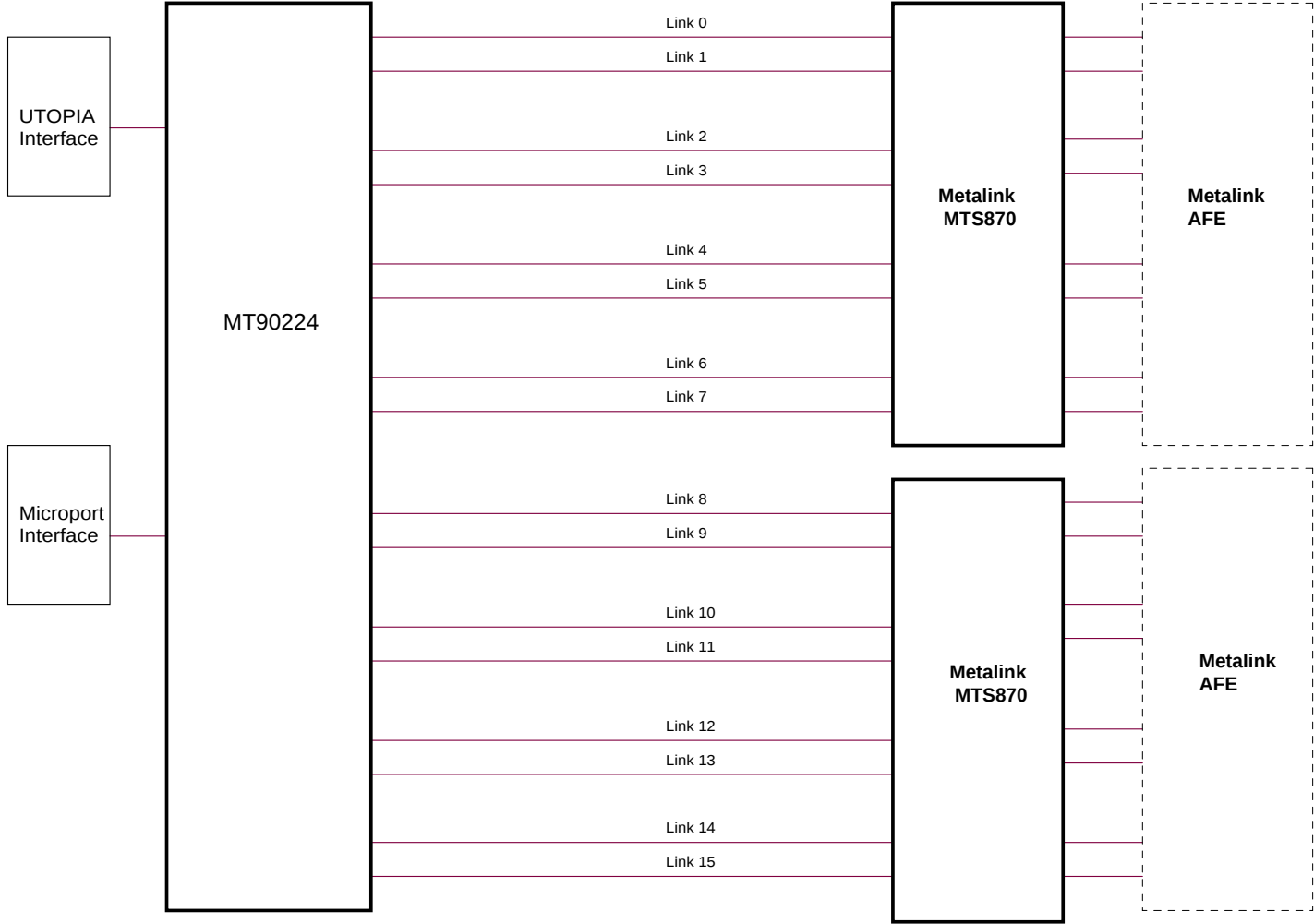
TDM Tx Link Control Register	0x0600	should be set to 0x00A3,
	0x0601	should be set to 0x04A3,
	0x0602	should be set to 0x08A3,
	0x0603	should be set to 0x0CA3,
	0x0604	should be set to 0x10A3,
	0x0605	should be set to 0x14A3,
	0x0606	should be set to 0x18A3,
	0x0607	should be set to 0x1CA3,
	0x0608	should be set to 0x20A3,
	0x0609	should be set to 0x24A3,
	0x060A	should be set to 0x28A3,
	0x060B	should be set to 0x2CA3,
	0x060C	should be set to 0x30A3,
	0x060D	should be set to 0x34A3,
	0x060E	should be set to 0x38A3,
	0x060F	should be set to 0x3CA3.
TDM Tx Mapping Registers	(0x0610 - 0x061F)	should be set to 0xFFFF.
TDM Tx Mapping Registers	(0x0620 - 0x062F)	should be set to 0xFFFF.
TDM Rx Link Control Register	(0x0700 - 0x070F)	should be set to 0x04A3.
TDM Rx Mapping Registers	(0x0710 - 0x071F)	should be set to 0xFFFF.
TDM Rx Mapping Registers	(0x0720 - 0x072F)	should be set to 0xFFFF.
Rx Automatic ATM Synchronization Register	(0x0741)	should be set to 0x0036

3. MTS870 chipset provides RxCLK to MT90224, while the TxCLK is generated by MT90224 (from respective RxCLK) and output to MT90224.

4. MTS870 chipset should be configured in transparent (datapump) mode.

For detailed programming and pinout of MTS870, please refer to Metalink's data sheet and G.SHDSL Transceiver Reference Design.

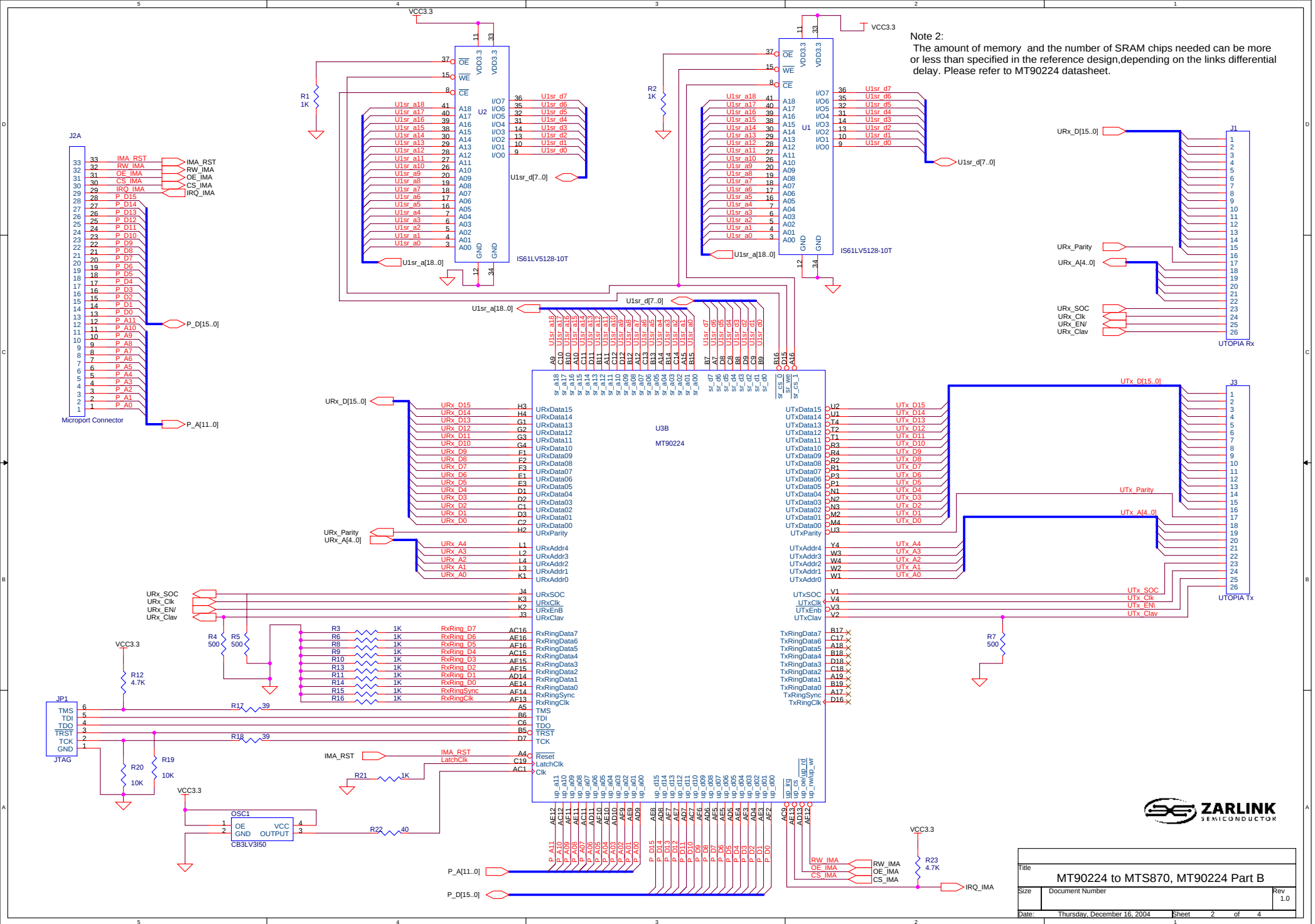
Interfacing Zarlink MT90224 IMA device to Metalink MTS870
Octal G.SHDSL/SDSL/HDSL2/HDSL/IDSL Transceiver Chip
Set

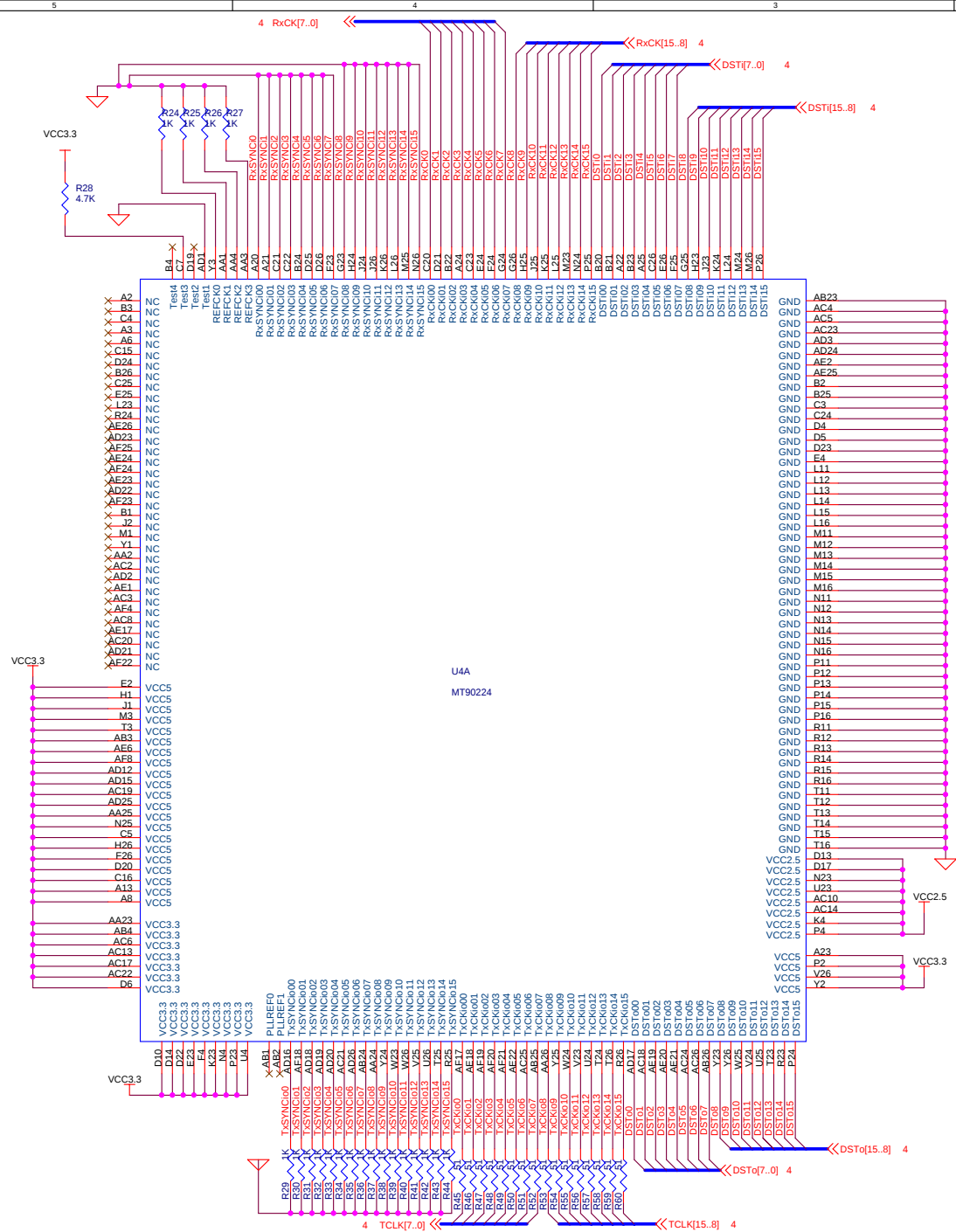


Note 1:
Decoupling capacitors are not shown in the reference design.
They should be placed where needed.

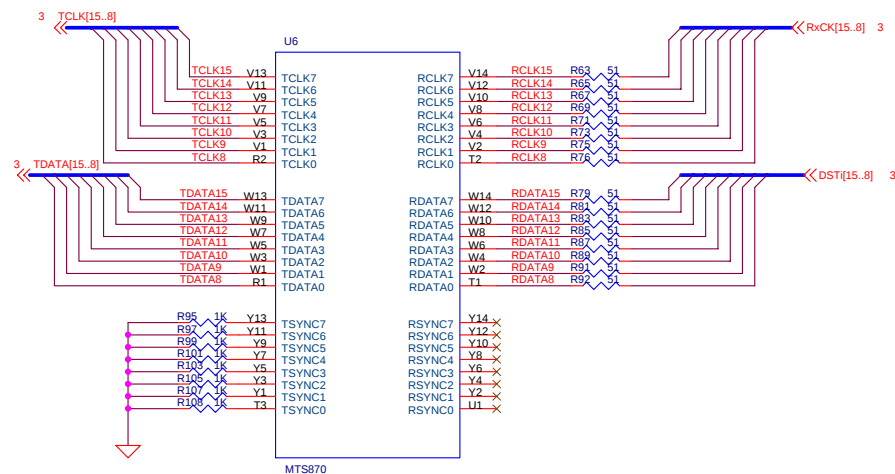
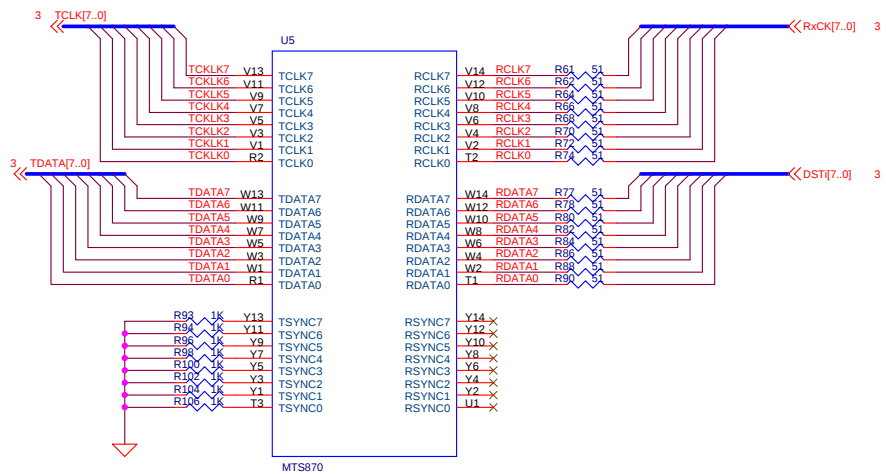


Title			
MT90224 to MTS870, Block Diagram			
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Note 3:

MTS870 chipset configuration:

- Datapump or unframed mode.
- Refer to Metalink's documents: MTS870 datasheet and Metalink's G.SHDSL Transceiver Reference Design



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MT90224 to MTS870, MTS870			
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