MSAN-191

Designing a HotSwap Board with Zarlink Components

Application Note

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Contents

1.0 Overview

Some of Zarlink's devices are compatible with the Enterprise Computer Telephony Forum (ECTF) H.110 specification. The H.110 specification allows the designing of applications suitable for use in a CompactPCI platform. The CompactPCI platform offers attractive features such as hot swappable cards, integrated PCI and H.110 TDM buses, and a rugged backplane and a mechanical design. This new standard is replacing the older ribbon-cable based bus standards such as MVIP-90, H_MVIP and SCbus. The advantages of a hot-swap capable design in this architecture are numerous. This technical note details the specifications that must be met in order to design a HotSwap card, and presents a design using Zarlink devices.

Hot Swap is the ability to perform live insertion and removal of boards and other components. The challenge of this process lies in preventing interference with the signals on the backplane and avoiding disturbance of the DC voltage levels on the backplane power rails. The H.110 Hardware Compatibility Specification from ECTF adds several important details to the PICMG 2.0 R2.1 CompactPCI specification about achieving HotSwap.

Preventing interference and avoiding voltage disturbance can be achieved in two ways. First, by limiting the overall capacitance connected to the power pins. The in-rush current is reduced when the board is first connected to the backplane. Second, by making the various data lines appear to be open (tri-state) and then charging the lines to just under 1 volt before the data lines actually contact the backplane, disturbance on the backplane signals is minimized. After the board is fully seated in the backplane and power has stabilized on the card, the data lines can be brought out of tri-state and the board begins to communicate over the CT Bus on the CompactPCI bus.

The specifications and circuitry that accomplish these requirements are discussed in detail in this application note. Section 4 of the CompactPCI Core Specification covers the actual physical design of the card (connector implementation, etc) in detail, and is beyond the scope of this document.

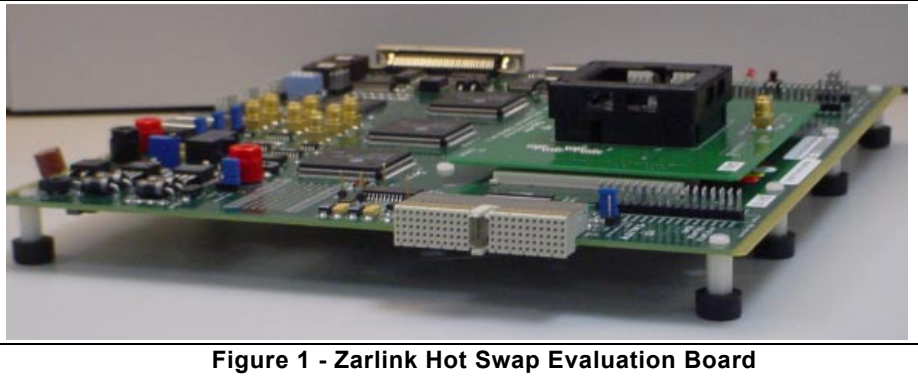

Figure 1 - Zarlink Hot Swap Evaluation Board

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2.0 System Models

There are three Hotswap architectures. The three architectures vary depending on the process of hardware and software connections. The simplest system provides limited control by the software to the connection processes and requires a high level of operator interaction, whereas the most complex system is entirely software controlled.

System Type	Hardware Connection	Software Connection
Basic Hot Swap	Automatic in Hardware	Manually by Operator
Full Hot Swap	Automatic in Hardware	Automatic by Software
High Availability	Controlled by Software	Controlled by Software

Table 1 - Hotswap Architectures

- The basic hot swap architecture describes the attributes needed to plug and unplug a board without disturbing bus activity and requirements to ramp board power up and down to prevent loading the backplane or generating sparks. This is done on the plug-in board, as the backplane is entirely passive. Software control, if used, is done by operator intervention at a console.
- The full hot swap builds on the basic model and defines a method to indicate to the operating system of the impending insertion or impending extraction of a board. An enumeration interrupt, ENUM#, is used to inform the OS of the impending event. After the OS has shut down the board's functions, it signals the operator via an LED that it is safe to remove the board. When a new board is installed, the OS automatically configures the system software. This signaling method allows the operator to install or remove boards without the extra step of reconfiguring the system at the console.
- The high-availability model significantly enhances the performance and the complexity of the system by allowing software to control the board's state. Radial control lines to the CPU inform the OS that a board is present and initiate the power up. As before, the power ramp controller is on the plug-in board. The plug-in board indicates to the OS that it is powered up and it asserts a “healthy” signal. The system then uses radial signals from the CPU to release the board from reset. It is then electrically connected to the bus. Software connection then proceeds in the same way as defined by the full model. Duplicate boards can coexist in the same chassis so individual boards that fail can be isolated, shut down, and replaced by another board. This model adds a special hot swap controller that manages the entire process and allows for unattended fault recovery and, in some cases, unattended repair.

The reference design presented by Zarlink Semiconductor is a Basic Hot Swap design, and does not take into consideration the software that would be needed to control a full hot swap or high-availability board.

3.0 Physical Connection Process

The CompactPCI connector contains three different lengths of pins: short, medium and long. When an insertion or removal is occurring, the different lengths of these pins are used to put the card into the necessary states to avoid interfering with traffic on the backplane.

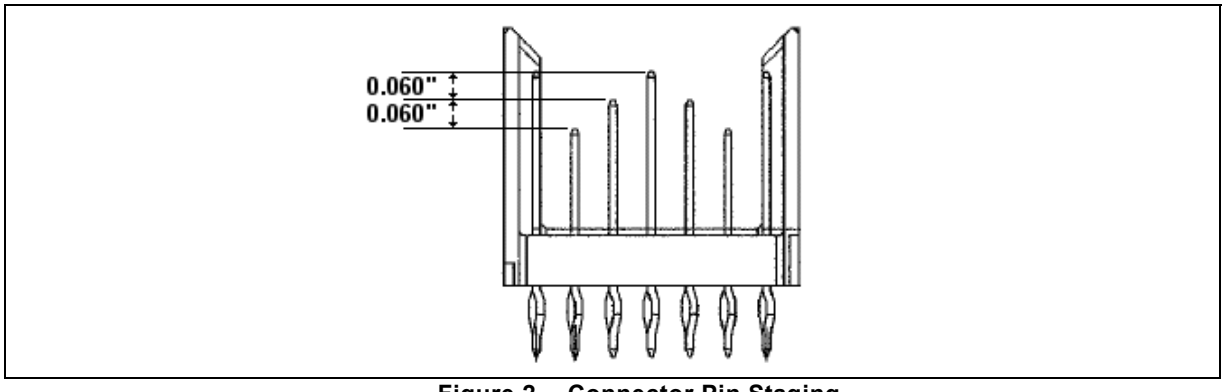

Figure 2 - Connector Pin Staging

- The longest pins on the connector make contact with the backplane first. These pins are comprised of the +5V, +3.3V, Ground and Frame Ground pins. These pins are referred to as early power because they provide the card with the preliminary power in order to interface to the backplane without disturbing it. Other than the ground pins, these pins are not typically used to power the rest of the card in normal operation after successful card insertion.
- The medium pins on the connector make contact after the long pins. These pins are comprised of data, control and clock lines, as well as +5V, +3.3V and ±12V. The medium power pins are typically switched on by power FETs on the card when the insertion process has been completed successfully. These FETs are generally controlled by a hotswap power controller, such as the SMH4042 or LTC1421.
- The short pins are used to signal to the card that it has either completed insertion or that it is about to be extracted. These pins signal the onboard power controller to tri-state the data, control and clock lines, as well as reset and power down the unused local card logic.

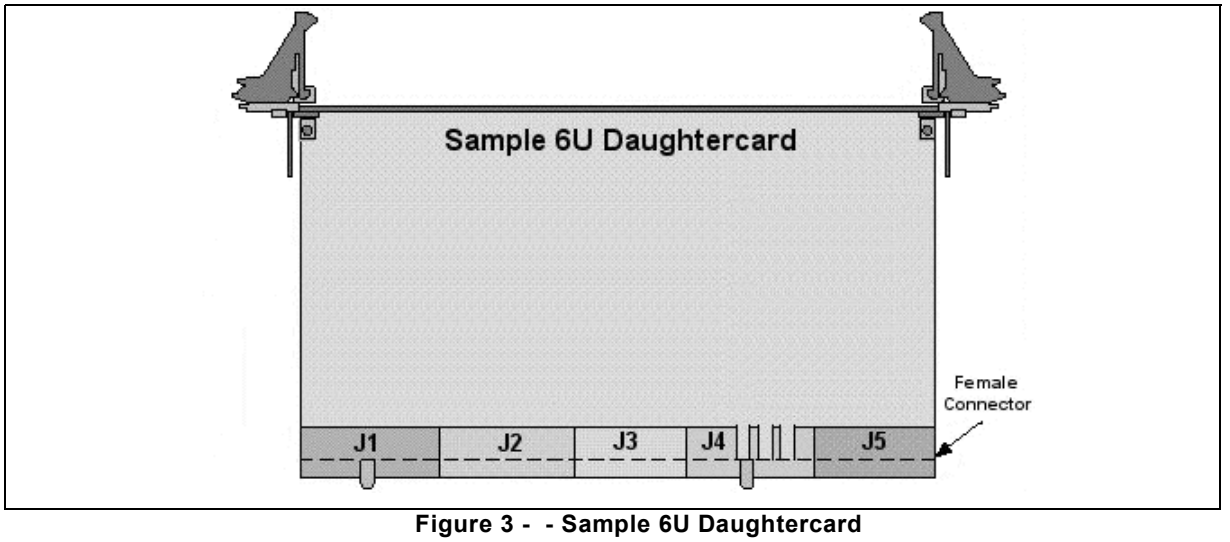

Figure 3 - - Sample 6U Daughtercard

As the card is inserted or removed, there is a required minimum of 4 ms between each length of pin contacting or breaking contact with the connector. This comes from assuming that the worst case pin staging time delay is 0.7 ms per 0.010" of pin length. Therefore, the standard 0.060" pin stagger will result in a 4 ms of delay per pin stage.

3.1 Insertion Process

1. The card is in uninstalled state and the physical connection process begins.
2. The card enters the card guide.
3. The card front panel is discharged to FRAME ground through a bleed resistor. This prevents electrostatic discharge from damaging the components.
4. Card logic is discharged to FRAME ground through a bleed resistor. This discharges the decoupling capacitors on the card in order to prevent an inrush of current from the card to the backplane. This current could either disrupt the backplane or, if the current was large enough, could possibly physically damage the backplane.
5. The bleed resistor breaks contact with frame. Card logic ground is again isolated.
6. Card front panel makes low resistance contact with frame.
7. Card contacts long pins on backplane (ground, +5V, +3.3V, and V(I/O)). Card is in unstable state while pins are first mated.
8. Card contacts pins to achieve a stable Early Power.
9. CompactPCI bus interface logic is powered up, and decoupling capacitors attached to early power are charged. This provides reasonably stable early power to the interface portion of the card.
10. The peripheral's local reset is driven active, and all necessary CTBUS data/control/clock pins signals are asynchronously tri-stated in order to isolate the CompactPCI interface from the presently unpowered circuitry on the card.
11. The card's CompactPCI bus interface pins are precharged to the required potential (0.54V - 0.88V) from Early Power. This allows these pins to contact the associated pins on the backplane connector without disturbing the signals that are present on the backplane.
12. Hotswap logic is reset with the LED initially in the ON state. This LED provides feedback to the operator that insertion can be completed.
13. A minimum of 4ms after the long pins contact, the card contacts the intermediate pins on the backplane.
14. The CTBUS data/control/clock pins make first contact with the bus.
15. The card's CompactPCI pins begin to track the levels on the PCI bus. The card is now receiving the PCI clock.
16. Medium length power pins contact. Input power to the power FETs is available (FETs are still turned off at this point). These power FETs are used to turn on stable power to the backend of the card when insertion has been completed successfully.
17. Board contacts the short BD_SEL# (J1) or short /CT_EN (J4) pin, depending on the exact configuration of the card. This pin is grounded on the backplane (or controlled for high availability platforms) and pulled high by a pull-up resistor on the board. Its assertion indicated that the board has been fully inserted into the backplane.
18. Precharge potential is optionally removed.
19. The card enters installed state. At this point, the power FETs can be turned on in order to power up the backend of the card, and the local PCI reset signal can be removed. The card is ready to be used.

3.2 Extraction Process

1. The card is in the installed state and the operator starts to withdraw the card.
2. The BD_SEL# (J1) or /CT_EN (J4) pin, depending on the configuration of the card, disconnects. This signal is debounced for use as the trigger for the withdrawal sequence. This notifies the card power controller/logic that the card is about to be removed.
3. Local reset is activated for the peripheral logic if it has not already been activated as part of a High Availability Extraction or failed insertion. This holds the backend of the card in a reset state in preparation for power-down.
4. Precharge power is applied if it had been removed as part of the insertion process. This prevents the card from corrupting signals on the data/control/signal lines of the backplane during card removal.
5. Peripheral power is turned off. This minimizes power consumption during the extraction.
6. If any hazardous potentials have developed during the operation of the card, they must now be discharged before the operator can make contact with them.
7. Card logic should be stabilized at this point such that any re-insertion will not cause bus or power subsystem faults due to decaying peripheral power, partially valid memory locations, etc.
8. Medium length PCI pins disengage.
9. Long power and ground pins disengage.
10. Card logic ground is connected to FRAME through a bleed resistor. This discharges any capacitors that might continue to hold a charge after the card has been removed. This is to minimize the possibility upon re-insertion of an inrush of current from the card to the backplane.
11. The card front panel is connected to FRAME through a bleed resistor. This discharges any electrostatic charge that may have built up during card operation.
12. Card leaves the ESD guide.
13. The card is in the uninstalled state.

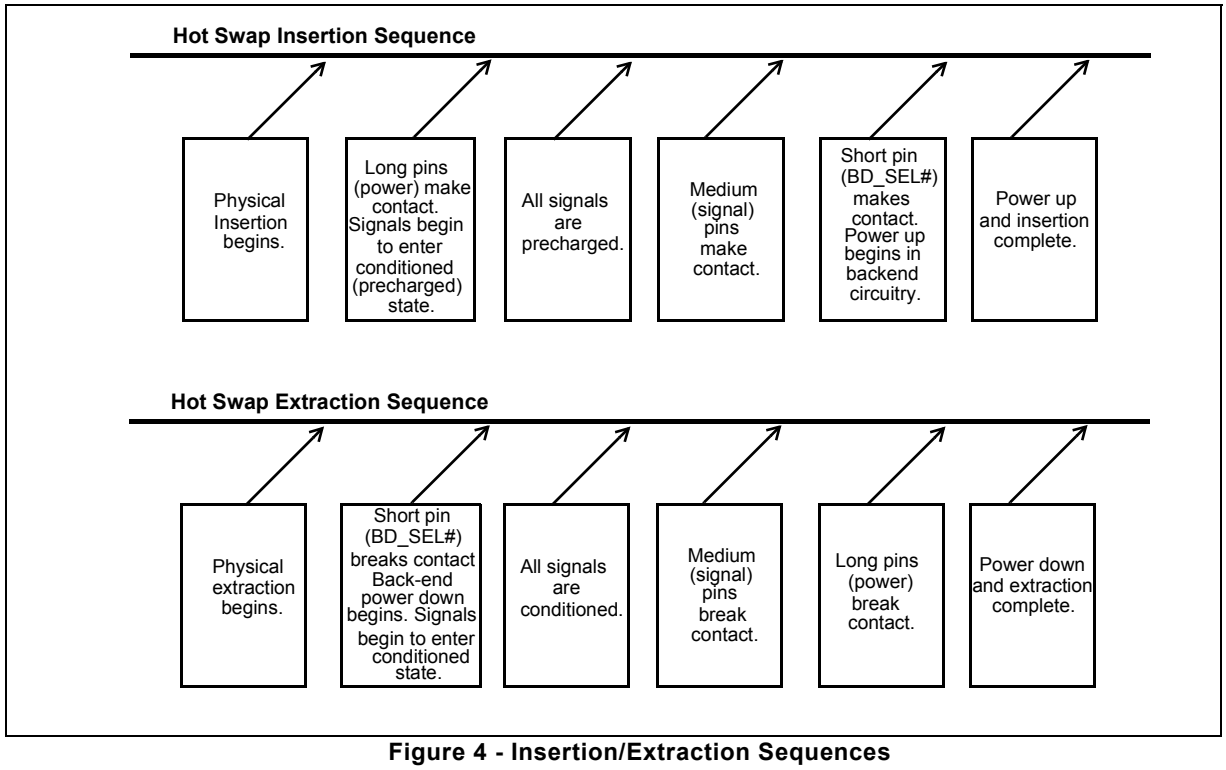

Figure 4 - Insertion/Extraction Sequences

4.0 Hot Swap Technical Specifications

This section lists the relevant specifications to consider when designing a hotswap card. These specifications may change slightly in the future as ECTF is planning to combine the CompactPCI Hot Swap Specification PICMG 2.1 R1.0 with the H.110 Hardware Compatibility Specification. The following specifications are derived primarily from the H.110 spec from ECTF. This application note does not eliminate the need to read and fully understand the official H.110 and PICMG 2.1 specifications.

4.1 Power Usage

This section discusses the Early power usage, necessary power isolation, as well as allowed current usage.

4.1.1 Early Power Usage

Early power is defined as the unswitched side of the power bus, and the following statements must be true:

1. The current surge through any single pin must not exceed 2 amps and must settle to within 5% of its sustained DC level within 100 microseconds.
2. The total sustained DC current drawn though the long early power pins must not exceed 2 amps.
3. In order to minimize a current surge on insertion, there must be no bulk capacitors connected directly to the early power pins.
4. The total capacitance of each early power plane must not exceed 8.8 μF for 5V, 3.3V and V(I/O) supply voltages, and 1.5 μF for +12V and -12V supply voltages.
5. Unused power pins and power pins that do not otherwise connect directly to low impedance power planes must provide an efficient AC current return path.
   a. The decoupling must average 0.01 μF (high frequency ceramic) per power pin, but must not exceed 0.2 μF.
   b. The trace length from pin to capacitor pad must be no greater than 15.2 mm using a trace width of at least 0.5 mm.
   c. There is no limit to the number of pins that can share the same capacitor provided that the first two requirements are met.
6. It is recommended that only one of the early long power pins be used in order to minimize the possibility of sneak current paths that might exist between early power potentials, signals, etc. in the absence of a stable ground.

4.1.2 Power Isolation

1. The board must provide isolation between the backplane power and the board's Back End load. Only the circuitry that must use Early Power is excluded from this requirement.
2. The power isolation circuitry provides a controlled turn on/off. During turn on/off, the maximum rate of change of current on the +5V and +3.3V supplies must be limited to 1.5A/ms. The ±12V supplies must be limited to 0.15A/ms.

4.1.3 Current Usage

1. The maximum DC current drawn by a board should be limited to 1A per pin. The current must not exceed the limits shown in IEC 1076-4-101 current derating curves for the 2mm connectors.
2. The +3.3V should be limited to 10A and the +5V should be limited to 8A. They should be limited to 8A and 6A respectively if the long Early Power pins are separate from the main supplies or resistively limited.

4.2 CT Bus Signal Conditioning

During insertion, extraction or /CT_RESET (or RST#[1]), the following must be true:

1. All data lines must be set as tri-state outputs (CT_D[0:31])
2. All clock lines must be set as inputs with the shorting device in the open position. (CT_C8, CT_FRAME)
3. All outputs must be set as tri-state outputs. (CT_NETREF)
4. Precharge levels must be established. The board's precharge bias voltage source must be capable of charging the onboard network to 80% of the precharge voltage within 5 microseconds.
5. CT_MC must be disabled.

These conditions must be met within 1ms after the application of early power (long pins making contact) on insertion and within 1ms after the de-assertion of /CT_EN or BD_SEL# (short pins breaking contact) on extraction.

4.3 Terminations

This section discusses the necessary terminations on the CT data lines, CT (CT_NETREF) network reference lines, CT_8M and frame pulse clocks and the CT enable line.

4.3.1 CT Bus Data Lines and CT_NETREF

1. All CT Bus data lines and CT_NETREF must provide 24 Ω series termination.
2. This termination resistor should be as close as possible to the connector.
3. These signals must be connected to an 18 KΩ (minimum) precharge resistor connected to 0.7V typically.
4. The point between the 24 Ω resistor and the backplane must be between 0.52V and 0.88V.

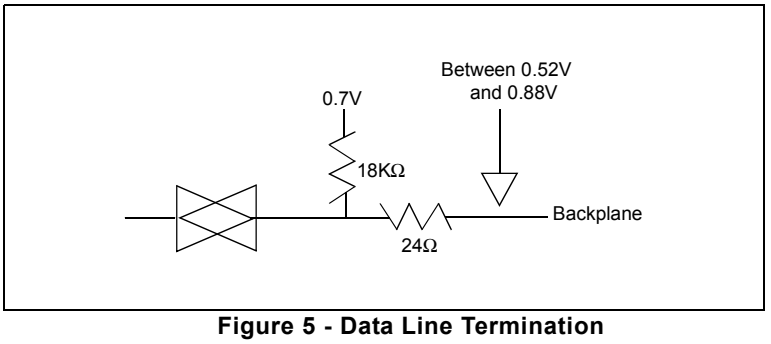

Figure 5 - Data Line Termination

4.3.2 CT_C8 and /CT_FRAME

1. The signals CT_C8 and /CT_FRAME must have termination consisting of a 100 Ω / 100 pF AC termination network at the physical ends of the backplane.
2. A 33 Ω series resistor must appear on these lines on each card, and should be as close as possible to the connector.
3. When the card becomes a CT Bus clock master, this resistor must be shorted out. The switch that shorts out this resistor must follow the requirements in table 4-3 in the ECTF H.110 specification.
4. These signals must be connected to a 10 KΩ resistor to ground.
5. The voltage at point A in Figure 6 must be between 0 and 0.5V prior to connection with the CT Bus on the backplane.

1. See reset requirements, section 4.4.

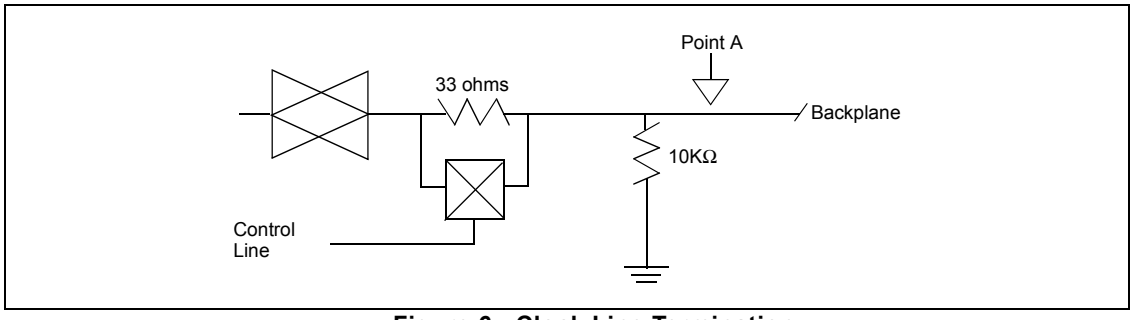

Figure 6 - Clock Line Termination

4.3.3 /CT_EN

/CT_EN must be connected to logic high (de-asserted) through a 1.2KΩ resistor or current source equivalent.

4.4 Reset Requirements

1. If the CT Bus card populates only J4, the card must respond to /CT_RESET signal when it is asserted.
2. If the card populates both J1 and J4 then /CT_RESET is ignored, and the J1 RST# line must be responded to.
3. If both J1 and J4 are populated, the card may repeat the RST# signal on /CT_RESET if so desired.

5.0 Block Design Overview

This section provides an overview of a possible design around Zarlink devices in order to satisfy the various hotswap requirements. Two potential solutions are given for the hotswap power controller and two solutions are given to provide the necessary buffering on the clock and data lines during card insertion/extraction.

5.1 Internal Buffers

Note: Not all Zarlink devices support the internal buffering solution. Please consult your FAE to confirm if the device you are using supports this solution.

In this design, the device is primarily driven from Early Power. This is done so that the device can tristate the data and control lines from the backplane.

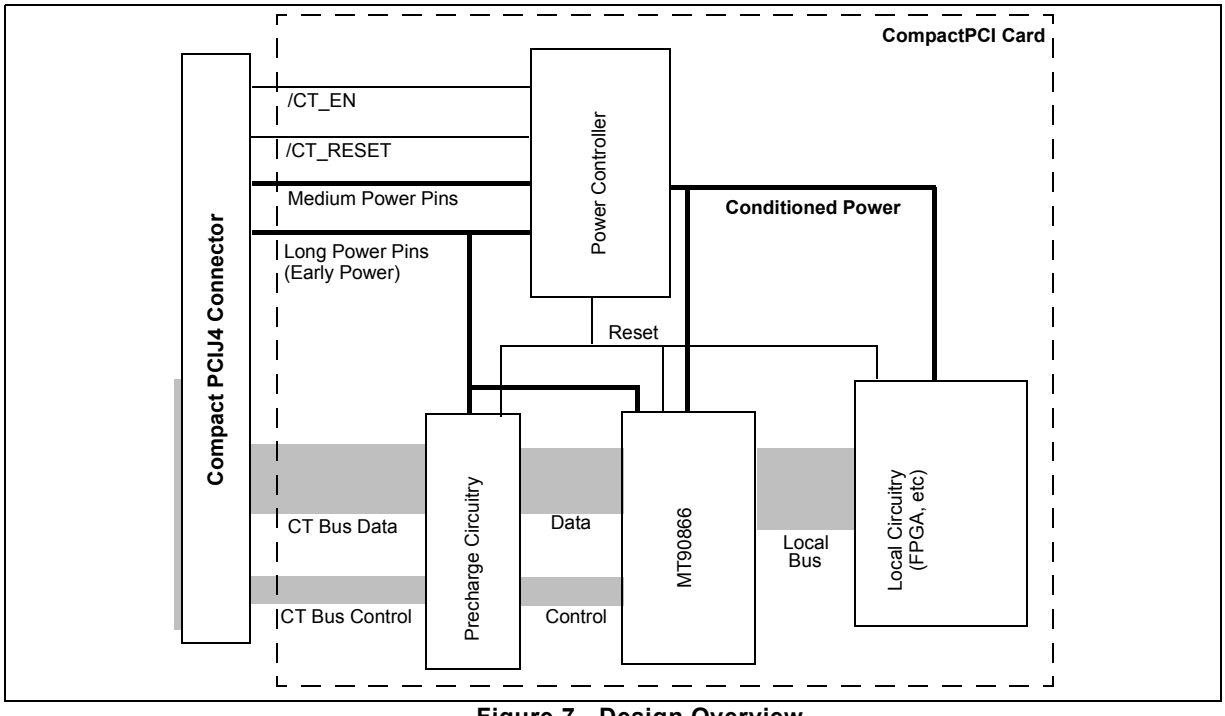

Figure 7 - Design Overview

5.1.1 Description of System Blocks

Power Controller: This block controls the power sequencing of the card. It monitors the power lines and shuts down the card in the event that the power becomes unstable or the card begins to draw too much current.

Precharge Circuitry: This block terminates the CT Bus signals as required by the hotswap specification. These requirements are described in the Termination section of the hotswap specs on the previous pages.

MT90866: The MT90866 tristates the bus during card insertion and extraction in order to avoid disturbing the CT Bus signals. After insertion, it provides the H.110 interface to the CompactPCI bus.

Local Circuitry: Contains the main circuitry other than that needed to achieve hot swap. This includes other switches, FPGAs or any other circuitry that is needed to provide the primary functionality of the card.

5.1.2 Implementation of System Blocks

This section describes the system implementation in more detail.

5.1.2.1 Power Controller

There are many ways to design the power controller on a CompactPCI card. Zarlink recommends using a dedicated power controller chip, such as the SMH4042 or LTC1643L. These parts have the advantage of monitoring the condition of the incoming power lines, and will electrically disconnect the card when the power is considered unsatisfactory.

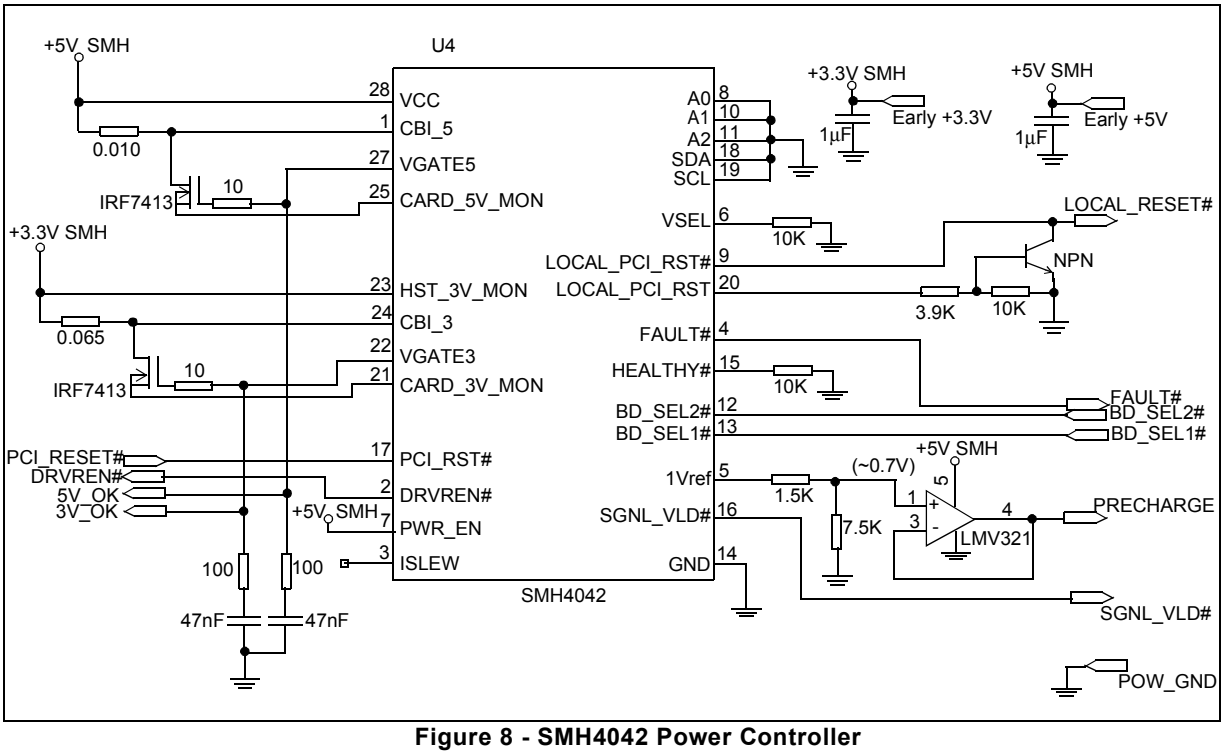

Figure 8 - SMH4042 Power Controller

The SMH4042 provides a 1 volt output (1Vref) which is used for the precharge voltage. A voltage divider is used to drop the voltage to within the specified CompactPCI range (0.52 to 0.88 V). This voltage is then buffered through a LM321 to prevent loading of the SMH4042.

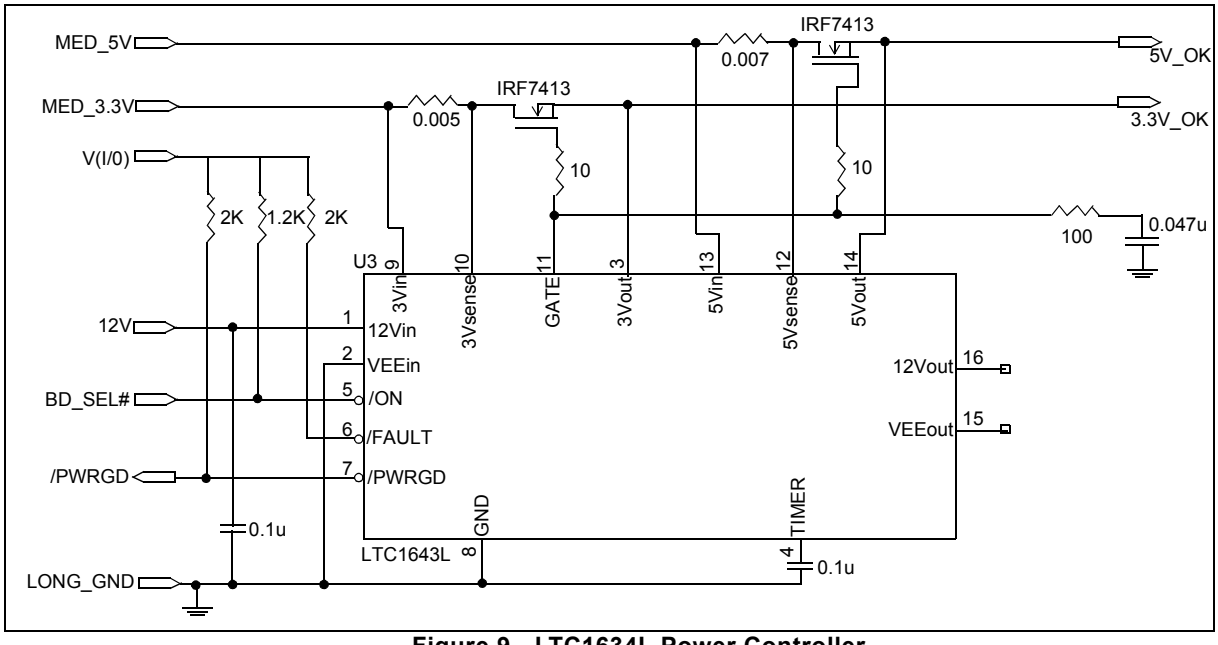

Figure 9 - LTC1634L Power Controller

The LTC1634L is similar to the SMH4042, except that it does not provide a precharge voltage or a reset signal. A sample precharge circuit which can be used with the LTC1634L, is shown in Figure 11. The reset signal can be provided through logic as in Figure 10.

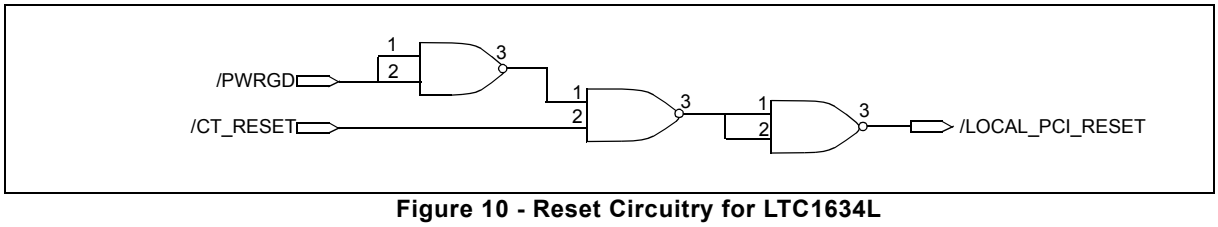

Figure 10 - Reset Circuitry for LTC1634L

Both the SMH4042 and LTC 1643L use IRF7413 FETs to monitor the incoming voltage condition. If the voltage condition is deemed unsatisfactory, both parts will turn off the FETs, effectively powering down any circuitry on the card that uses the medium power pins. The SMH4042 will also assert a reset signal, which is used to tristate the bus signals. The LTC1643L provides a /PWRGD signal which can be used to reset and tristate the card, as shown in Figure 10.

5.1.2.2 Precharge Circuitry

The precharge circuitry primarily consists of each CT-Bus data line running through a 24Ω resistor and being pulled up through a 18kΩ resistor, as shown in Figure 5. The precharge voltage is either generated by the power controller chip as in the SMH4042 case, or can be designed using external components as shown in Figure 11.

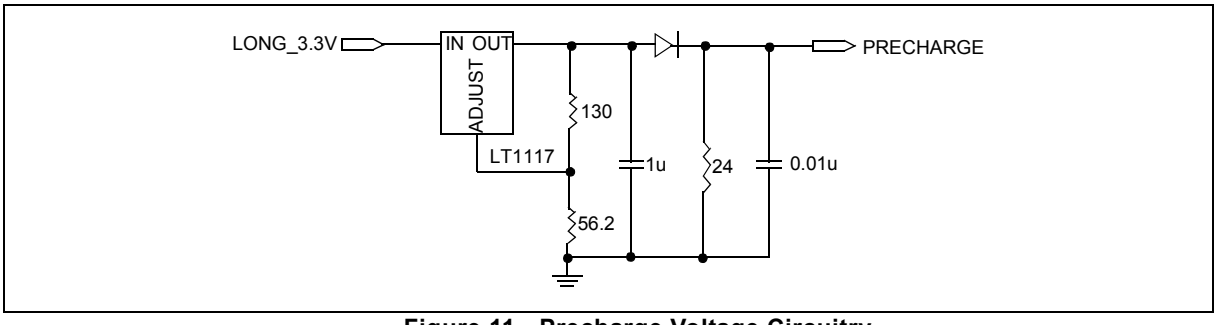

Figure 11 - Precharge Voltage Circuitry

If the CompactPCI card acts as both a master and a slave, the CT_C8 and /CT_FRAME signals must be handled in a special manner, as detailed in Section 4.3.2 of this technical note. A sample circuit which achieves this can be seen in Figure 12. If the card is designed to be either a slave or a master and never change between the two, the switch shown in Figure 12 can be eliminated. This switch can be controlled by the A_Active/B_Active pins of the MT90866.

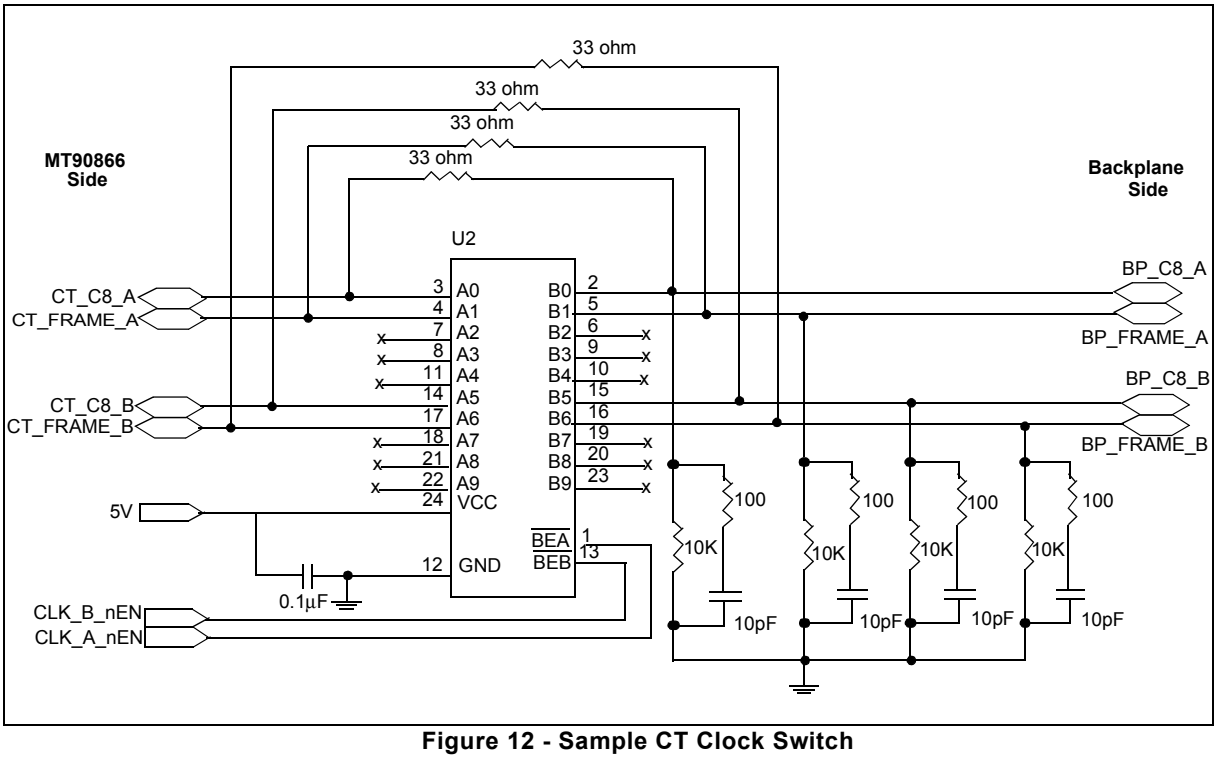

Figure 12 - Sample CT Clock Switch

5.1.2.3 MT90866

Either the /PCI_OE or /RESET pin on the MT90866 can be used to tristate the STio bus during insertion/extraction. The /PCI_OE pin only tristates the backplane STio0-31 pins, whereas the /RESET pin tristates and holds the MT90866 in reset. Typically, this reset line is asserted by the power controller on the board. The power controller monitors the incoming power conditions and combines this condition with the /CT_EN, /CT_RESET and RST# backplane signals to provide the reset signal to the MT90866. The ODE pin can be used to tristate both the local and backplane interfaces during insertion/extraction if required.

The CT_Bus backplane signals are connected to the equivalent lines (STio, etc…) on the MT90866.

5.1.2.4 Local Circuitry

The local circuitry will be implemented based on the design requirements. It does not need to consider the hotswap portion of the board. The local circuitry should be powered by the medium power lines, which are controlled by the power controller on the board. The local circuitry also needs to meet the requirements of the reset line that the power controller exerts during an insertion, extraction or bad power conditions.

5.2 External Buffers

In this design, the device is powered from conditioned power (medium pins) rather than Early power. The external buffer takes care of tri-stating the H.110 bus lines, rather than the H.110 device. This avoids powering up the device with early power, but has the disadvantage of extra components.

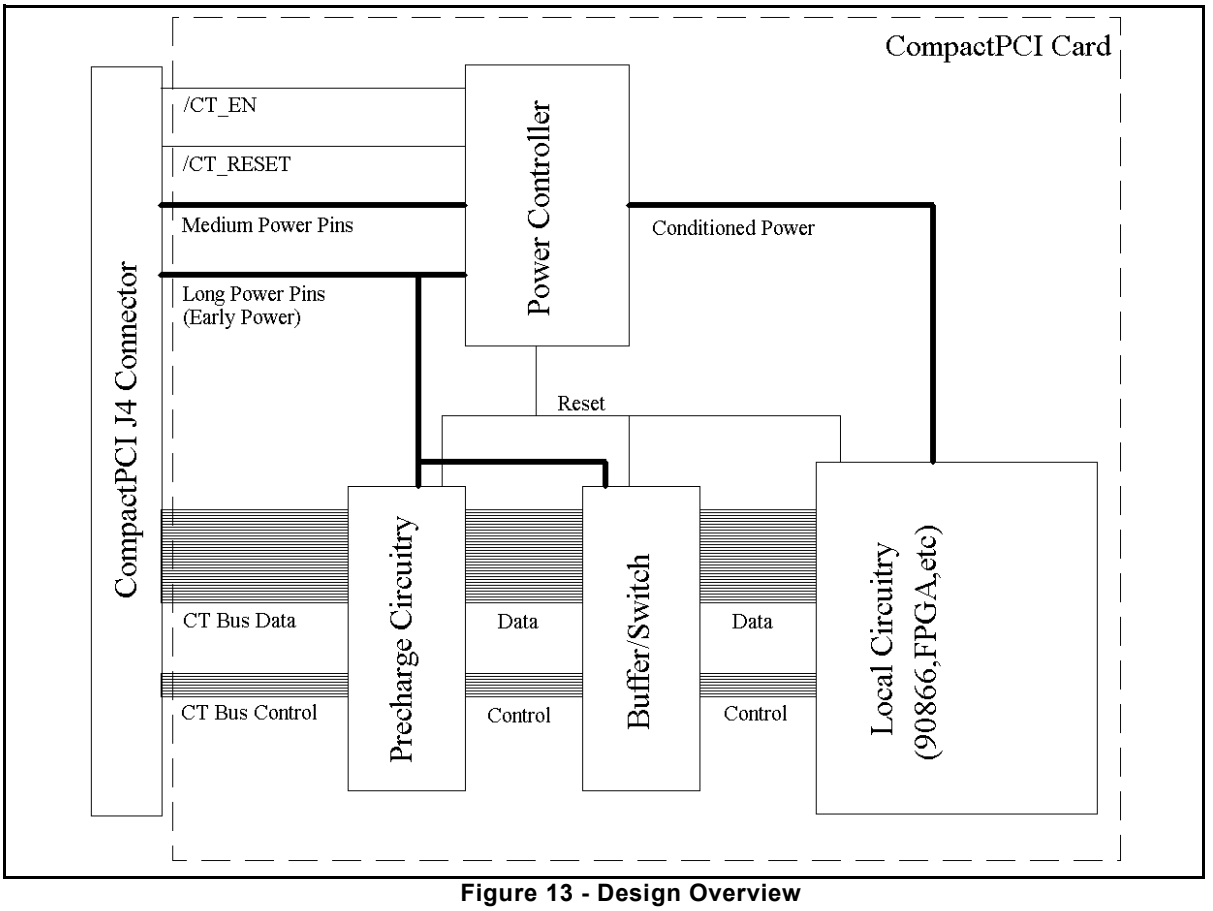

Figure 13 - Design Overview

5.2.1 Description of System Blocks

Power Controller: This block controls the powering up and down of the card. It monitors the power lines and shuts down the card in the event that the power becomes unstable or the card begins to draw too much current.

Precharge Circuitry: This block terminates the CT Bus signals as required by the hotswap spec. These requirements are described in the Termination section of the hotswap specs on the previous pages.

Buffer/Switch: This block takes care of tri-stating the bus when an insertion or extraction is in process. It achieves this using bus switches, such as the IDTQS34XVH245 or similar parts.

Local Circuitry: Contains the main circuitry other than that needed to achieve HotSwap. This includes the Zarlink H.110 compatible device, FPGAs or any other circuitry that is need to provide the primary functionality of the card.

5.2.2 Implementation of System Blocks

This design is very similar to the previous design shown in section 5.1, with the exception that a tri-stating switch/buffer is now placed between the backplane and the Zarlink device.

5.2.2.1 Power Controller

The power controller can be designed in the same manner as the non-buffer design presented in section 5.1.2.1.

5.2.2.2 Precharge Circuitry

The precharge circuitry can be designed in the same manner as the non-buffer design presented in section 5.1.2.2.

5.2.2.3 Buffer/Switch

The buffer sections consists of bus switches, such as the QS3VH245 or the QS34XVH245, which are used to tristate H.110 bus data signals during insertion and extraction. Figure y shows a QSVH245 along with precharge circuitry being used to buffer the first 8 H.110 data lines.

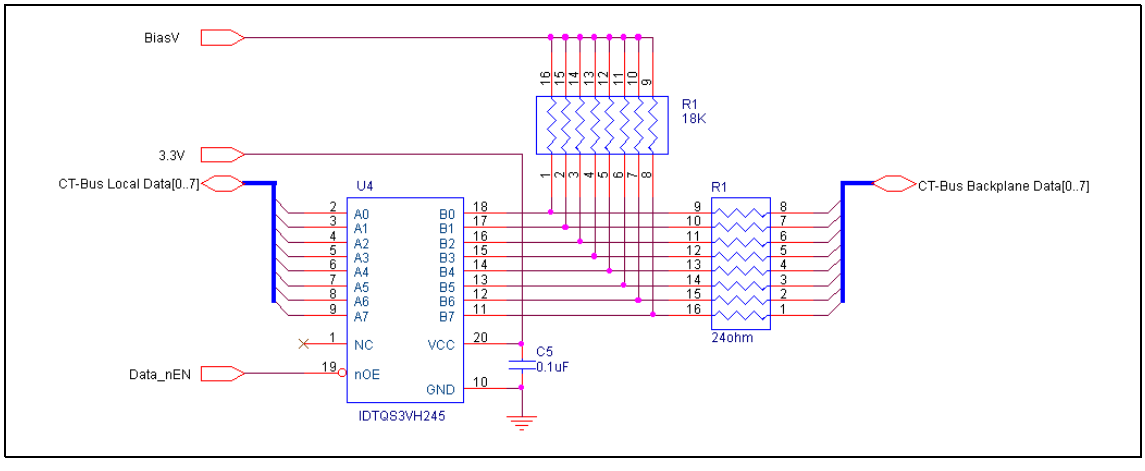

Figure 14 - Sample Switch/Buffer Design with Precharge

The CT_C8 and /CT_FRAME signals must be dealt with in the same manner as in section 5.1.2.2.

5.2.2.4 Zarlink Device/Local Circuitry

The Zarlink Device/local circuitry will be implemented in whatever manner is needed to fulfill your design. It does not need to concern itself with the hotswap portion of the board. The local circuitry should be powered by the medium power lines, which are controlled by the power controller on the board. The local circuitry also needs to obey the reset line that the power controller exerts during an insertion, extraction or bad power conditions.

6.0 Conclusions

Hotswap in an emerging technology, and will become more important in the future. The ability to add and remove components from a live system in order to reduce system downtime is essential to a high availability telecom system. Shutting down and powering off a system prior to the insertion, removal or replacement of system boards causes unacceptable levels of inaccessibility. Systems with hot-swap capabilities range in the ability to reduce this downtime from hours of system unavailability to mere minutes. As the uptime of a system increases, so does the complexity of the hardware and software of that system.

A hotswap compliant design is not an easy task as there are many factors that must considered. The Zarlink MT90866 simplifies the design by providing the ability to tristate the CT-Bus lines while an insertion or extraction is taking place, as well as providing H.110 compliant signaling.

7.0 Hot Swap Terminology

Early Power: Power supplied by the long pins of the CompactPCI connector. This power is potentially unstable, and should only be used to power the components absolutely necessary to facilitate the hotswap process.

Precharge: A means to bias the capacitance of a load to a nominal potential, prior to its connection with an active circuit.

Quiesced: No operations are in progress or pending, and there is no authorization to launch new operations.

V(I/O): Power pins labeled +V(I/O) provide power for Universal boards utilizing I/O buffers driving backplane signals that MAY operate from +5V or +3.3V. On these boards, the PCI components I/O buffers SHALL be powered from V(I/O), not from +5V or +3.3V power pins. Backplane pins labeled V(I/O) are connected to +5V on 5V keyed systems and +3.3V on 3.3V keyed systems. Alternatively, a separate V(I/O) power plane may be provided to supply 5V or 3.3V power.

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