Performing Subrate Switching Through Oversampling

Application Note

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April 2003

1.0 Introduction

There are three forms of fractional channel switching. Each is useful for a particular type of application. When a switching device does not have the integrated feature for performing the fractional switching function, it can be accomplished through oversampling. Below are some applications of where subrate switching is useful.

Bit switching (1 bit per channel) is useful in wireless communication applications. In these applications, voice needs to be compressed from 8 bits/channel to 1 bit/channel.

Dibit switching (2 bits per channel) is essential to the operation of adjunct ISDN equipment that is used to terminate ISDN lines at (CO) Central Offices where D-channel processing capability is non-existent. The 16kb/s D-channels are collected and packed into a T1/T3 or E1/E3 transmission facility and sent to a CO capable of processing the D-channel data.

Nibble switching (4 bits per channel) is used in digital wireless communications and pair gain systems where 8-bit (64kb/s) PCM (Pulse Code Modulation) data is compressed into 4-bit (32kb/s) ADPCM (Adaptive Differential Pulse Code Modulation) data.

There are no specific registers that need to be set in order to perform subrate switching, unless the device in question has subrate swithing as an integrated feature (in which case the data sheet for the specific part should be consulted).

This application note illustrates the use of Zarlink switches as fractional switching devices through the use of oversampling.

2.0 Switching Configuration

Zarlink devices switch 8-bit (64kb/s) channels at ST-BUS data rates ranging from 2.048Mb/s to 65.536Mb/s, depending on the particular device being used. In fractional bit switching applications, the device's internal clock rate must be increased while a lower data rate is maintained on the serial streams. The following sections show how to configure Zarlink switches in such applications.

The data rate that the device is operating at will determine the maximum number of channels in a 125µs frame, assuming there are no memory limitations in the device. Each channel is comprised of 8 bits of information.

Data Rate	Channels per Stream
2.048Mb/s	32
4.096Mb/s	64
8.192Mb/s	128
16.384Mb/s	256
32.768Mb/s	512
65.536Mb/s	1024

Table 1 - Maximum Channels Available

Note: Memory size defines the maximum number of channels supported by the device, regardless of whether channels are 8 bits, 4 bits, 2 bits or 1 bit wide.

Figure 1: Channel Mapping and Timing shows typical frame pulse and clock inputs, as well as the timing for normal operation with 8 bit channels. In following the ST-BUS standard, a 2x clock is used for traffic at 2.048 to 8.192Mb/s and a 1x times clock is used for 16.384Mb/s and higher data rates. The frame pulse associated with the clock will be a 8kHz signal with varying widths. As the clock rate increases, the frame pulse width will decrease approprately.

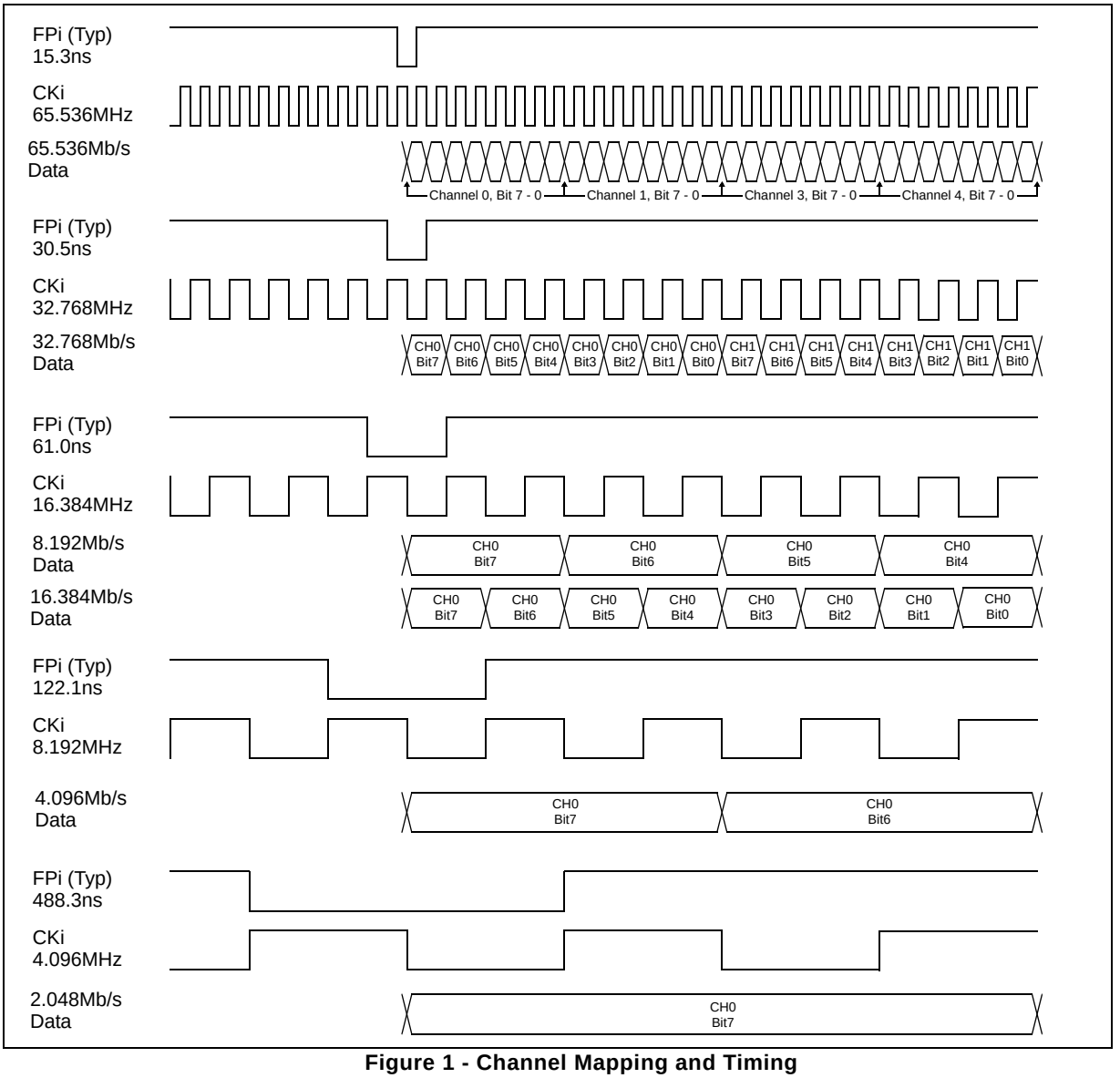

Figure 1 - Channel Mapping and Timing

2.1 Nibble Switching

For an example of nibble switching, a Zarlink switch is set to run in the 4.096Mb/s mode while the external ST-BUS streams are maintained at 2.048Mb/s. The device over-samples the input stream by a factor of two (requiring an input clock of 8.192MHz and frame pulse with a width of 122ns outlined in the ST-BUS standard). Each bit of the 2.048Mb/s data stream is stored in two consecutive bit locations. Thus one nibble is stored in one eight bit memory location (each two bits in the memory contain nibble bit). In this configuration the switch will output one bit in two consecutive bit cells (two bit cells at 4.096Mb/s = one bit cell at 2.048Mb/s).

2.2 Dibit Switching

In dibit switching, Zarlink switches are configured to operate at four times the input data rate. For example, the external ST-BUS streams are maintained at 2.048Mb/s, but they are sampled as though they were running at 8.192Mb/s (using a 16.384MHz clock and 61ns wide frame pulse as specified in the ST-BUS standard). Each bit of the 2.048Mb/s input data stream is stored in four consecutive bit locations. Thus each dibit is stored in a single memory location, with one dibit in the first four bits of memory and the other dibit in the second four of memory. In this configuration the switch will output one bit in four consecutive bit cells. (Four bit cells at 8.192Mb/s = one bit cell at 2.048Mb/s.)

2.3 Bit Switching

When bit switching applications are being implemented, data must be sampled at 8 times the input data rate. For example, to perform bit switching at 2.048Mb/s, the input data must be sampled at 8 times that rate, or 16.384Mb/s (using a 16.384MHz clock and 61ns frame pulse according to the ST-BUS standard). The device will store the sampled data in eight consecutive bit locations, or in other words, it will use an entire channel location to store one bit of information. (Eight bit cells at 16.384MB/s = one bit cell at 2.048Mb/s.)

Figure 2: Input Sampling, shows how a higher input clock can be used while the data is input at a lower rate to provide the functionality of subrate switching. This figure also shows the typical sampling points based on the input timing.

Table 2: Input Data Memory Contents When Input Stream Configured for 65.536Mb/s Operation shows how the sampled data is stored in the data memory for the particular device.

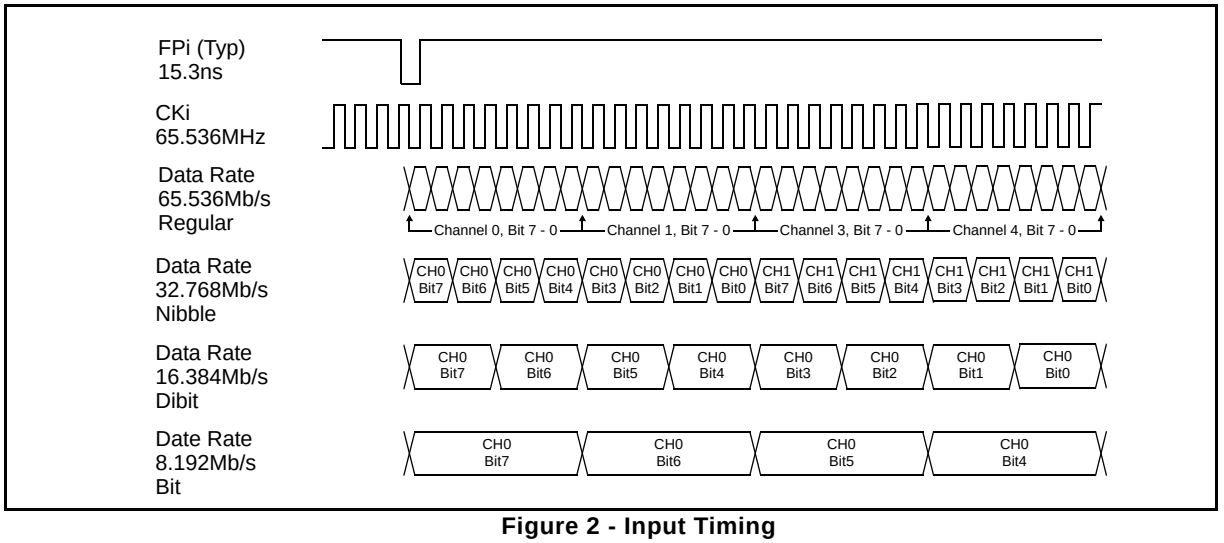

Figure 2 - Input Timing

ONE 8 BIT DATA MEMORY LOCATION								
	Channel 0							
Date Rate	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
65.536Mb/s Regular	Ch0 B7	Ch0 B6	Ch0 B5	Ch0 B4	Ch0 B3	Ch0 B2	Ch0 B1	Ch0 B0
32.768Mb/s Nibble	Ch0 B7	Ch0 B7	Ch0 B6	Ch0 B6	Ch0 B5	Ch0 B5	Ch0 B4	Ch0 B4
16.384Mb/s Dibit	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B6	Ch0 B6	Ch0 B6	Ch0 B6
8.192Mb/s Bit	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7	Ch0 B7

Table 2 - Input Data Memory Contents When Input Stream Configured for 65.536Mb/s Operation

3.0 Typical Examples

Table 3: Input Data Sampling Subrate Possibilities demonstrates what type of subrate switching is possible at various input clock rates. For example, if the input stream is configured for 8.192Mb/s operation, it is possible to perform nibble switching at 4.096Mb/s and dibit switching at 2.048Mb/s. It is not possible to perform bit switching, as bit switching requires an 8x clock.

Figure 3: Examples of Subrate Switching Configuration shows an example of how you can divide up a channel into channel, nibble, dibit and bit switching configurations and then how you could switch the data into another channel.

Data Rate	Nibble Switching	Dibit Switching	Bit Switching
2.048Mb/s	Not Applicable	Not Applicable	Not Applicable
4.096Mb/s	2.048Mb/s	Not Applicable	Not Applicable
8.192Mb/s	4.096Mb/s	2.048Mb/s	Not Applicable
16.384Mb/s	8.192Mb/s	4.096Mb/s	2.048Mb/s
32.768Mb/s	16.384Mb/s	8.192Mb/s	4.096Mb/s
65.536Mb/s	32.768Mb/s	16.384Mb/s	8.192Mb/s

Table 3 - Input Data Sampling Subrate Possibilities

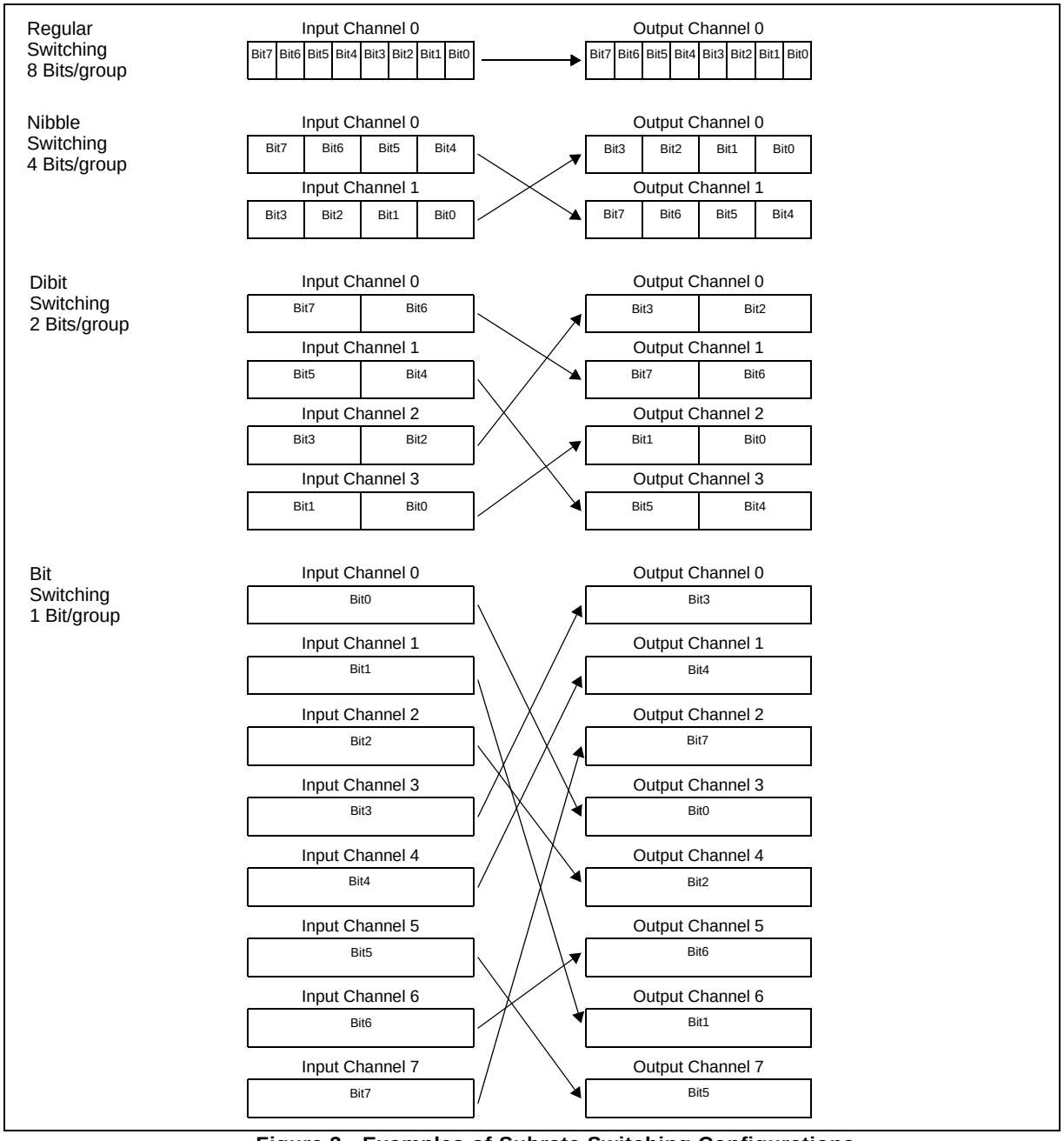

Figure 3 - Examples of Subrate Switching Configurations

4.0 Conclusion

In this application note we have illustrated how to use Zarlink TDM switching devices in subrate switching applications through the use of oversampling. For more information, please consult the specific Zarlink data sheet, or contact your Zarlink Semiconductor representative. On the internet reach us at www.zarlink.com and questions can be sent directly to technicalhelp@zarlink.com

For more information about all Zarlink products
visit our Web Site at

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