Application Note **MSAN-172**

Automated Measurement of Cable Delay using the MT9173/74

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1.0 Introduction

As the demand for Mobile Personal Communication grows, the capacity of the existing analog systems is becoming inadequate. This has prompted development of multiplexing techniques such as Time Division Multiple Access (TDMA) which utilize available bandwidths more efficiently. The TDMA type air interface requires frame synchronization between the phone and the Base Station. When the phone is mobile, frame synchronization between adjacent Base Stations must be closely aligned to ensure that during handovers the calls are not dropped and that the transition is noise free. For example, if a mobile phone roams through the coverage area of base stations 1, 2, & 3 (see Figure 1), the delay caused by the different loop lengths between the Base Station Controller (BSC) and base stations may cause the mobile phone to lose synchronization.

This application note illustrates how to continuously measure the loop delay and use this information to

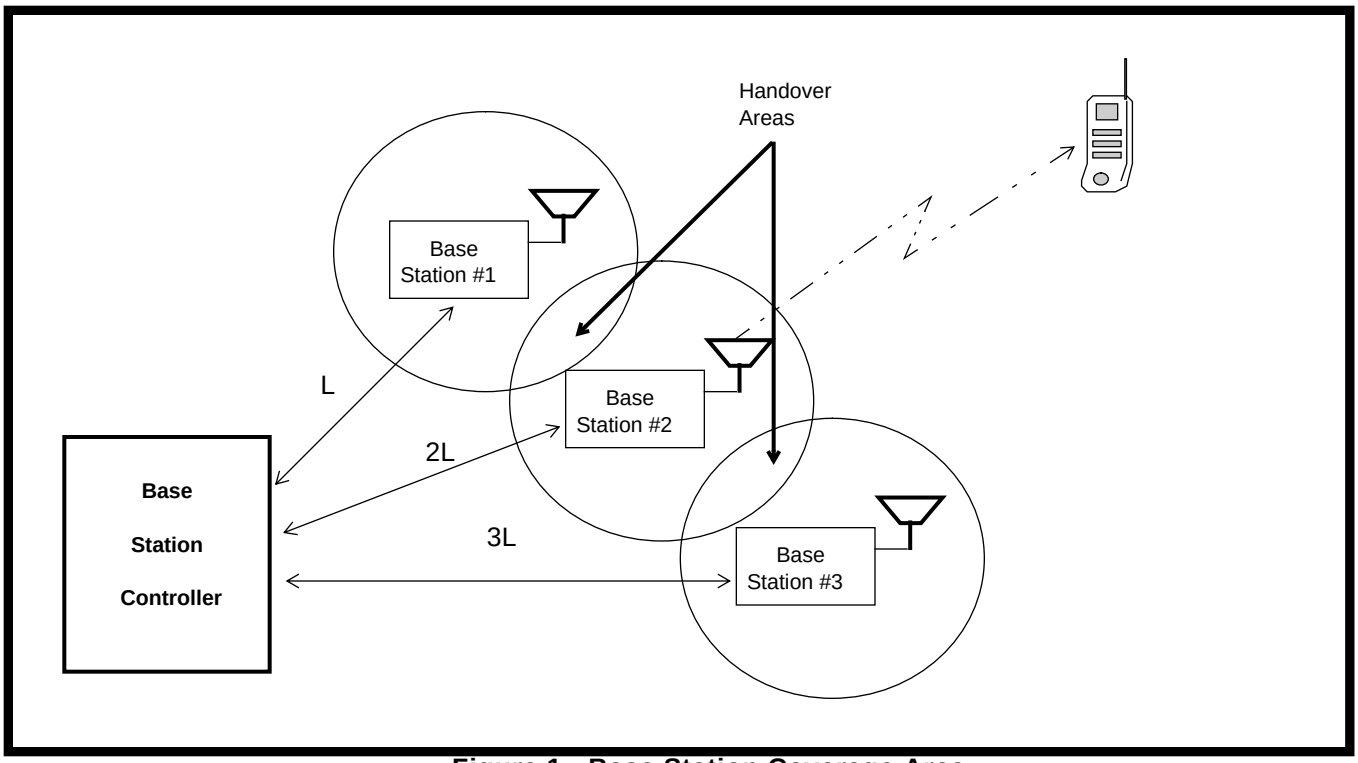

Figure 1 - Base Station Coverage Area

automatically adjust frame alignment between the BSC and all Base Stations.

2.0 Methods of Determining Loop Delay

Aligning TDM frames requires measuring the delays between the base stations and the BSC. Once these delays have been determined, they can be used to program a compensation circuit inside the BSC to equalize the delay in all the loops (add delay to the shorter loops to match the delay of the longest loop). There are three methods to determine the loop delay between the base station and the BSC.

2.1 Calculation Method

The signal delay between the base station and the BSC can be calculated given the length of the cable and the propagation delay (approximately 7μs/Km). Since the length of the cable between the base station and the BSC may be a gross approximation, this method does not yield reliable results.

2.2 Time Domain Reflectometer (TDR) Method

Another method of determining loop delay is to use a TDR. A TDR transmits a pulse down the line and measures the time it takes for the reflected pulse to return. This return pulse may be low in amplitude due to the high attenuation of the twisted pair line. This limits the distances that can be measured. Another disadvantage of using a TDR is that the far end of the cable must be either opened or closed.

2.3 MT9174 Received Frame Position Method

Both the calculation and TDR methods require human involvement. This can be easily eliminated by using Zarlink's Digital Network Interface Circuit (MT9174). The MT9174 outputs a receive frame signal which permits measurement of the time difference between the transmit and receive frame positions, thereby determining the loop delay.

3.0 Loop Delay Measurement Using the MT9174

Features of the MT9174 are:

1. Access to the Receive frame boundary through the RxSB pin.
2. Synchronization status via the RxSB pin.
3. Full duplex transmission over a single twisted pair.
4. Selectable 80 or 160 Kbits/s line rate.
5. Adaptive echo cancellation.
6. Up to 4km loop reach.
7. ISDN compatible (2B+D) data format.
8. Transparent modem capability.
9. Built in frame synchronization and clock extraction.

All of these features are common to Zarlink DNIC devices except for the RxSB functionality which is found only in the MT9174. Access to the frame boundary position through the RxSB pin was incorporated specifically to perform loop delay measurements.

3.1 Frame Pulse Path Block Diagram

Figure 2 shows a block diagram indicating the frame pulse path through the system. A frame pulse is applied to the /F0 pin of the master MT9174 to indicate the start of a frame. This framing information is encoded onto the data and is transmitted to the slave MT9172.The slave extracts the timing information from the data stream and uses it for the slave system timing. This received timing is used to transmit data and frame boundary information back to the master MT9174. The master MT9174 extracts timing information from the received line and uses this to clock data into an elastic buffer. In addition the recovered frame pulse is output on the RxSB pin. The loop delay counter circuit measures the time between /F0 and RxSB. This value represents the total of all circuit and propagation delays in the communications link. This information is then read by the microprocessor and used to program the delay circuit in the BSC to compensate for the loop delay. The function of the loop delay timer is described in section 4.

3.2 Line Card Block Diagram

Figure 3 shows a block diagram of a line card application. Three MT9174s are used on the master side and the three RxSB bits are applied to the loop delay timer circuit. Under micro-processor control the delay between the selected RxSB and the local frame pulse is measured. This measurement must be taken after the MT9174s are in synchronization and the channel quality bits indicate a good data link.

3.3 Delay Circuit Description

This technical note does not cover the delay circuitry in detail, however, a short description will be given to complete the discussion.

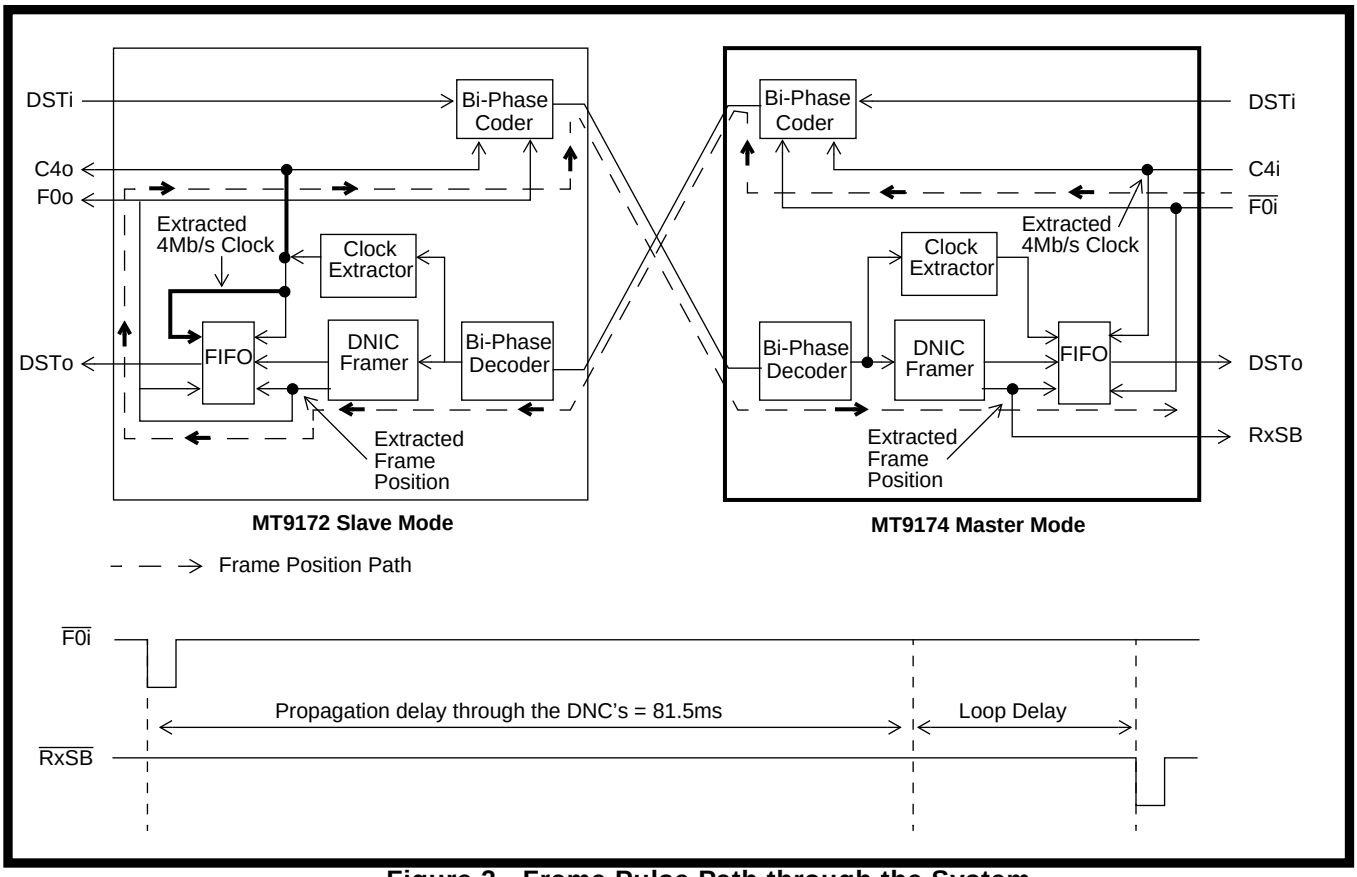

Figure 2 - Frame Pulse Path through the System

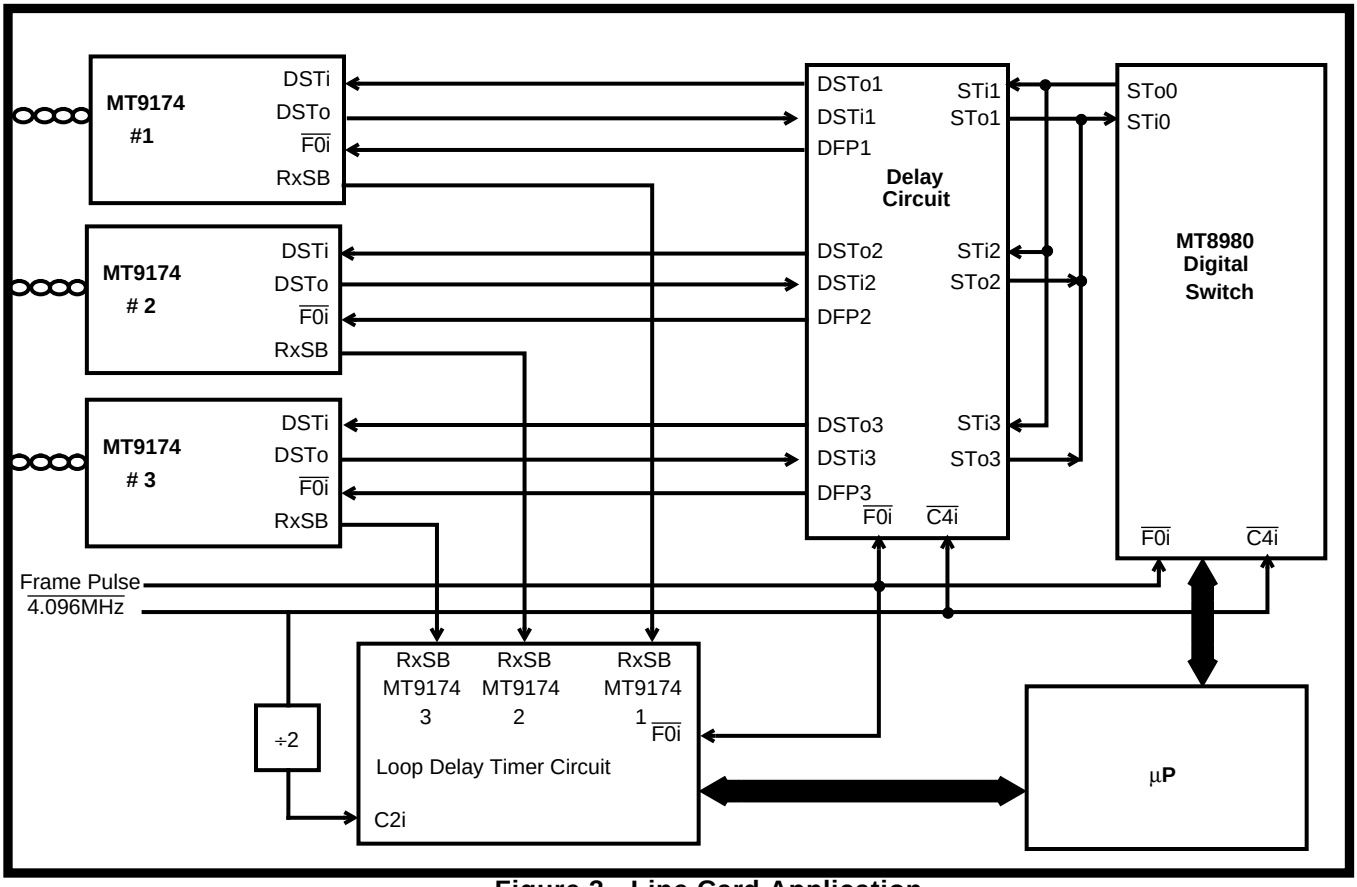

Figure 3 - Line Card Application

The delay circuit needs to delay the bit cell boundary by an integer multiple of the 2.048MHz clock period. In order to do this the delay circuit must contain a FIFO with at least one frame of memory. For a single basic rate link (2B+D) the delay circuit needs at least an 18 bit FIFO in each direction. Figure 4 shows a block diagram of a delay compensating circuit. The transmit section will delay the data by a specified amount (determined by the measured loop delay). The receive section will delay the received data by one frame period minus the transmit delay. This circuitry will maintain proper ST-Bus alignment on the system side even though the frame alignment on the base station side differs.

4.0 Loop Delay Measurement Circuit and Algorithm Description

The following section covers the conditions in which the loop delay must be measured.

4.1 Determining Channel Quality

Before measuring the loop delay, the MT9174 must be synchronized with the channel quality bits indicating medium high to high. To obtain an accurate channel quality measurement, it is recommended that the channel quality bits be averaged over several frames.

4.2 Functional Description of the Automatic Delay Measurement Circuit

The schematic diagram shown in Figure 6 is a circuit used to measure the loop delay of up to eight different MT9174 lines. The circuit uses two data multiplexers (74HC151) to select the MT9174 line to be measured. One 74HC151 selects the master frame pulse and the other selects the receive synchronization bit. The master frame pulse is used to load an 8 bit counter with a value that corresponds to the inherent delay through the MT9174s. This delay is specified in the data sheet as 81.4µs (at 160 Kb/s) (Figure 5). The value to be loaded into the counter can be calculated using the following equation:

$$LoadValue = MaximumCount - \left| \left(\frac{MT9174Delay}{CounterClockPeriod} \right) \right|$$

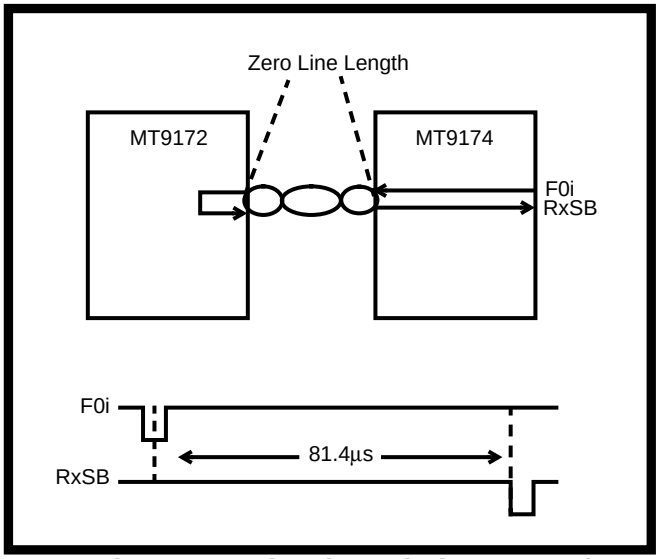

Figure 5 - Delay through the MT9172/74

For the circuit shown in Figure 6 which uses a 2.048 MHz clock, the load value would be 58h. Once this value is loaded by the frame pulse, the counter will count up through zero, effectively subtracting the inherent delay through the MT9174. The RxSB signal latches the count value into the 74HC574. This value represents the propagation delay of the

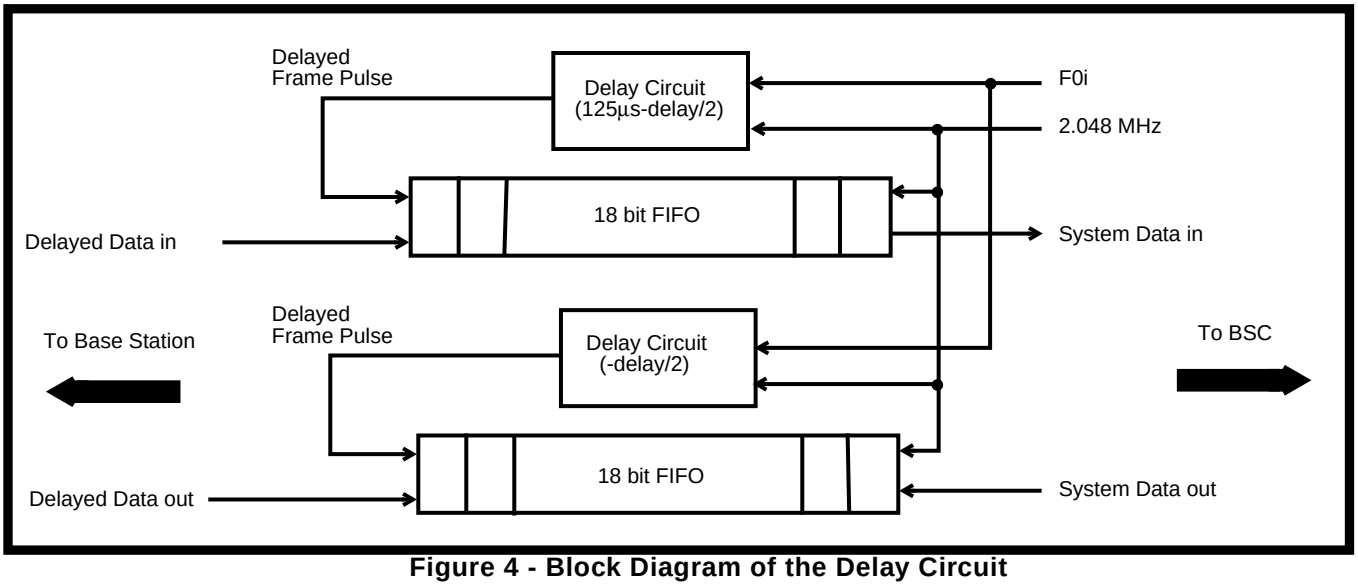

Figure 4 - Block Diagram of the Delay Circuit

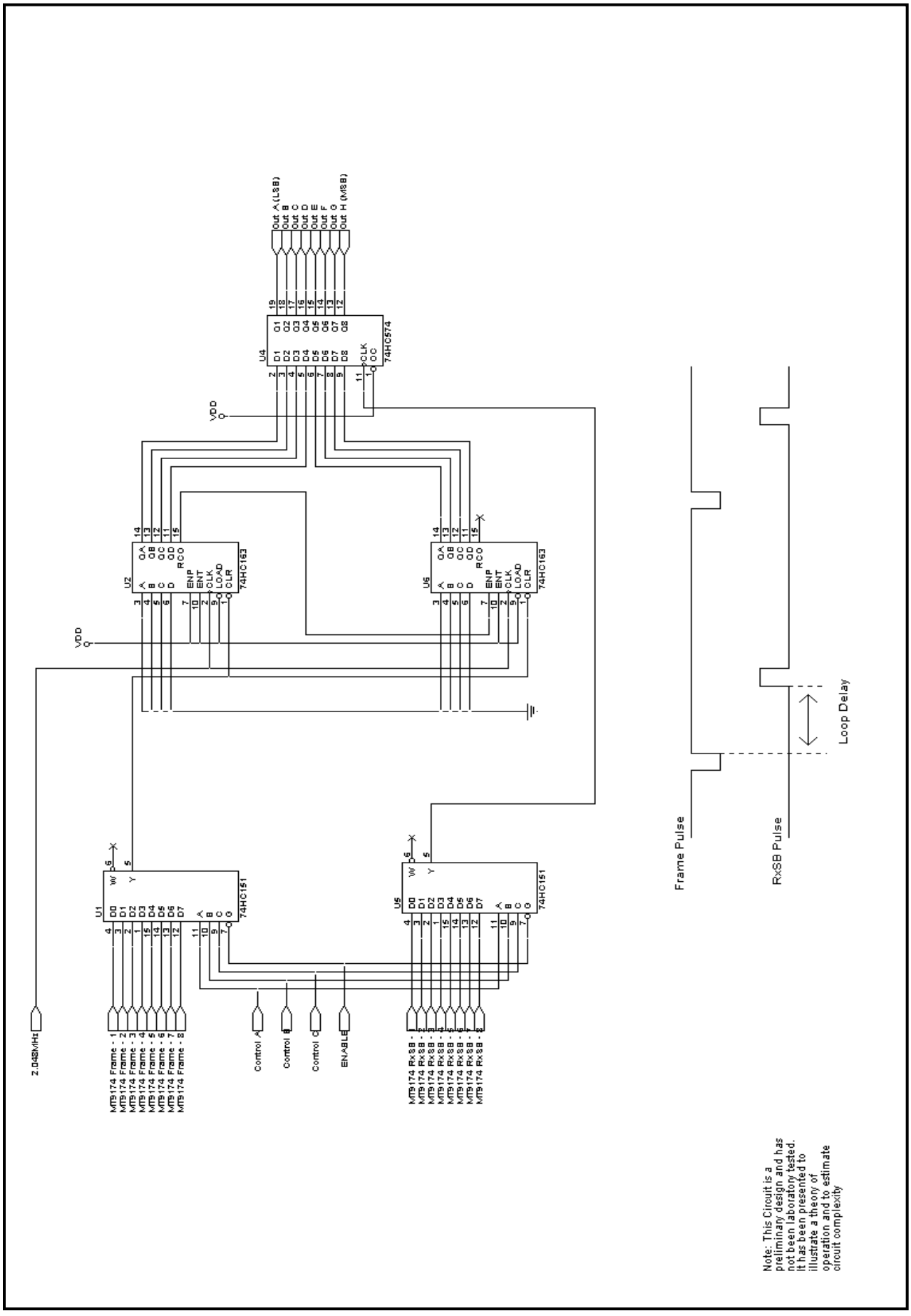

Figure 6 - Loop Delay Measurement Circuit

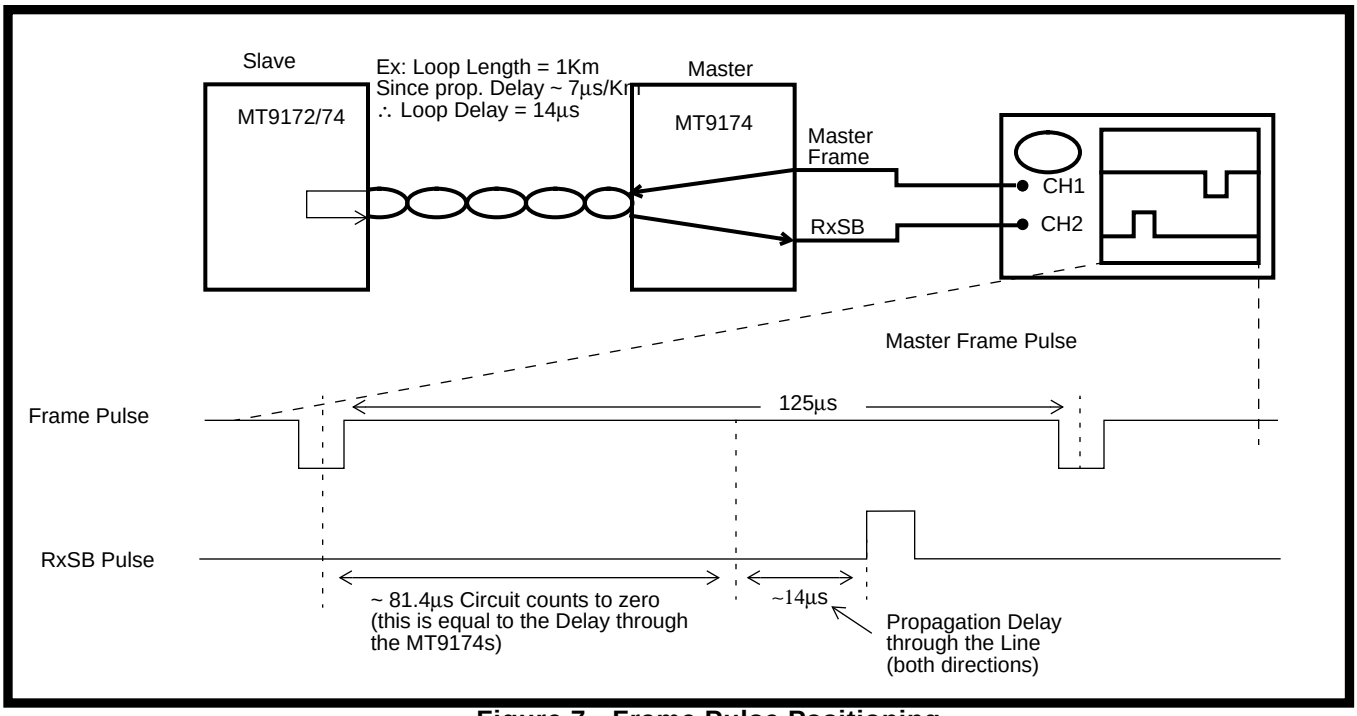

Figure 7 - Frame Pulse Positioning

transmission line and can be converted to seconds by using the following equation:

Delay Time = Count x Counter Clock Period

For example, if the value from the counters was 1Dh then the loop delay time would be 13.6µs or 6.8µs for one direction (approximately 1 km of propagation delay for twisted pair). Figure 7 shows the position of the RxSB pulse in relation to /F0.

4.3 Loop Delay Measurement Algorithm

The following description and flow chart (Figure 8) outlines a suggested algorithm for measuring the loop delay.

1. Clear all counters and loop delay memory.
2. Monitor bit 0 (Synchronization Bit) of the status register. If this bit is high then go to step 3. If this bit is zero, repeat step 2.
3. Read bits 1 and 2 (Channel Quality bits) of the status register. If the Channel quality bits are 01 (medium high) or 11 (high), increment a counter. If the counter equals 5 then go to step 4. If the counter is less than 5, wait one frame then repeat step 2.
4. Read value from the loop delay timer circuit. Store the value in memory and increment a counter. If the counter value is less than 5 then wait one frame and repeat step 4.
5. If the counter is equal to 5 then average all the loop delay values stored in memory together, subtract the inherent delay and divide by two.
6. Set up delay circuit.

5.0 Accuracy of the Measurements

The accuracy of the loop delay measurement is limited by the accuracy of the internal MT9174 RxSB circuitry and the resolution of the loop delay measurement circuit. The RxSB signal is accurate to within 250ns at 25°C and 5V. This accuracy worsens to 800ns over the full voltage and temperature range. The resolution of the loop delay measurement circuit is determined by the period of the clock. The resolution can be improved by increasing the clock frequency. Since the accuracy for the RxSB is (800ns (worst case) a clock period of 488ns (2.048MHz) is sufficient.

6.0 Conclusion

This method of determining the loop delay for digital base stations is superior to the existing methods of calculating the loop delay or measuring it using a TDR. Previous methods required a technician and can only be done on system installation. This makes it difficult to interchange line interface boards as each board needs to be individually adjusted. The automated solution, outlined here, eliminates manual adjustment and allows loop delay measurement to be performed at any time, even while the MT9174 link is in use.

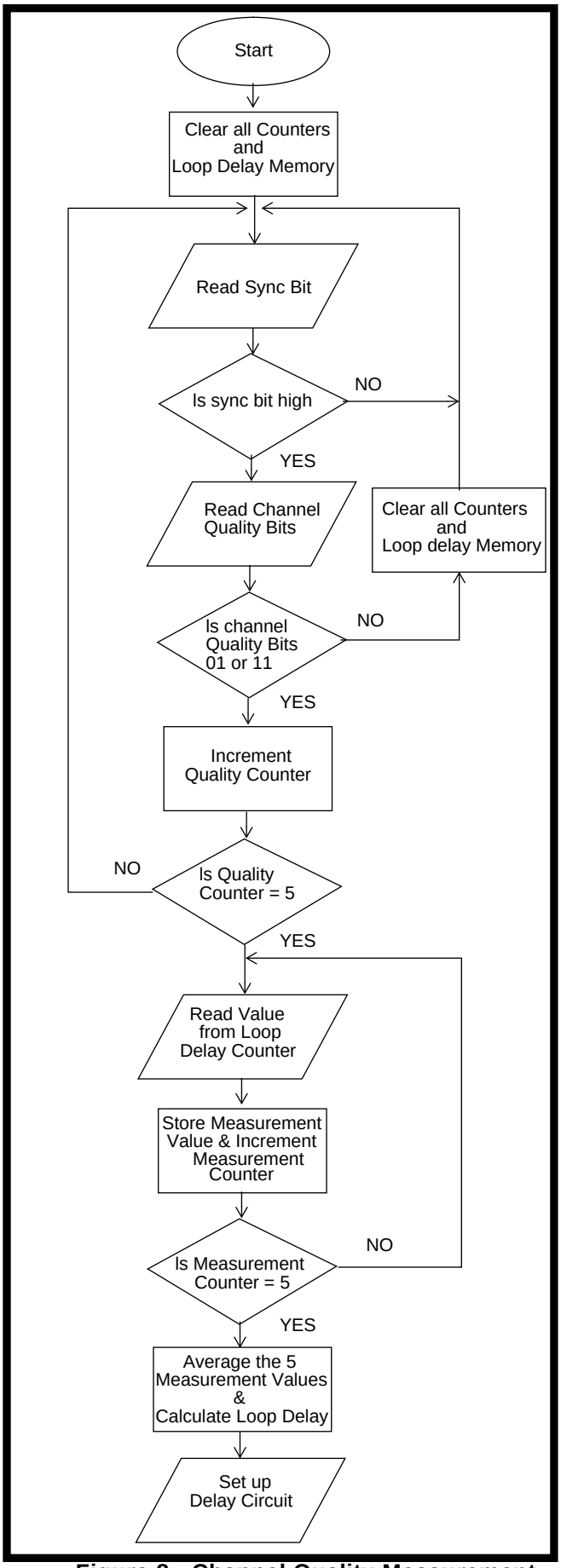

Figure 8 - Channel Quality Measurement Flowchart

Notes:

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