ZARLINK SEMICONDUCTOR

Application Note MSAN-131
Subscriber Line Interface for Digital Switching Systems

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Table of Contents

- **1.0 Introduction**
- **2.0 MT8960-67 Voice Codec General Application Information**
- **3.0 MT8960-67 Functional Description and Application Details**
  - 3.1 Channel Timeslot Assignment
  - 3.2 Switching and Control Using the MT8980 Digital Crosspoint Switch
- **4.0 Subscriber Line Interface Circuit Applications**
- **5.0 MH88610 Application Details**
  - 5.1 Battery Feed
  - 5.2 Off-Hook Detection and Dial Pulse Signalling
  - 5.3 Application of Ringing and Automatic Ring Trip Implementation
  - 5.4 Transmit and Receive Signal Levels
- **6.0 Consideration of Loss and Level Plans in SLIC Design**
- **7.0 Line Card Power Supply Filtering and Codec Circuit Protection**
- **8.0 Line Card Layout Guidelines**
- **9.0 Conclusions**
- **10.0 References**

1.0 Introduction

In digital telephone switching systems, the two wire analog loops interface to the switch through a Subscriber Line Interface Circuit (SLIC). The basic functions of the SLIC are frequently summarized using the acronym BORSCHT - which stands for Battery, Overvoltage, Ringing, Signalling, Coding, Hybrid and Test. Zarlink's MH88610 Subscriber Line Interface Circuit (SLIC) and the MT8960-67 series of Voice Codecs can be used together to implement these functions.

The MT8960-67 series of Voice Codecs integrate all the functionality necessary to encode analog signals in the voice band into a digital format using Pulse Code Modulation (PCM). The encoded signal can be readily handled by digital time-space crosspoint switches and digital transmission interfaces. The codecs also perform the converse function of decoding PCM back into an analog format. The MH88610 is a thick film hybrid circuit which can be used to implement the remaining BORSCHT functions mentioned previously.

This application note provides details on how the Zarlink MT8960-67 series of Voice Codecs can be used in conjunction with the MH88610 to implement a complete subscriber line interface for a digital PBX. A general discussion on loss and level plans has been included to highlight how some of the features incorporated in the codecs facilitate design of switching systems. Guidelines on low noise line card design and codec protection have also been presented.

2.0 MT8960-67 Voice Codec General Application Information

The MT8960-67 (MT896X) series of voice codecs integrate all the functions necessary to convert analog voice signals to PCM and PCM back to analog. The devices meet CCITT and AT&T codec standards for primary rate interface. The MT8960-67 series of codecs are optimized for use in line card type applications and therefore incorporate several features not generally seen in other devices with similar functionality including software programmable gain pads, uncommitted drive outputs and a number of loopback and test modes.

Device Type	Part Number	Number of SD Outputs	Code
A-Law Devices	MT8961	4	True Sign/True Mag.
	MT8963	6	True Sign/True Mag.
	MT8965	4	ADI*
	MT8967	6	ADI*
μ-Law Devices	MT8960	4	True Sign/True Mag.
	MT8962	6	True Sign/True Mag.
	MT8964	4	True Sign/Inv. Mag.
	MT8966	6	True Sign/Inv. Mag.

Table 1. Voice Codec Variants Manufactured by Zarlink

** Alternate Digit Inversion*

The basic differences in the codec variants are described in Table 1. The even numbered devices - MT8960, MT8962, MT8964 and MT8966 all use the μ-companding law. The MT8960 and MT8962 conform to the sign and true magnitude data format. The MT8964 and MT8966 conform to the sign and inverted magnitude format. In the latter, the seven magnitude bits are inverted. To ensure a higher ones density, AT&T requires the line code output by an interface on to a T1 line to conform to the sign and inverted magnitude format. However, this requirement does not necessarily restrict the user to the MT8964 and MT8966 because most T1 interfaces perform the inversion of the data bits before the signal is transmitted on the line side. Zarlink's MT8976 T1 interface device offers a user selectable option to enable or disable inversion of the magnitude bits. Therefore any of the μ-law codecs can be used with it.

The odd numbered devices - MT8961, MT8963, MT8965 and MT8967 use the A-companding law. The MT8961 and MT8963 conform to sign and true magnitude data format. The MT8965 and the MT8967 generate a code in which the even numbered bits of the octet are inverted (Alternate Digit Inversion) - a requirement specified by CCITT for PCM code transmitted on the primary multiplex line. Zarlink's European primary rate interface devices, the MT8978 and MT8979, provide user selectable options which permits either type of codec to be used.

The MT8960, MT8964, MT8961 and the MT8965 have only four uncommitted drive outputs, while the MT8962, MT8966, MT8963 and the MT8967 have six such outputs.

3.0 MT8960-67 Functional Description and Application Details

A detailed codec functional and pin description is available in the MT8960-67 data sheet. A brief

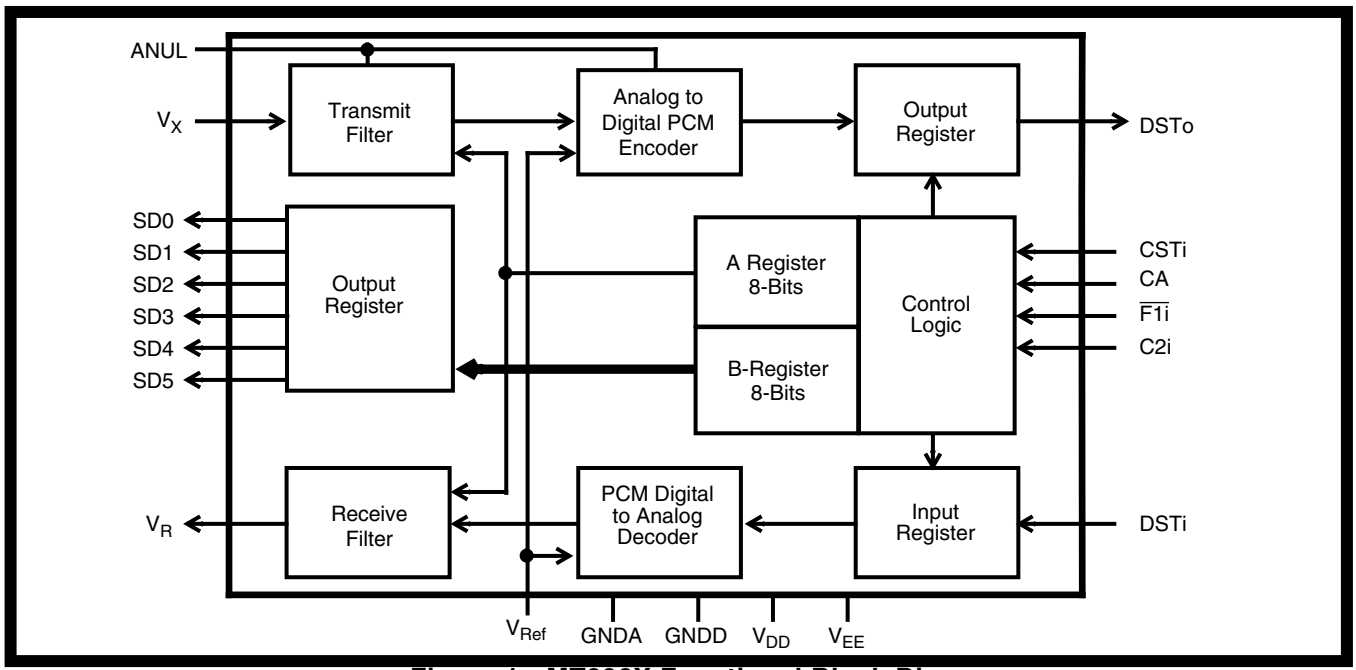

Figure 1 - MT896X Functional Block Diagram

summary is presented below to highlight some of the features of the device as they pertain to digital control and data I/O.

The analog signal input to the device at the Vx pin (see Figure 1) is filtered using switched capacitor filters. It is sampled by the analog to digital converter which generates the appropriate PCM byte according to the applicable encoding law (μ-law or A-law). The 8 bit digital byte is held in a serial register. It is clocked out at DSTo with the 2.048 MHz signal applied at C2i when the digital interface is enabled by asserting the appropriate level on $\overline{F1i}$ and CA. The PCM byte from the far end is also clocked into the device through the DSTi input at this time. The device performs the D/A conversation and makes available the filtered analog signal on V_R. The codec uses the signal applied at C2i for all internal timing and clocking of switched capacitor filters. In order for the device to meet the stringent CCITT and AT&T standards, the frequency of the C2i clock should be accurate to within ± 0.1%.

As mentioned earlier in the introduction, the MT8960-67 series of voice codecs have a number of extra features which facilitate line card design. Features such as gain control, activation/ deactivation of uncommitted drive outputs, loopback and test modes, and, the powerdown mode are all accessed through the serial control input pin CSTi. This pin accepts data in a serial format for two internal registers, A and B.

The A register is loaded when $\overline{F1i}$ and CA are both low (GND). When $\overline{F1i}$ is low (GND) and CA is high (+5V), register B is loaded. The A register controls the gain pads, loopback modes and the powerdown function. The B register controls the state of the external uncommitted drive points (SD0-SD5) and the various test modes. Note that the data input at CSTi must be continually made available to the device once per frame. This is illustrated in the timing diagram shown in Fig. 2. It is possible to use the codecs in a default mode. If CA is tied to -5V and CSTi is tied to ground, the encoder and decoder will function normally. However the gain pads will be set to the default state of 0dB, the uncommitted control outputs will all be disabled, and the various test modes will not be accessible. In the second default mode, CA is tied to GND and serial data clocked into CSTi may be used to control the receive and transmit gain by loading the A register.

3.1 Channel Timeslot Assignment

The $\overline{F1i}$ and CA inputs are used to assign a device to a specific 8 bit channel within a time division multiplexed serial stream such as the ST-BUS. The ST-BUS is a time division multiplexed serial bus with a bit rate of 2048 kbit/s. In a telecommunications

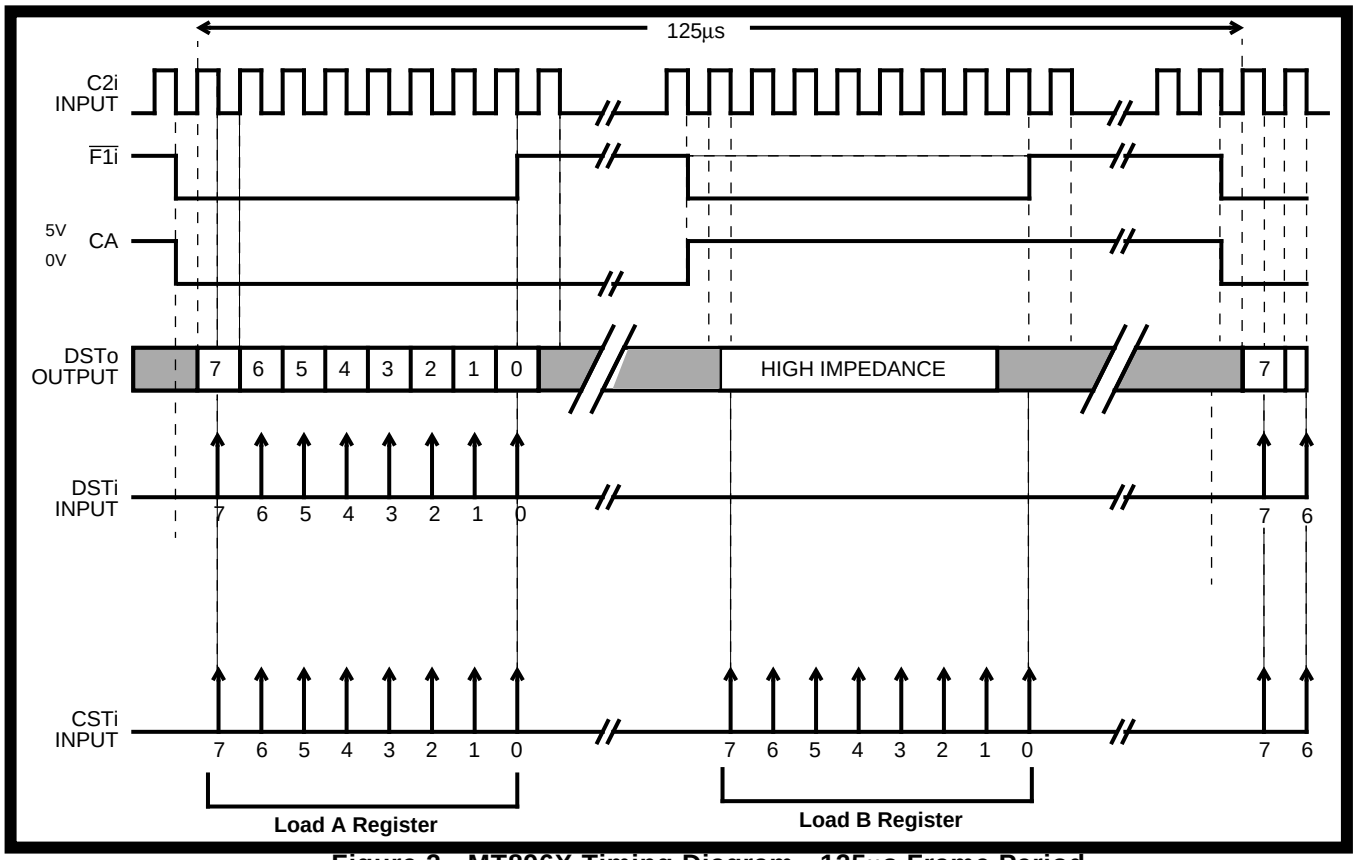

Figure 2 - MT896X Timing Diagram - 125μs Frame Period

environment, the serial stream is divided into thirty two 8 bit channels. Each channel has a bandwidth of 64 kbit/s. The voice codec uses one ST-BUS channel for PCM data and two channels for control. The digital word is clocked out (most significant bit first) with the first rising edge of C2i after $\overline{F1i}$ is taken low. When $\overline{F1i}$ is high, the device does not accept any input at the DSTi or CSTi pin and the DSTo output goes into a high impedance state.

The timing relationship of the C2i clock signal with respect to the input and output digital word and $\overline{F1i}$ is illustrated in Figure 2. The $\overline{F1i}$ set-up time of 50ns and hold time of 25ns with respect to the rising edge of C2i must be adhered to in order for the device to operate properly (see MT8960-67 data sheet for more information). The MT896X is enabled on the first rising edge. $\overline{F1i}$ must subsequently be taken high after eight periods of C2i, as shown in Figure 2.

The timeslot assignment circuit shown in Figure 3 generates the Framing type 1 (F1o) and the Control Address (CA) signal in a manner which allows the codec to be assigned to any one of 32 channels. The F1oX (where X = 0, 1, 2,... 31) output from the circuit is connected to a codec's $\overline{F1i}$ input. The CA output from the circuit is connected to the CA input on the first 16 codecs.

The codec connected to F1o0 will be enabled during timeslot 0 on the ST-BUS serial stream. Similarly a codec connected to F1o1 will be enabled during channel 1. For codec 0, the $\overline{F1i}$ and CA signals are both low during timeslot zero. During channel 16, only $\overline{F1i}$ is taken low. CA is kept high. Thus register A will be loaded during timeslot zero and register B will be loaded during timeslot 16. The CA inputs on the first 16 codecs are connected directly to the CA output of the timeslot assignment circuit. The CA inputs of the next 16 are connected to an inverted CA. Thus codec number 16 will accept its PCM input and load the A register during timeslot 16 when both CA and $\overline{F1i}$ are low. The B register will be loaded during timeslot 0 when CA is high and $\overline{F1i}$ is low.

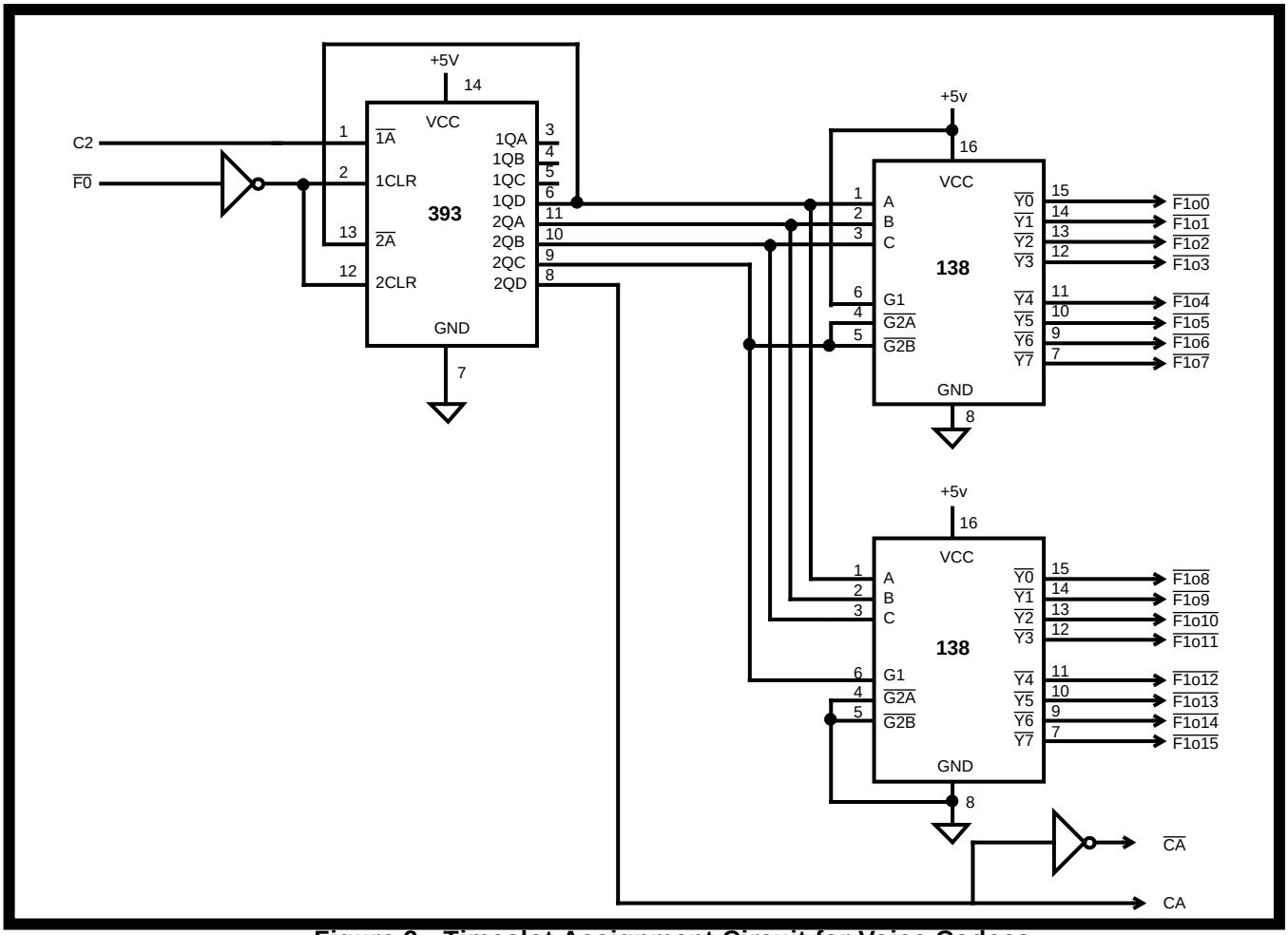

Figure 3 - Timeslot Assignment Circuit for Voice Codecs

3.2 Switching and Control Using the MT8980 Digital Crosspoint Switch

Zarlink's ST-BUS devices are designed to complement each other in terms of functionality and ease of interface. The MT8980 digital crosspoint switch can be used both for switching and control function. It has eight serial input ports and eight serial output ports. Each of these I/O ports support a 32 channel ST-BUS stream. Any channel on the ST-BUS inputs can be switched to any output channel timeslot. An output channel can also be programmed to source data from internal memory. This mode, referred to as message mode, can be used for controlling peripheral devices. In message mode, the 8 bits corresponding to the specific memory location in the connection memory are transmitted out during the appropriate timeslot on the ST-BUS stream. A peripheral device such as a codec connected to this stream and assigned this specific channel timeslot, will accept the byte. In this manner the control registers of the various devices are effectively mapped into memory locations in the MT8980. The microprocessor interfaced to the MT8980 writes the appropriate word to the connection memory corresponding to the selected output channel. The contents of the memory are continually output, once per frame, until the MPU changes the mode of operation. This feature can be used to control the MT896X codecs by placing the appropriate channels on the ST-BUS stream connecting the MT8980 digital switch to the CSTi inputs of the MT896Xs in message mode (refer to the MT8980 data sheet and MSAN-123 Application Note *"The MT8980 and MT8981 Digital Crosspoint Switches"* for more details).

A simplified configuration of a switching system using the MT8980 and the voice codecs is illustrated in Figure 4. The MT8980 provides both the switching and control function.

The configuration illustrated in Figure 4 shows only 32 codecs. The MT8980 has the capability to support 256 voice channels. In applications utilizing the full capability of the codec, three ST-BUS channels per device are required. One for the PCM data and two for controlling the device via the A and B registers. Therefore to support 256 codecs fully for switching and control, three MT8980s would be required. However, as mentioned earlier, the MT896X series of voice codecs can be operated in a default mode whereby only the encoding and decoding function is utilized. The A and B registers are not loaded. In this case, only one MT8980 would be required to function in a switching capacity for 256 voice codecs.

The ST-BUS I/O streams chosen for illustration in Figure 4 were selected arbitrarily. The STi0 input stream on the MT8980 accepts PCM data from the codecs for switching. The output stream STo0 transmits PCM data to the codecs. All 32 codecs share a single input stream and a single output stream. STo1 and STo2 are used for controlling the devices. The timeslot assignment circuit provides the $\overline{F1i}$ and CA signals which enable the appropriate codec at a specific time during which it accepts data from the TDM stream. For example, the $\overline{F1i}$ and CA signals input to codec #0 go low during channel timeslot 0. This codec will clock in PCM data originating from the MT8980 STo0 during this timeslot. The device will also clock out PCM data for transmission to the MT8980 over the STi0 at this time. Each codec requires two ST-BUS channels for control. Since each ST-BUS stream is capable of supporting only 32 channels, only 16 codecs can be handled by each stream. In the configuration illustrated in Figure 4, CSTi inputs of the first 16 codecs are connected to STo1, while the remaining 16 are connected to STo2. Also note that the first sixteen devices (0 to 15) receive CA from the timeslot assignment circuit where as the last 16 receive $\overline{CA}$. Thus codec number 16 will accept PCM input and data for register A during timeslot 16. Register B will be loaded during timeslot "0" via CSTi. As an example, in Figure 4, codec # 0 has its CSTi pin connected to STo1. This codec has also been assigned channel 0 for its A register and channel 16 for its B register. In the MT8980, channels 0 and 16 on this stream are put in "message mode". The appropriate control byte desired for the A register is placed in the Connection memory location corresponding to channel 0, output stream 1 (STo1). The control byte for the B register is written into the connection memory low corresponding to channel 16, stream 0. The control bytes are accepted by this codec during channel timeslot 0 and 16. The timeslot assignment circuit generates the $\overline{F1}$ signal and the CA signal.

Note that if the channel assignment circuit illustrated in Figure 3 is used, the voice codec expects the A and B registers to be updated once per frame.

The MPU interface to the MT8980 can place the codecs into the different modes and control external devices or circuits connected to the SD outputs. The transmit and receive gains of each codec can be controlled digitally through the A register.

Supervisory information originating from the line card, such as an off-hook indication, can be multiplexed onto a ST-BUS channel using the circuit illustrated in Figure 5. The circuit can be assigned an ST-BUS channel using the timeslot assignment

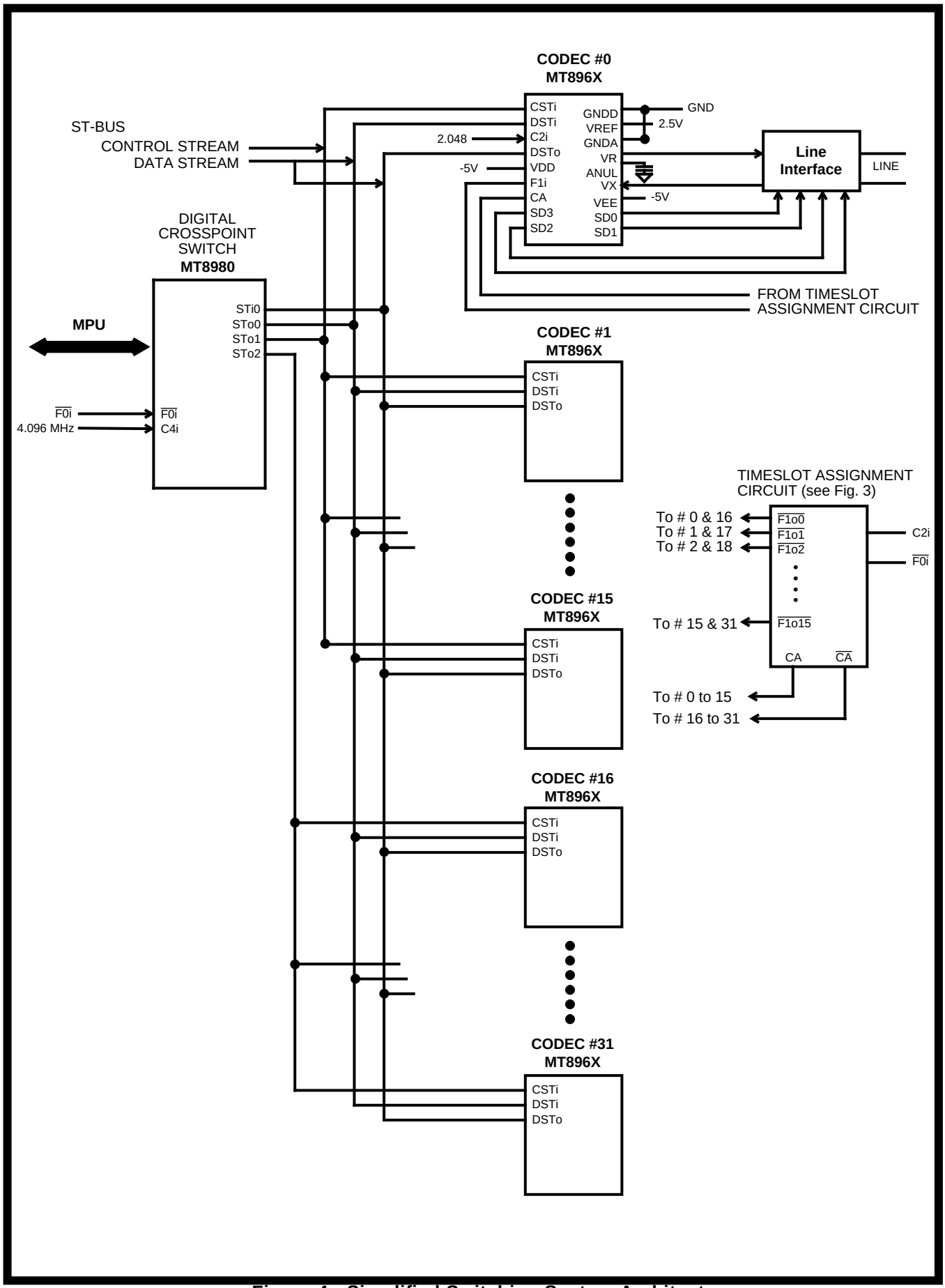

Figure 4 - Simplified Switching System Architecture

circuit shown in Figure 3. The status from eight interfaces can be multiplexed on to a single ST-BUS channel and transmitted to the MT8980. The MPU interfaced to the MT8980 can monitor this channel by reading the appropriate "Data Memory" location in the MT8980. When an off-hook condition on any of the lines occurs, the appropriate bit in the received channel is set (or reset as the case may be). This is detected by the mpu which then takes appropriate action i.e. connects an incoming call to the subscriber or conversely, if the subscriber is requesting service, connects a dial tone source to it.

This type of serial control and switching bus architecture minimizes PCB tracking density and backplane wiring. This in turn permits more line interfaces to be supported per card. Consequently the overall size of the system can be reduced. The lower power consumption and reduced physical size requirements can offer an important marketing advantage. The physical wiring and drive requirements of a parallel bus for similar contol capability adds extra cost penalties which are not offset by advantages inherent in the simpler parallel bus architecture.

4.0 Subscriber Line Interface Circuit Applications

Voice codecs are four wire devices, i.e., the encoded voice is transmitted and received on different paths. Connection of a codec to the balanced analog two wire subscriber loops requires a 2 to 4 wire converter circuit referred to as a "Hybrid". The hybrid function is an integral part of the Subscriber Line Interface Circuit. The Subscriber Line Interface Circuit (SLIC) also provides battery feed for operation of the subscriber telephone. It asserts ringing voltage on the loop to alert the subscriber of an incoming call, and, detects when the subscriber set goes off-hook. The hybrid and battery feed function has traditionally been performed using transformers. However, with the continuing trend in the industry towards smaller and more compact systems, transformerless SLICs are rapidly becoming more common. Transformerless SLIC's have size advantages and can be designed with switchable options to permit use of the same line card in different applications.

The basic principle of operation of a hybrid is illustrated schematically in Fig. 6. If the impedance reflected to the primary side of the transformer equals Z_B, then the transmit signal component will be cancelled from the composite signal on the receive output - thus isolating the receiver from the transmitter. In order to maximize the cancellation, Z_B should be matched to Z_L (the two wire loop impedance) as closely as possible. In the practical loop environment, there is significant variability in length and wire size. Matching impedance on a line to line basis is not practical. In PBX applications two standard balance networks are chosen - one for short loops (generally 600 ohms) and a second for long loops (350 ohms in series with Ik ohm shunted with 0.21 µF). The degree of cancellation for a

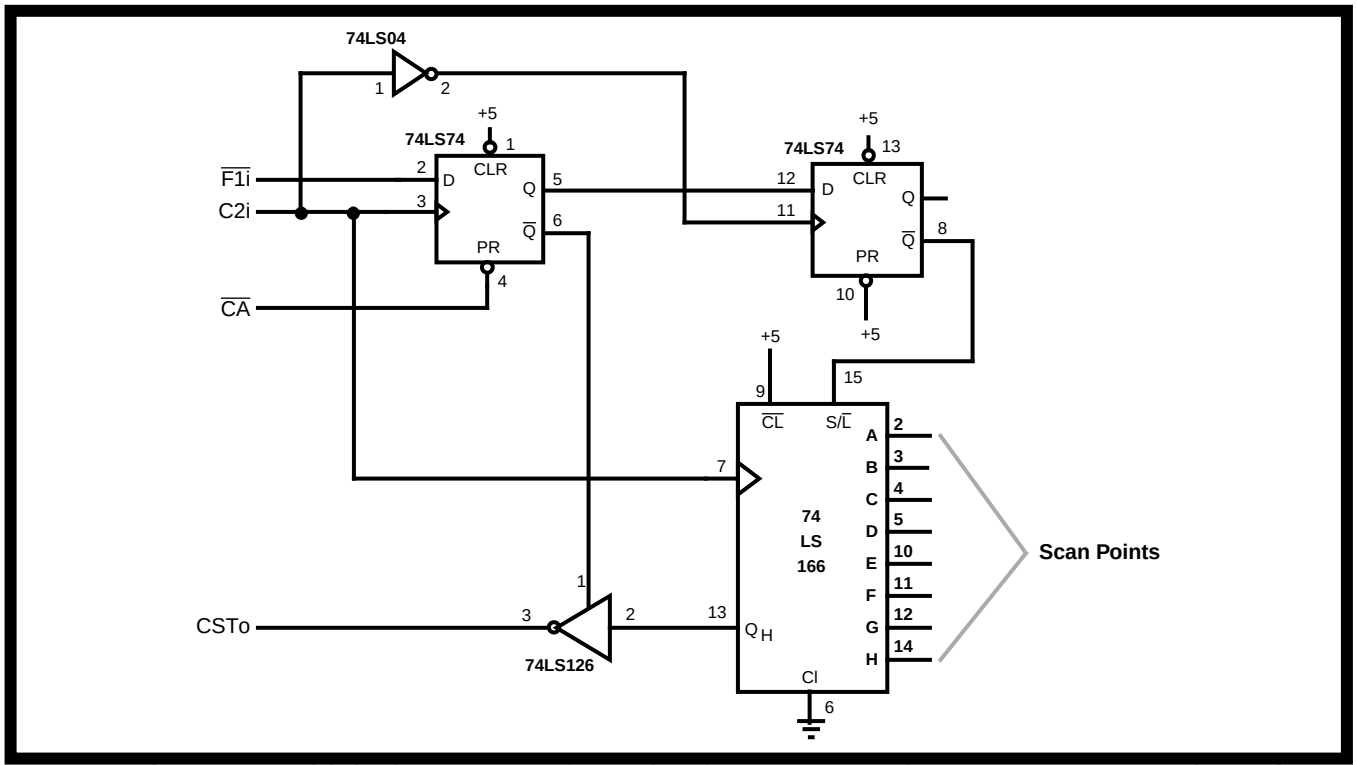

Figure 5 - Multiplexing Status Information from 8 Scan Points on to a ST-BUS Channel

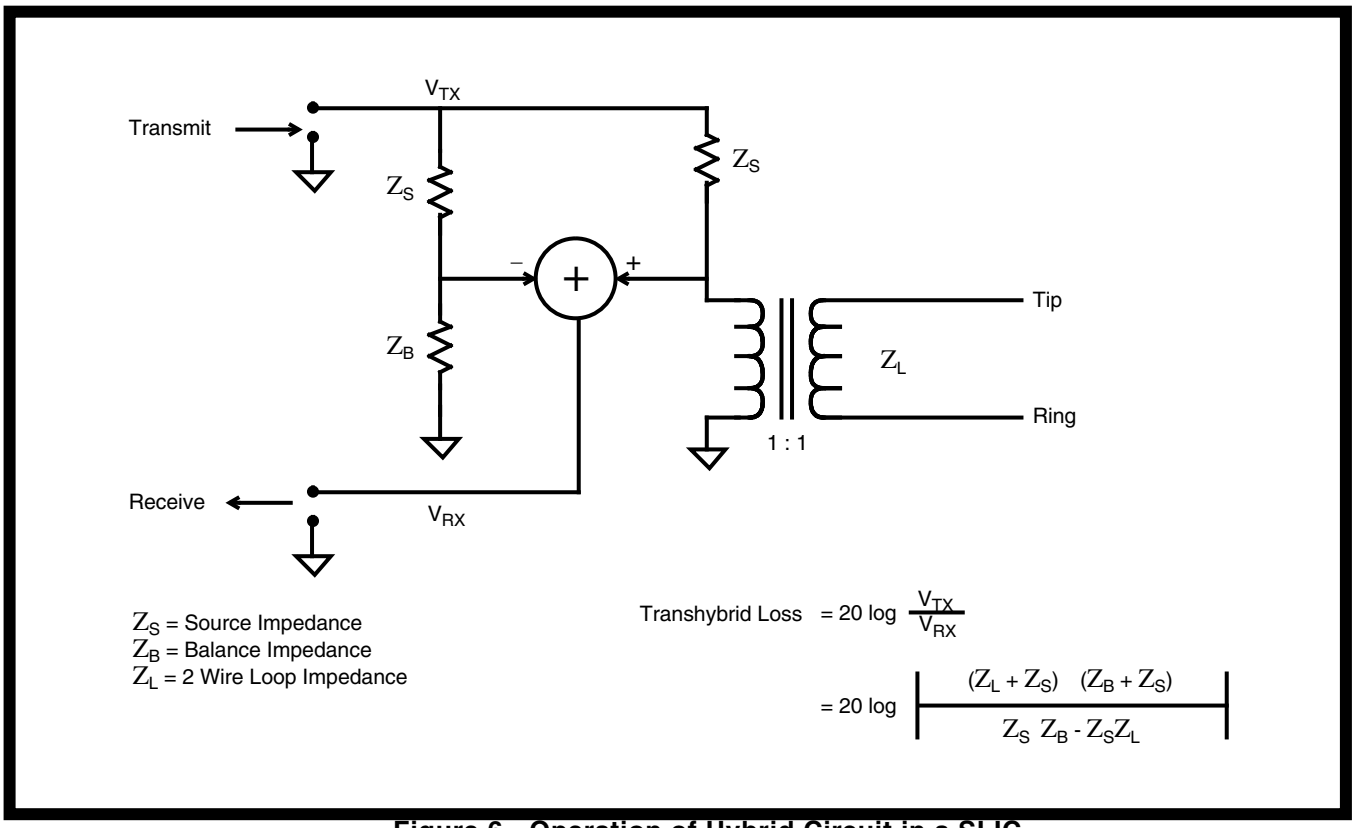

Figure 6 - Operation of Hybrid Circuit in a SLIC

particular line interface circuit is specified as the Transhybrid loss. SLIC's can be designed so that the balance network is selected using an externally accessible node in the hybrid circuit. By tying this node to ground or permitting it to float, effectively modifies the balance impedance. The SD outputs on the Zarlink codecs may be used to switch the node to ground or leave it floating. For example, the outputs SD3 to SD5 are open drain outputs which are pulled to ground when the appropriate bit in Control Register B is set. Therefore, if the external node which selects the balance network in the hybrid is tied to one of these drive points, the correct balance network could be selected by merely writing to the codec's control register. This would allow the switching system to be reconfigured for different loop types through software control at time of installation or when changing requirements make it necessary. Other filters and gain pads may also be switched in or out of the circuit to suit specific applications in a similar manner.

5.0 MH88610 Application Details

The Zarlink MH88610 is a Subscriber Line Interface Circuit (SLIC) designed specifically for on-premise applications. The application circuit shown in Figure 7 shows how the MT896X codecs can be used with this device to interface to a two wire subscriber loop.

The MH88610 provides an interface between the two wire subscriber loop and the four wire codec. It does all of the SLIC functions described in the preceding section.

5.1 Battery Feed

The MH88610 provides the loop with constant DC current to power the telephone set. The voltage applied at the V_{Ref} pin determines the actual magnitude of the loop current.

$$I_{Loop} = V_{Ref} / 0.423 \qquad \text{mA } (\pm 2 \text{ mA})$$

where V_{Ref} is in volts and is negative with respect to ground.

For typical applications, the DC subscriber loop current required is 26mA. This requires V_{Ref} to be -11V which can be generated from the 2.5V reference used by the voice codec (see Fig. 7). The loop is connected to the Tip and Ring pins on the hybrid. Varistors RV1 and RV2 provide primary protection against overvoltage to the MH88610. Diodes D1, D2, D3 and D4 provide secondary protection.

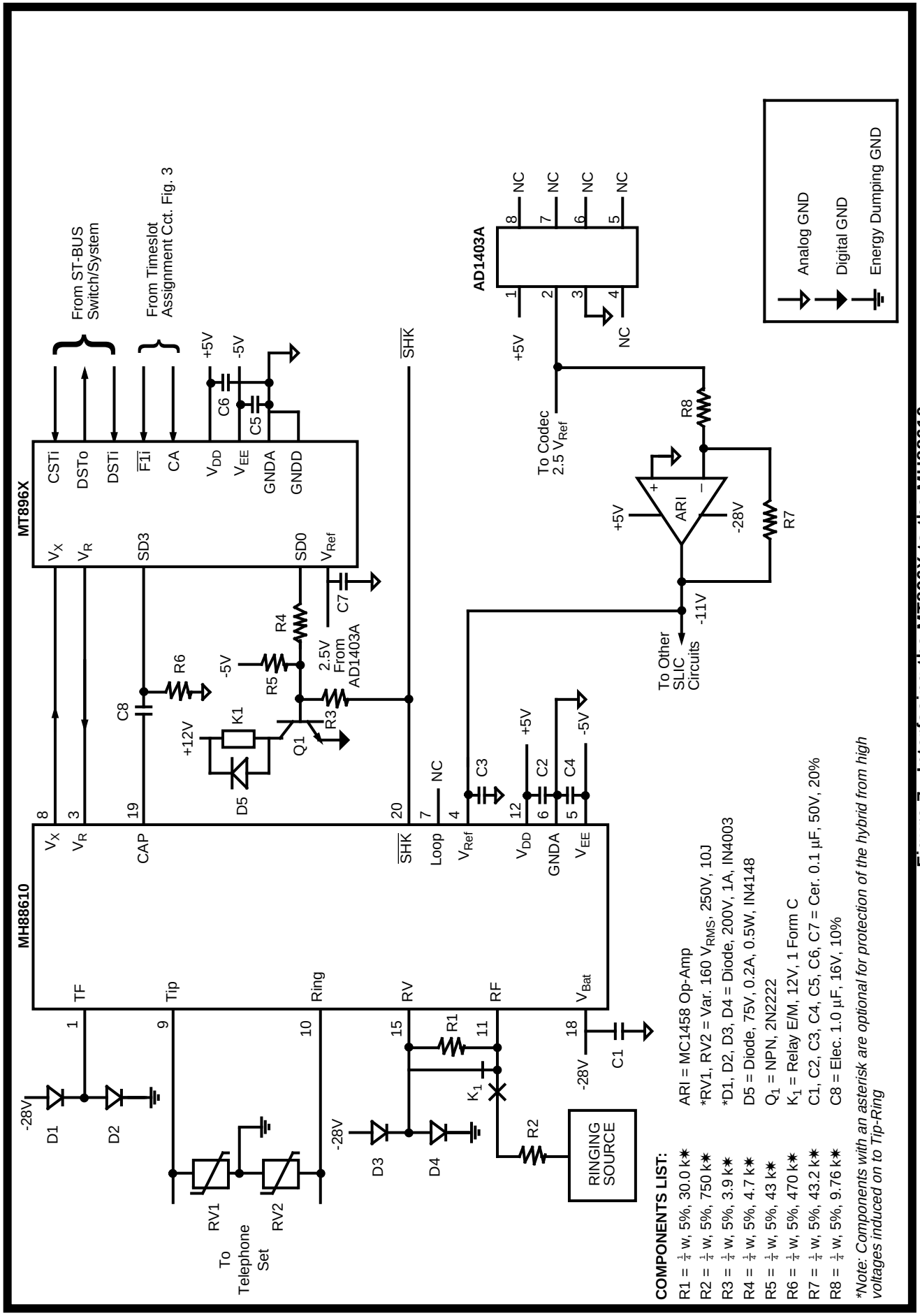

Figure 7 - Interfacing the MT896X to the MH88610

5.2 Off-Hook Detection and Dial Pulse Signalling

When a subscriber set goes off-hook, the local loop is closed and a DC current flows. The MH88610 monitors the loop current flow and indicates an off-hook condition when a specific threshold has been exceeded. The current flow is a function of the loop impedance. An off-hook will be detected by the MH88610 when the loop impedance falls below 1200 ohms. The $\overline{SHK}$ output on the MH88610 can be monitored by the system processor to detect when the subscriber set goes off hook.

Dial pulses are generated by the subscriber set by opening and closing the loop and therefore can be detected on the $\overline{SHK}$ output. The processor monitoring the output would have to time and count the pulses.

5.3 Application of Ringing and Automatic Ring Trip Implementation

Ringing is applied to the line by disconnecting RF from RV and connecting a ringing generator to the RF pin. Relay K1 is activated by the SD0 pin on the MT896X. Resistor R1 serves to provide battery feed to the subscriber loop during the transitionary state. R2 is necessary to limit the surge of DC current when the subscriber set goes off-hook.

The ringing signal must be DC biased at the battery voltage in order for the MH88610 to detect an off-hook condition while the ringing signal has been applied. The operation of the ringer at the telephone end of the loop causes AC current to flow in the loop. This current may cause the device to indicate a false off-hook. In order to prevent this from happening, a capacitor is connected between ground and the CAP pin while the ringing signal is connected to the loop. The capacitor is disconnected for normal operation when the ringing signal is removed. In the application circuit one of the SD outputs of the codec is used to ground one end of the capacitor when the ringing is applied. The SD3 output is an open drain output which is in high impedance state when it is deactivated and connected to GND when activated. For normal operation SD3 is deactivated and the ground is removed. C8 is left grounded through a 470 kΩ resistor. The resistance is large enough that C8 is effectively out of the circuit. Resistors R3 and R4 are used in order to disconnect the ringing signal from the two wire loop when the subscriber set goes off-hook during ringing. When the set goes off-hook, the $\overline{SHK}$ output will go low to-5V. This will turn off transistor T1 which in turn will disable relay K1, thus disconnecting the ringing signal from the loop.

5.4 Transmit and Receive Signal Levels

The transmit and receive levels for the Codec-SLIC circuit depend upon the gain through the SLIC and the programmable gain through the codec.

0dBm0 for a Codec

Codecs from different manufacturers operate at voltage levels best suited to the semiconductor technology used. However, all PCM codecs designed to meet CCITT standards are calibrated to a defined full scale standard. The maximum peak analog voltage which the device can accept is referred to as the overload decision level and corresponds to 3.172 dBm0 for μ-law devices and 3.14 dBm0 for A-law devices. The 3.172 dBm0 level is defined by CCITT as being a sinusoid whose peak voltage is equal to ±8159 normalized voltage units for μ-law codecs. The normalized voltage units have been chosen so that all quantization levels are expressed as integers. For A-law devices the comparable value is ±4096 units. In this manner the CCITT standard indirectly defines the power at the 0 transmission level point. All gains and losses in a digital system are specified with respect to this power level.

The overload decision level for Zarlink μ-law codecs at the analog input corresponds to a voltage of 4.829 volts peak-to-peak. This voltage level has been selected purely due to the technology used for the A/D or D/A conversion in the device. By definition, according to CCITT recommendations, this corresponds to a power level equal to 3.172 dBm0.

3.172 dBm0 = 4.829 Vpp

0 dBm0 = 3.352 Vpp or $1.185V_{RMS}$.

External gain or loss has to be added for specific requirements. The gain pads built into Zarlink Codecs can be used to change the gain or attenuation.

The 0 dBm0 level for Zarlink μ-law codec's is 1.185 V_{RMS}. This is the amplitude of the analog signal generated at the V_R output when a digital milliwatt byte sequence is input at the PCM port of the codec. The digital milliwatt corresponds to 0 dBm (see window on 0 dBm0)

1.185 V_{RMS} = 3.69 dBm (referred to 600 ohms)

Therefore there is a net gain of 3.69 dB when a digital signal is converted to analog by the codec.

The MH88610 attenuates the signal applied at the V_R pin by 6.69 dB (typical) before transmitting it out on Tip and Ring. When the voice codec is interfaced to the MH88610, there will be a net attenuation of 3 dB from the digital side to the analog two wire side. Conversely, when a 3.69 dBm signal is applied at the V_X input of the codec, the PCM signal generated corresponds to a digital milliwatt which by definition is the digital equivalent of 0 dBm. Therefore there is a net loss of 3.69 dB when an analog signal is converted to PCM. The MH88610 applies a gain of 0.69 dB in from the two wire tip and ring port to the V_X pin. Therefore there is a net loss of 3 dB from the two wire port to the digital port.

The losses and gains for a typical connection are illustrated in Figure 8.

The gain and losses through the voice codec can be changed by the user through Control Register A. The gain in the transmit direction can be increased by 7 dB in 1 dB steps. When the codec is used in combination with the MH88610, the maximum gain that can be added from the Tip/Ring port to the digital side is 13 dB. In the digital to analog direction, the attenuation can be varied from 0 to -7 dB in 1 dB steps. Incorporating the loss introduced by the MH88610 and the inherent loss in the D to A conversion (due to the codecs designed 0 dBm0 level), the net attenuation from the digital side to the Tip and Ring port can be varied from -3 to -10 dB.

The facility to modify the gain or loss on a connection-by-connection basis is necessary to meet loss and level plans imposed by different telephone administrative authorities (see next section). The software control of the gain pads in the Zarlink voice codecs makes it very easy to meet different loss and level plans. For example, in the connection illustrated in Fig. 7, if the end-to-end loss required was 3 dB, the codecs transmit gain pads in both ends could be set to provide 3 dB gain. This would counter the fixed losses of the various components. For 0 dB net loss through the system, the gain in the receive direction (A to D) would have to be set to +6 dB.

6.0 Consideration of Loss and Level Plans in SLIC Design

Introduction of digital switching and transmission can be expected to improve the overall transmission quality. However, this will occur only when the penetration of both digital transmission and switching becomes high. In the interim, where a mixture of analog/digital transmission and switching predominates, a certain degree of degradation of the signal occurs due to the A/D and D/A conversions, and, due to loss introduced to maintain stability in specific connections. In an all digital network, transmission and switching systems will not add any appreciable degradation to the end-to-end quality of the voice signal. Unlike transmission of an analog voice signal, PCM encoded signals do not not undergo any attenuation during transmission. There will be no requirement for 2/4 wire hybrid circuits since digital transmission requires separate receive and transmit channels. On standard telephone loops this can be achieved using elaborate echo cancellation or time compression multiplexng schemes.

Digital switching and transmission systems are inherently four wire. The encoded voice is transmitted and received on different paths - making up a four wire circuit. Connection to a two wire analog loop, requires a hybrid circuit (described in the previous section). The four wire circuit forms a closed loop feedback system. If the impedance of the hybrid balance network does not match the impedance of the subscriber loop, energy will circulate within the closed four wire path. The connection will start to oscillate if the closed loop has unity voltage gain at a frequency at which the phase shift is a multiple of 360 degrees. In telephony, the tendency of a system to oscillate is described using the parameter referred to as Sing Margin. If the Sing Margin is low, the connection tends to sound hollow (the rain barrell effect) or distorted. The rain barrel effect can also be due to the presence of listener echo. Listener echo is the result of the talker's signal going through two reflections and adding, with some delay, to the transmitted signal. The listener perceives the received sound to be hollow. The phenomenon is illustrated in Fig 9. On long connections talker echo is more dominant.

One other factor which is also of significant importance in network design is contrast minimization. Contrast minimization generally entails limiting the loudness in connections which do not

have sufficient inherent loss in the level of the signal transmitted. This ensures that the difference in type of connections made is not perceptible to the caller and the loudness level is maintained within a specific tolerance level.

In order to control singing, near singing, talker echo and minimize contrast, loss is introduced in the connection. A compromise loss value is selected so that the extra added signal attenuation provides adequate echo control while providing satisfactory volume level for the primary speech path. The actual loss added depends upon the type of connection, the type and length of trunk involved, etc. Loss and level plans implemented by telephone administrations are based on large amounts of statistical data and take into account the various factors discussed above. The North American VIA Net Loss Plan was introduced in the 50's for loss allocation in the largely analog network. The more recent North American Switched Digital Network Loss Plan was introduced in the 70's to accommodate the emerging digital switching technology in the class 5 end office. Under this plan digital trunks are operated at zero loss. The

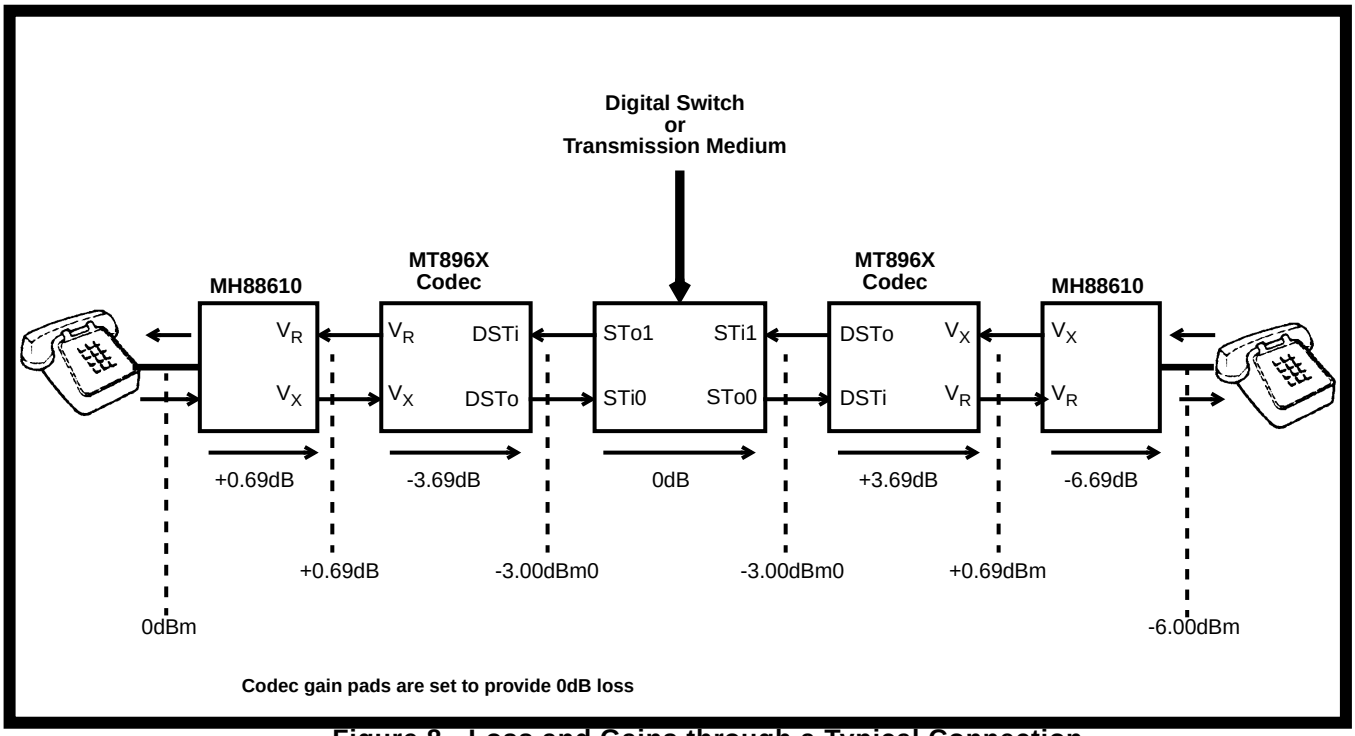

Figure 8 - Loss and Gains through a Typical Connection

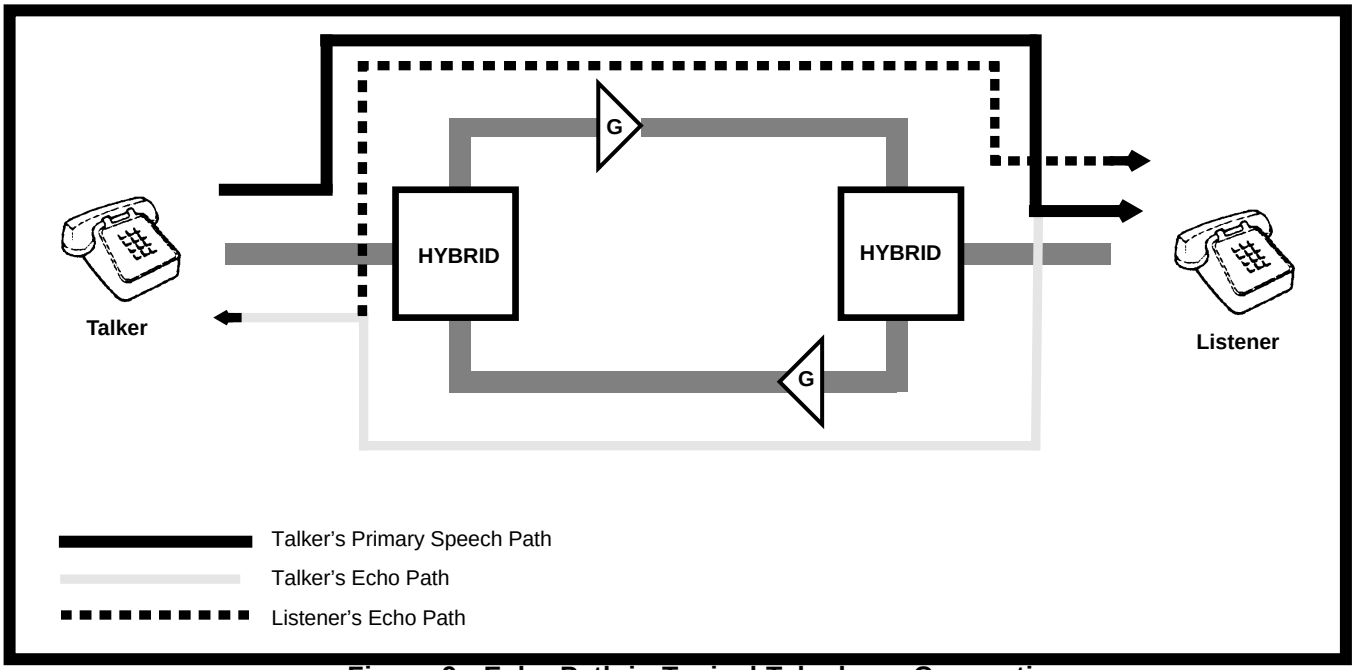

Figure 9 - Echo Path in Typical Telephone Connection

switch adds extra loss to realize the required line to trunk loss. For example, 6 dB loss is added in connections to digital tandem office trunks, while only 3 dB loss is added for digital intraoffice trunks in a metropolitan area. Intraoffice calls have a nominal 0 dB loss through the switch.

Loss and level plans can differ significantly from one country to another.

Digital PBXs have to accommodate a number of different line types and can, therefore, have similar constraints as the public switched network. Different line types include digital on-premise lines, off-premise lines, analog central office trunks, digital central office trunks and digital toll office trunks. On-Premise Subscriber Line Interface Circuits (ONS) interface directly to the subscriber two wire loops which service standard telephone set for basic POTS function. Off-Premise Subscriber Line Interface Circuits (OPS) interface to loops which traverse outside the protective environment of a building. The loop length is generally longer here also. OPS circuits may also be employed in Direct Inward Dialing Trunk interfaces (connecting to a central office). Central Offices are generally interfaced to the PBX through either Loop Start or Ground Start trunks. Digital Central Office Trunks such as AT&T's T1, are also becoming more common especially in larger PBX's. Digital transmission over standard loops is also increasingly being employed behind the PBX. This has been greatly helped by the wide scale availability of integrated circuits such as Zarlink's MT8972 which permit full duplex transmission of high speed digital signals over standard twisted pair. The capacity of a single loop can effectively be doubled by using a device such as the MT8972. This makes it cost effective for PBX manufacturers to offer full feature phones which permit simultaneous voice and data transmission over existing telephone wiring in a building.

In order to make private networks compatible with the public network, the Electronic Industries Association has developed a loss and level plan for digital PBXs. This plan stipulates the recommended insertion loss for different connections. A short summary of the plan has been presented in Table 2 in matrix form. Note that all the possible connection types have not been included in the diagram.

As an example note that when an ONS line is connected to another ONS line, 6 dB of attenuation is inserted in both directions. In ONS-OPS type connections, the inserted loss is only 3 dB. No loss is inserted when an ONS line is connected to a C.O. trunk.

		ONS ≠ ↓	OPS ≠ ↓	A/TT ≠ ↓	D/TT ≠ ↓
ONS	→	6	3	3	3
	←	6	3	3	9
OPS	→	3	0	2	0
	←	3	0	2	6
A/CO	→	0	0	$0_{/2}$	$-3_{/0}$
	←	0	0	$0_{/2}$	$3_{/6}$
D/CO	→	3	0	2	$0_{/-3}$
	←	3	0	2	$6_{/3}$

Table 2. μ-Law Digital PBX Loss Plan (Ref. 1)

ONS : On Premise Subscriber
OPS: Off Premise Subscriber
A/CO: Analog Central Office Trunk
D/CO: Digital Central Office Trunk
A/TT: Analog Tie Trunk (interconnecting two PBX's)
D/TT: Digital Tie Trunk

The programmable gain pads in Zarlink's Voice Codecs simplify the circuitry required to accommodate loss and level plans in different countries.

7.0 Line Card Power Supply Filtering and Codec Circuit Protection

Zarlink CMOS filter/codecs are extremely reliable devices. Significant measures have been incorporated into the design of the device to prevent latchup caused by external factors. However, in applications where the circuit cards are inserted into live sockets, adhering to the following guidelines will help to further reduce the probability of latchup (see Fig. 10).

- Ensure that ground is always connected to each device before any of the other supplies or signals. An extended ground pin should be used on the card edge connectors.

- Transient protection must be provided against even momentary transitions outside the supply voltages. Schottky diodes fitted between +5V and GND and between GND and –5V to clamp transient power supply reversals during power-up are recommended. Voltage excursions exceeding the absolute maximum ratings should be limited by connecting transorbs (with breakdown voltages not exceeding 6V) across V_{DD} and GND, and, across GND and V_{EE}.

- All supplies must be decoupled close to the card edge connector. Decoupling with a 25μF electrolytic capacitor in parallel with a 0.1μF

ceramic capacitor is recommended. This combination provides adequate filtering for both high and low frequencies, and accommodates large current spikes due to switching. The trace length from the edge connector to the decoupling capacitors should be kept short. Further high frequency filtering may be provided by placing 50 µH inductors in series with the supplies.

- The ±5V supplies must be decoupled at each codec with 0.1 µF capacitors from +5 to GND, and _5V to GND connected as close to the device as possible.

- If the codec is connected directly to a transformer type SLIC, back-to-back 5V zener diodes from the analog input and output pins of the codec are recommended to prevent spikes induced on the line side of the transformer from affecting the codecs analog I/O pins. Zeners with low leakage should be used.

- The +5V supply for the digital control circuitry on the line card should be derived from the edge 5V - GND decoupling point. This supply rail should be kept separate from the codec supply rail.

- Each logic device should have a decoupling capacitor from +5V to GND close to the device.

Ground connections for low voltage relays should use the digital ground.

8.0 Line Card Layout Guidelines

Line card designs using voice codecs incorporate a significant amount of digital and analog circuitry. One of the most important steps in designing a low noise line card is to ensure that the layout of the circuit components and the PCB tracking result in minimum of cross coupling between analog and digital signals. The following general guidelines can serve to optimize performance (see Figure 11):

- Separate analog and digital grounds should be maintained on the circuit card. However, in order to minimize ground loops, separate grounds going all the way to the power supply are not recommended. The optimum grounding configuration is to have a single ground source

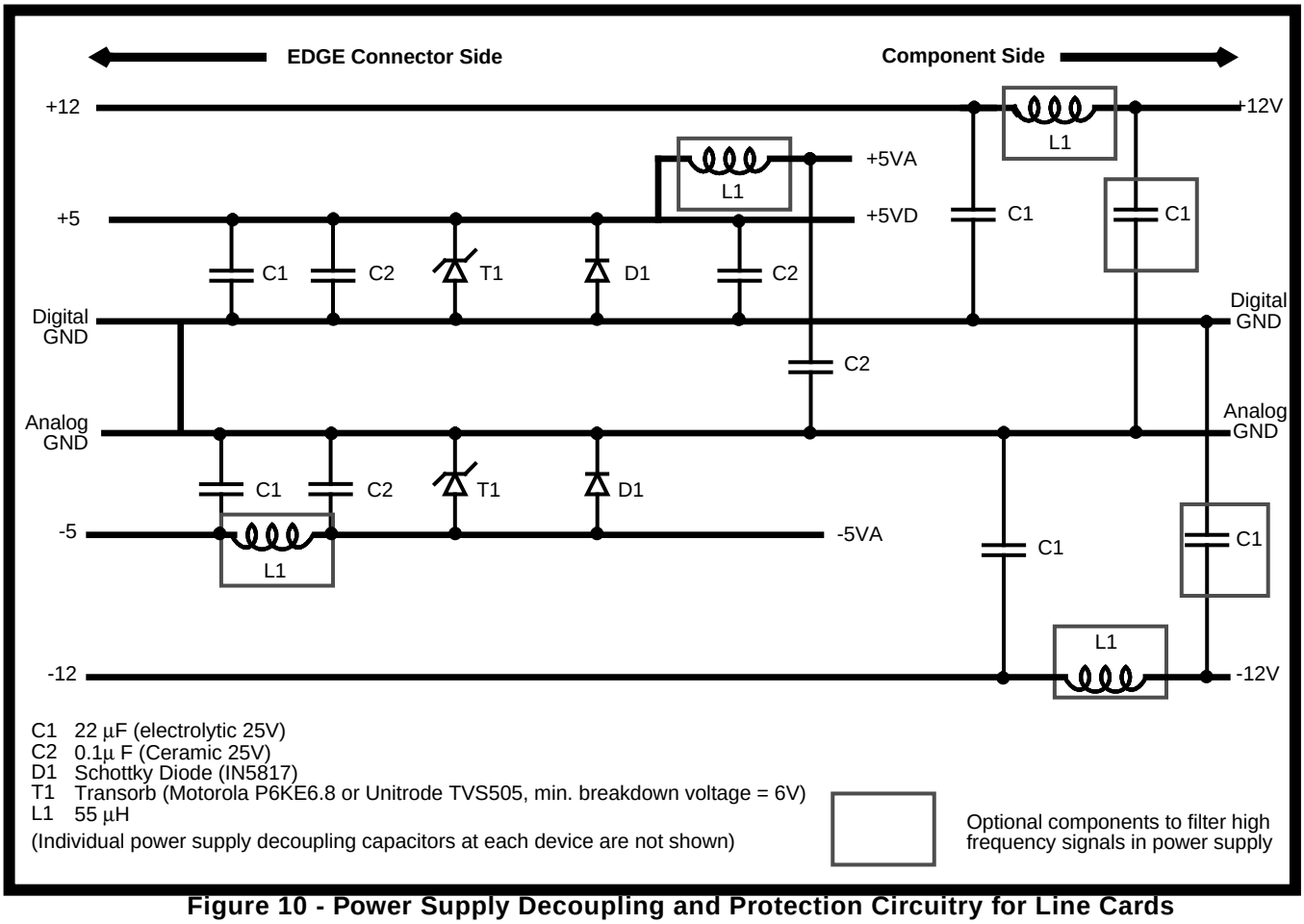

Figure 10 - Power Supply Decoupling and Protection Circuitry for Line Cards

from the power supply. If separate analog and digital ground rails are available from the power supply, they should be interconnected together near the edge connector into a central ground point for the entire card. Distinct analog and digital grounds should be derived from this common point and maintained separately on the circuit board.

- Voice codecs contain both analog and digital circuits. The Zarlink MT8960-67 series of voice codecs have two ground pins: GNDA and GNDD. As indicated in the codec data sheets the potential difference between the GNDD and GNDA pins should not exceed 0.1V. Optimum performance is achieved by connecting the two pins together close to the codec. The interconnected pair should then be tied to the analog ground rail.

- The +5V and -5V supply tracking to the codecs should be routed adjacent to the ground rails to ensure that any high frequency noise picked up by the trace is common mode.

- Digital control signals from the logic devices should not be routed near the 2.5V reference voltage input or the ANUL pin on the codec. In general, circuit traces carrying digital signals should not be run close to or in parallel with traces carrying analog signals.

- The reference voltage input is a high impedance input. The PCB trace carrying the 2.5V reference voltage must not be positioned parallel to digital signal tracking. Ideally it should be placed between analog supply or ground rails.

- The capacitor attached to the ANUL pin on the codec should have minimal lead length and track between the analog ground and the device pin.

- Edge connector pins carrying analog signals should not be assigned adjacent to pins carrying digital signals.

- All circuit tracking which carries signals capable of inducing large emf's into the audio channel should be routed around the edge of the card. This includes ringing signals, 2-wire subscriber circuits, battery feeds and relay control circuits. These tracks must not run close to or in parallel with the tracking carrying the unbalanced signals from the voice input/ output pins on the codec. The tracking for the balanced two wire subscriber lines from the SLICs should run in parallel with each other to ensure that any noise picked up is common mode.
- The diodes and varistors for primary and secondary protection for the Tip and Ring lines should be connected as close to the card edge connector as possible. A separate energy dumping ground should be used for overvoltage and lightning protection. An energy dumping ground is a heavy ground originating from the power supply.

9.0 Conclusions

The Zarlink MT896X series of voice codecs together with Zarlink's MH88610 offer telephone system designers most of the functions necessary to construct analog line interface cards for digital switching systems. Features such as programmable gain pads and uncommitted drive points in Zarlink codecs contribute to substantial savings in hardware. In addition the solutions provided by Zarlink's extensive family of compatible ST-BUS products simplify overall system design. For more information on these and other telephony components, refer to the appropriate data sheet

10.0 References

1. PN-1378 Private Branch Exchange Switching Equipment for Voiceband Applications. Proposed Rev. to RS-464-1, EIA.

2 TR-TS7-000507 LATA Switching System Generic Requirements (Section 7), Issue 2, Bell Communications Research, July 1987.

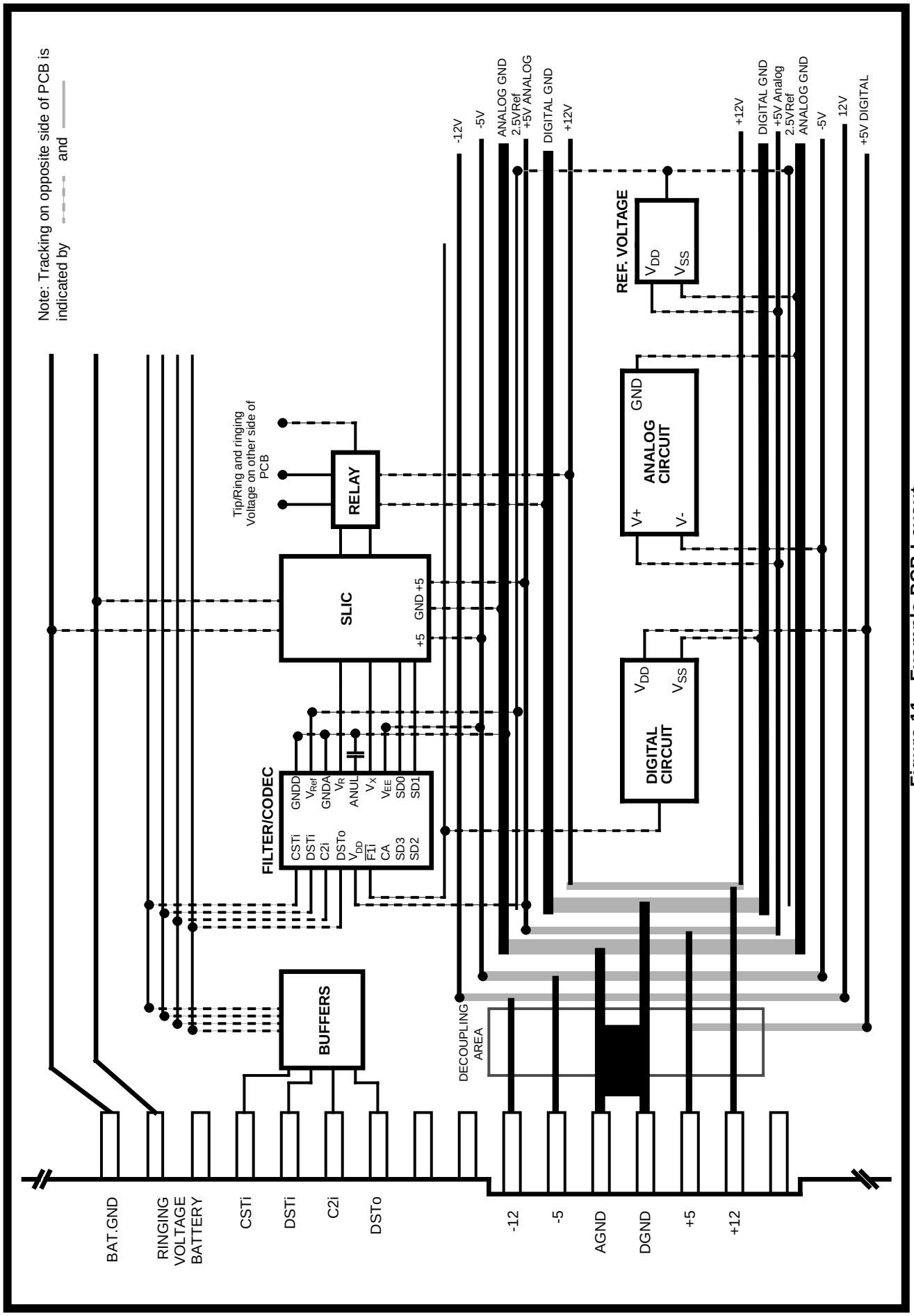

Figure 11 - Example PCB Layout

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