Application Note MSAN-122
Approaches to Digital Line Car Design

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1.0 Introduction

Two devices manufactured by Zarlink allow easy implementation of digital line cards utilizing existing twisted-pair wire. These devices, the MT8952B HDLC Protocol Controller and the MT8972B/71B Digital Network Interface (DNIC), can provide a link with a loop attenuation of up to 33 dB (4.0 km on 24 AWG @ 160 kbit/s) consisting of two 64 kbit/s B-channels and one 16 kbit/s signalling D-channel. The D-channel signalling information is formatted in HDLC protocol.

This note is intended to show a typical application in a private network environment - that found behind a PABX. The note will show, in particular, how the HDLC Protocol Controller can be used as a D-channel interface in a digital line card comprised of multiple DNICs. Three basic approaches are presented and are intended to give the telecommunications engineer a starting point for the development of his/her application. In addition, a design approach is presented for special-feature digital telephones/datasets for use at the far end of the link.

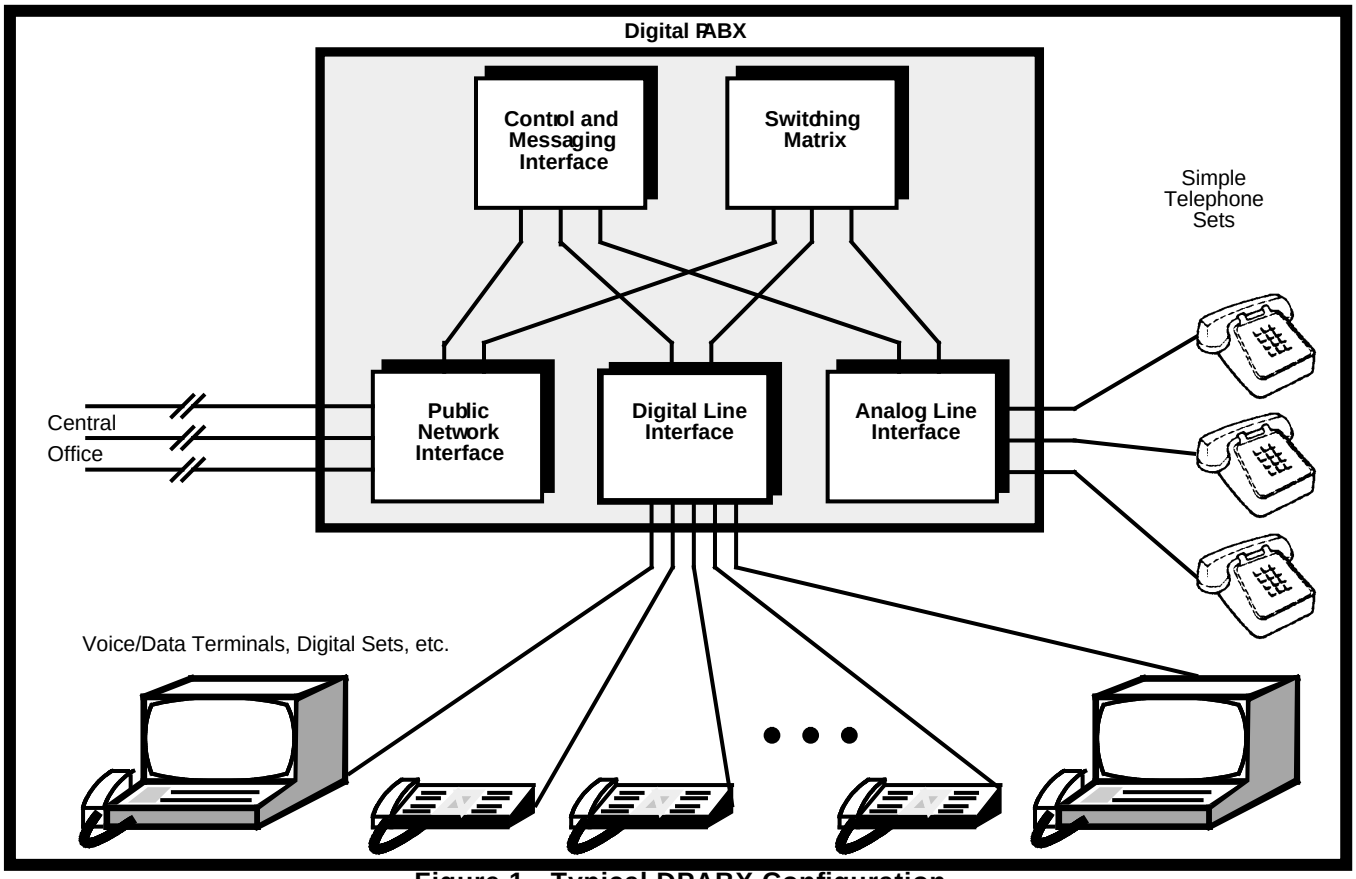

Figure 1 - Typical DPABX Configuration

Figure 1 illustrates a typical PABX configuration comprising an interface to the central office (public network) and interfaces to simple analogue telephone sets, feature-rich digital sets and data terminals. This application note will concentrate on the block labelled 'Digital Line Interface'.

Using the suggestions presented here and the unlimited possibilities offered by two clear 64 kbit/s channels and a 16 kbit/s channel over a simple analogue telephone line, PABX designers can design and offer advanced features in their PABX's previously considered impossible.

2.0 General Description

As a model for a high speed digital link, Figure 2 shows a configuration consisting of an interface for voice/data channels and an interface for a signalling channel. The Digital Network Interface Circuit (MT8972B/71B) and the HDLC Protocol Controller (MT8952B) integrate these two functions respectively.

Voice and/or data arrives at the digital line interface as two 64 kbit/s channels embedded in a 32 channel time division multiplexed stream known as the ST-BUS. Control and signalling information arrives at the signalling interface in parallel mode, perhaps from a local µP. This signalling information is then converted to ST-BUS format for input to the digital line interface.

The signalling channel and the voice/data channels are combined and then adapted for transmission on a single twisted-pair wire. One end of the link, the master, sources clock information while the slave end extracts this clock from the line.

The following provides a brief technical description of the MT8952B HDLC Protocol Controller and the MT8972B/71B Digital Network Interface Circuit (DNIC).

2.1 MT8952B General Description

The MT8952B HDLC Protocol Controller formats packets of information in accordance with ISO HDLC and Layer 2 of CCITT X.25 recommendations. It delimits and synchronizes frames using a unique eight bit Flag sequence (01111110). It also performs a cyclic redundancy check (CRC) on the data and inserts this into the packet prior to the closing flag. In order to ensure the flag sequence is not mimicked, the MT8952B inserts zeros after five consecutive ones have been transmitted. It then extracts these upon reception making the zero-insertion/deletion function transparent to the user. The packet structure is shown in Figure 3.

The MT8952B is capable of generating and detecting the various line states defined by HDLC protocol as well as other defined sequences. The device will generate and detect idle state (15 or more consecutive 1s), interframe time fill (continuous flags), abort sequence and a special Go-Ahead (GA) nine bit sequence (011111110). This special GA sequence is not defined as part of the ISO HDLC protocol but is very useful in some applications as will be shown in this note.

Functionally, the MT8952B may be regarded as a FIFO structure interfacing between a parallel µP bus and a serial bus. The transmit and receive FIFO's are both 19 bytes deep. Information loaded into the Tx FIFO will have the framing flags and the CRC automatically appended to it for transmission on the serial bus. Information arriving at the serial input has

FLAG	DATA FIELD	CRC	FLAG
1 BYTE	n BYTES (n ≥ 2)	2 BYTES	1 BYTE

Figure 3 - HDLC Frame Format

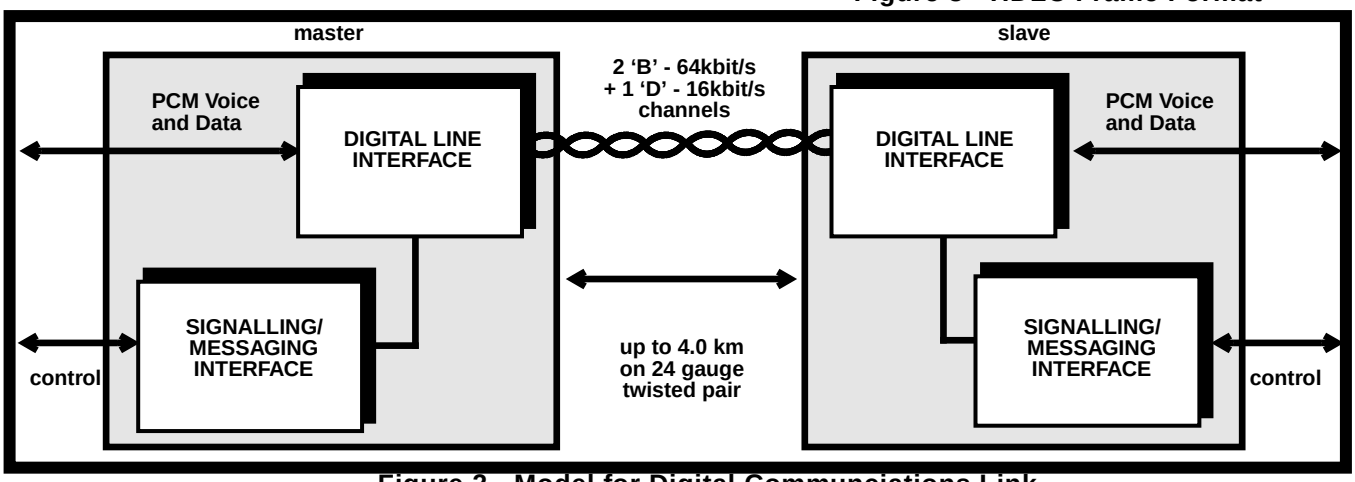

Figure 2 - Model for Digital Communciations Link

the frame structure stripped from the data before it is loaded into the Rx FIFO. Figure 4 provides a functional interface diagram showing the signals associated with the different ports. The MT8952B is controlled by a number of internal registers accessed via the parallel port.

The serial port can be configured in two ways depending on a bit in the Timing Control register. It can transmit/receive packets on selected timeslots in ST-BUS format or it can, using enable signal $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$, transmit/receive packets at a bit rate equal to the clock input CKi.

In the first mode called the 'Internal Timing mode' packets are shifted in/out serially in ST-BUS format using the timing signals $\overline{\text{F0i}}$ and $\overline{\text{C4i}}$/C2i. The number of bits and the timeslots on the ST-BUS during which the packets are shifted in/out are determined by bits in the Timing Control register. In this mode, the transmitter and receiver are both active at the same time and are therefore not independent as in the 'External Timing mode'. In the 'Internal Timing mode' the µP can access two registers called C-channel control/status. The device outputs the information stored here during ST-BUS channel 1 and conversely stores the information arriving during this channel in the status register. This feature is particularly useful when the MT8952B is used with the DNIC since it provides direct access to the DNIC's control/status channel.

In the External Timing mode the transmit and receive sections operate independently and are controlled by $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$ pins. These can be enabled during desired bit/channel times to allow the device to either transmit or receive packets in predetermined channel designations. As well, two pins labelled TEOP and REOP provide high going signals of one bit duration which indicate the completion of a packet transmission or reception respectively. These 'end of packet' signals are useful in multiplexing several data links onto a single HDLC Protocol Controller.

The µP port allows parallel data transfers between the Protocol Controller and a µP. This interface consists of the data bus (D0-D7), the address bus (A0-A3), E clock, chip select ($\overline{\text{CS}}$) and R/$\overline{\text{W}}$ control. As well, an open-drain $\overline{\text{IRQ}}$ pin allows the MT8952B to interrupt the µP on certain conditions as set up by the Interrupt Flag register and the Interrupt Enable register.

Complete technical data for the HDLC Protocol Controller can be found in the MT8952B Data Sheet.

2.2 MT8972B/71B General Description

The MT8972B/71B Digital Network Interface Circuit (DNIC) is a multi-function device providing a high speed full duplex digital transmission link over a single pair of twisted wires. The DNIC interfaces two serial ports to a high speed line port which may be operated at either 80 or 160 kbit/s. The application in which it is used here requires transmission at 160 kbit/s. It may be driven by a fixed external timebase or it may extract the timebase from the line depending on whether it is in master or slave mode.

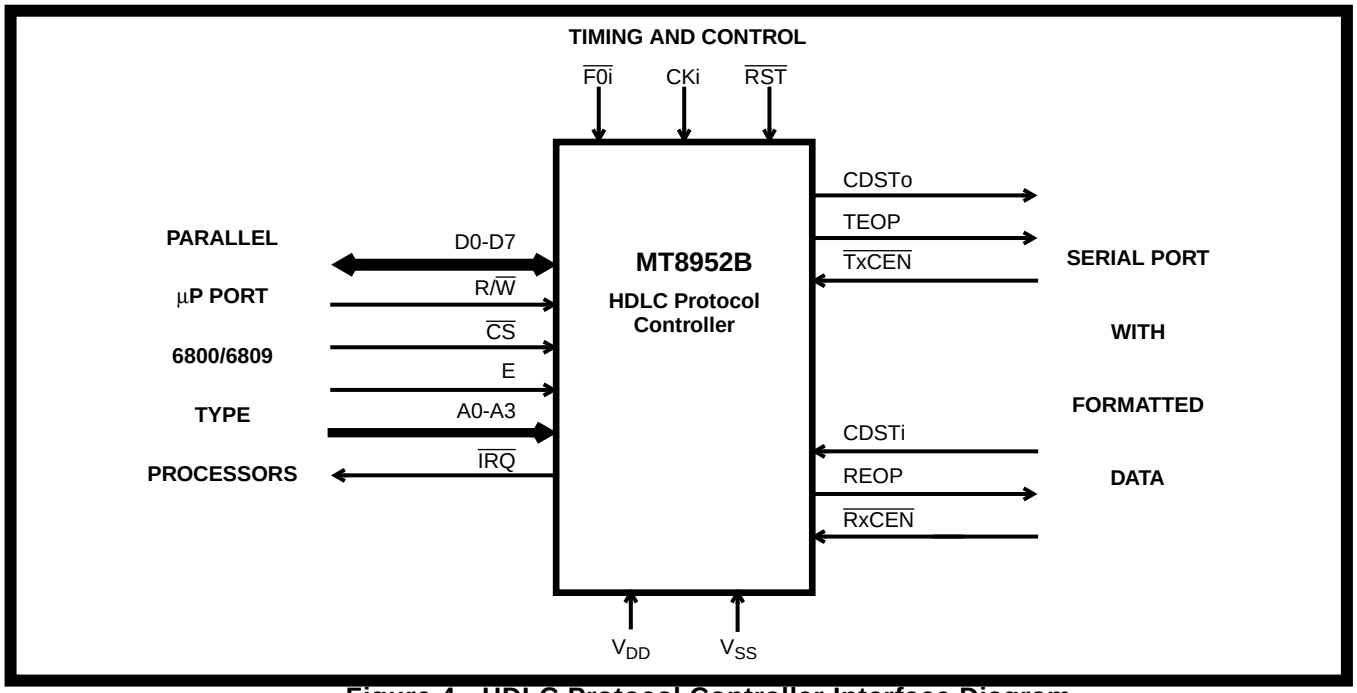

Figure 4 - HDLC Protocol Controller Interface Diagram

At the line port the DNIC supports the 2B + D channel format (two 64 kbit/s B channels, one 16 kbit/s D channel) over two wires as recommended for emerging ISDN 'U' reference standards. The other two ports on the device are in ST-BUS format. These ports are known as the DV and CD ports and are used to deliver the data/voice information and the control/data information respectively.

A functional interface diagram of the DNIC is shown in Figure 5. The DNIC has various modes of operation which are selected using the mode select pins MS0-2. In this application the DNIC is configured for Digital Network mode in which the information arriving at the CD and/or DV ports is in ST-BUS format. In Digital Network mode it may be further configured for Dual Port mode or Single Port mode. The B1 and B2 channels arrive at the DV port (DSTi/DSTo) while the C and D channels arrive at the CD port (CDSTi/CDSTo) in dual port mode. The B1/B2 channels are active during channels 0 and 16 respectively as are the C and D. In single port configuration the information is combined into one serial stream and arrives at the DV port (DSTi/DSTo) only. In this mode channels D, C, B1 and B2 are active during timeslots 0, 1, 2 and 3 respectively.

In order to connect more than one DNIC to the same ST-BUS stream, an $\overline{F0o}$ signal is generated which is a delayed frame pulse output. This signal is useful for 'daisy-chaining' several devices together in line card applications. With this arrangement, only the first DNIC would receive system $\overline{F0i}$ and subsequent DNIC's would be enabled after its predecessor has finished accessing the ST-BUS.

Complete technical data for the Digital Network Interface Circuit can be found in the MT8972B/71B Data Sheet.

3.0 Digital Line Card Implementation

Using the HDLC Protocol Controller and the DNIC one can easily implement digital line card solutions using various approaches. The choice of approach will depend on criteria such as system response time, cost and circuit card density desired. Presented below are the three basic approaches to implementing a line card using the MT8952B and the MT8972B/71B.

Expanding on the notion of a digital link presented in Figure 2, Figure 6 provides a functional representation of a line card consisting of several of these links. Each Digital Line Interface requires a source for the voice/data 64 kbit/s channels. This will originate elsewhere in the system hierarchy and will be interfaced via the block labeled 'PCM Voice/Data Interface' which is typically no more than a buffering mechanism. The bus structure used to transport these channels will be the ST-BUS.

The next block, labelled 'Control and Messaging Interface', is the one on which this application note focuses. It is the source of the Messaging information supplied to each line. The messaging channel utilizes HDLC format for error-free communications and can be implemented in one of three ways. The first uses a dedicated HDLC transceiver per line circuit and the last two share the

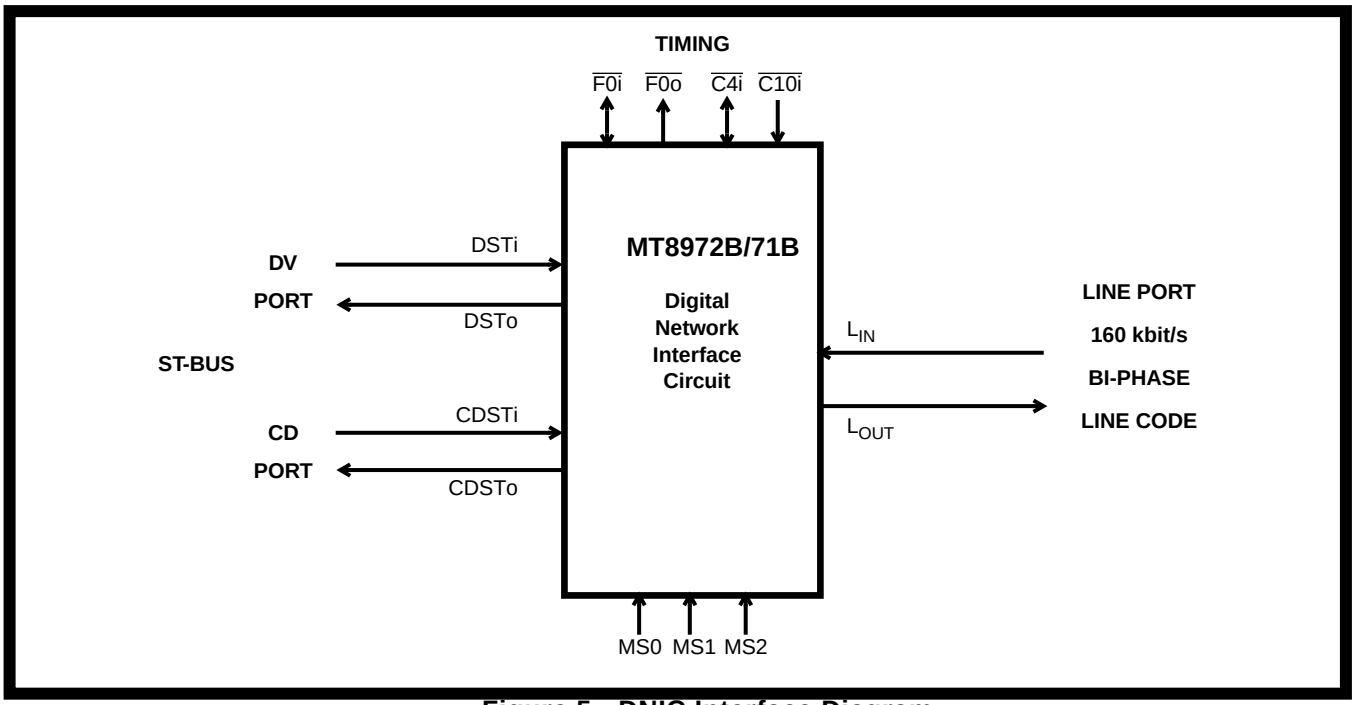

Figure 5 - DNIC Interface Diagram

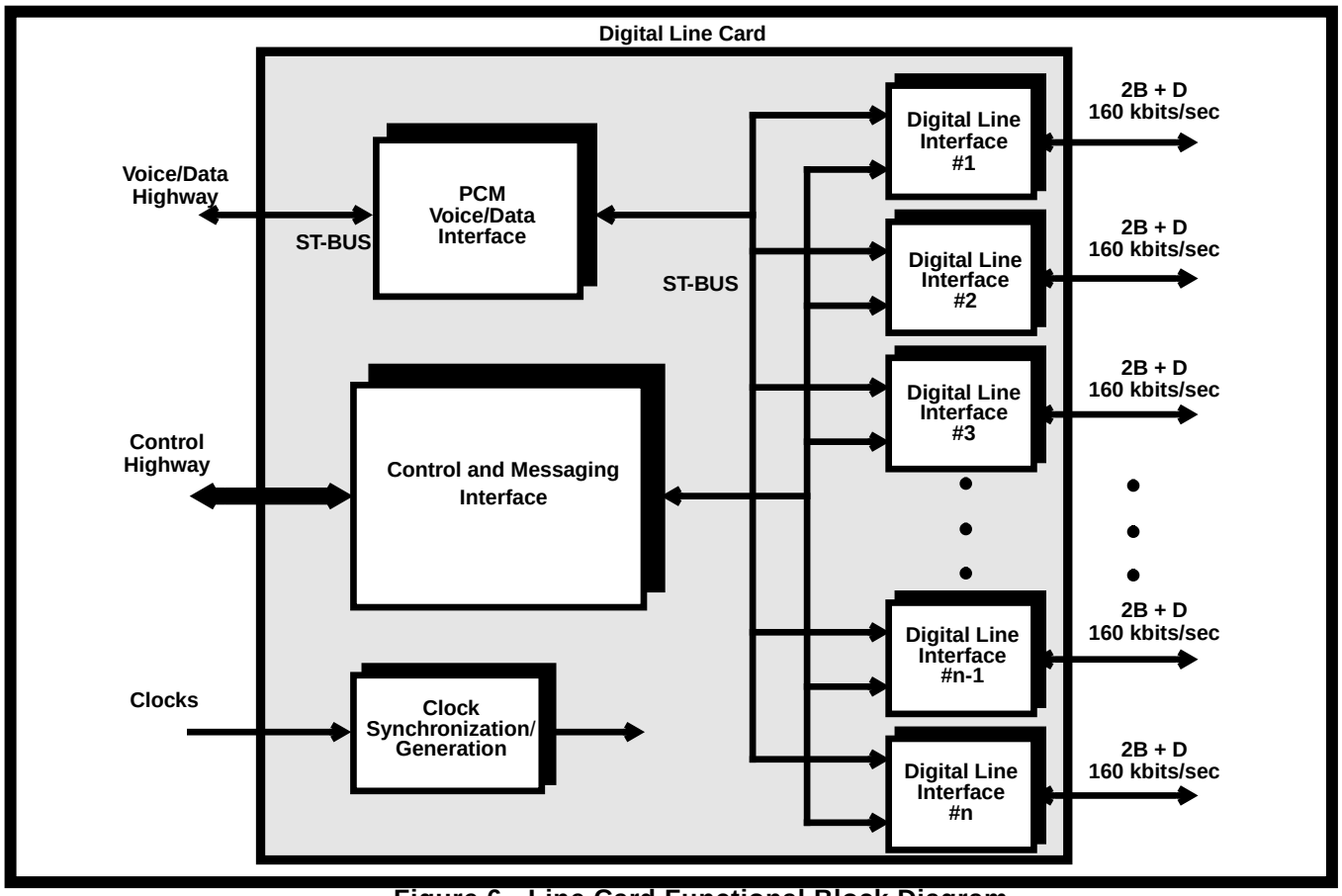

Figure 6 - Line Card Functional Block Diagram

resources of one HDLC transceiver over a number of lines. The second and third methods are feasible since messaging information is generally sporadic in nature and, when combined and queued, can be handled by a single non-dedicated device.

Section 3.1 provides an example of a dedicated HDLC transceiver per line circuit application while sections 3.2 and 3.3 provide two examples of time-shared HDLC transceiver resources. These examples illustrate the basic interconnection of the MT8952B with the MT8972B/71B and their utilization of the ST-BUS.

In Figure 6 the block titled 'clock synchronization/ generation' provides a phase-locked clock source to each of the digital line interfaces for synchronization with the system. Actual implementation of this block is shown in Figure 8.

3.1 Dedicated HDLC Interface Per Line

This method, as stated earlier, allocates a dedicated HDLC transceiver per line circuit. Figure 7 shows the typical inter-connection of the devices.

In this setup the MT8952B is used in the internal timing mode and is programmed to output the HDLC D-channel in ST-BUS channel 0. In addition, the µP has access to each DNIC's control channel through the MT8952B C-channel registers. This C-channel is active on the ST-BUS during timeslot 1. The MT8952B is shown using $\overline{C4i}$. However, in internal timing mode it may alternatively be programmed to use C2i clock.

The DNIC in this case is operated in single port, digital network mode as shown in Figure 16. In this mode the DNIC expects the D and C channels to be active during ST-BUS timeslots 0 and 1, respectively. It also expects B1 and B2 channel information to be present on channels 2 and 3, respectively. The B1 and B2 channels arrive at and depart from the line card at STi and STo.

This approach connects all devices to the same ST-BUS serial link by making use of the delayed frame pulse ($\overline{F0o}$) from the DNIC. In single port, digital network mode the DNIC supplies a frame pulse output at the end of channel three. This is used to activate the next DNIC to retrieve information from the ST-BUS during the subsequent four channels. In this application, this signal is also supplied to the next HDLC Protocol Controller so that it will activate its D and C channels exactly four channels after the previous HDLC device in the chain. Using this approach, up to eight digital lines with corresponding

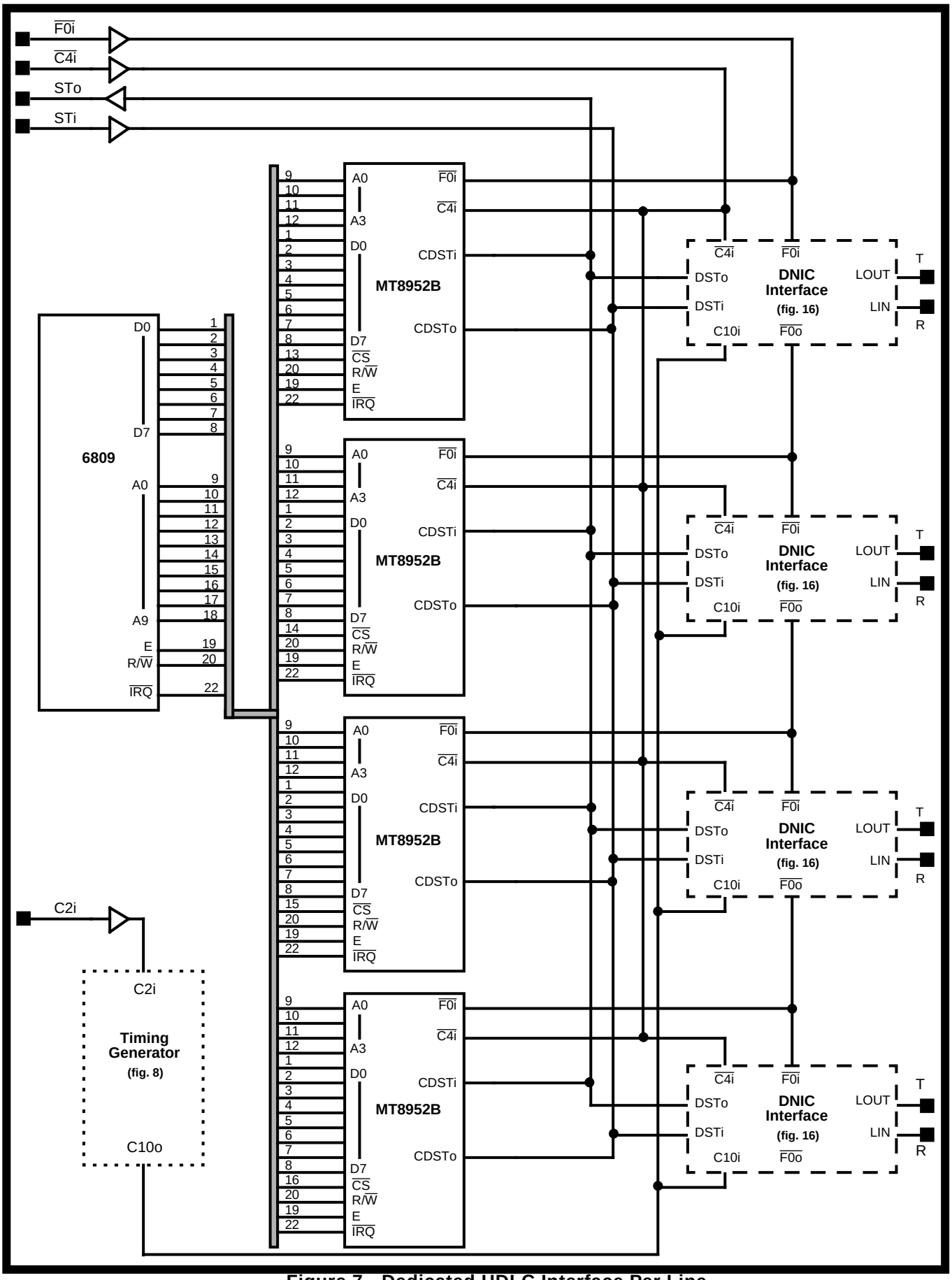

Figure 7 - Dedicated HDLC Interface Per Line

dedicated MT8952Bs may be supported by one ST-BUS link. The resulting composition of the link is shown in Figure 9.

It is important to note that the HDLC device, while not transmitting, is in a high impedance state allowing a different source to drive the B1 and B2 channels. Likewise, in this application, it is imperative that the source of the B1 and B2 composite stream also go into a high impedance state whenever one of the MT8952Bs is active on the ST-BUS. If the B1 and B2 channels are driven directly from a MT8980 Digital Crosspoint Switch this task is made easy since the MT8980 can be programmed to go into high impedance during selected channels. If buffer circuits are driving the ST-BUS at this point, special consideration must be given to disabling these during the appropriate channels.

While this method is the more costly of the three approaches presented in this note, it is by far the fastest in terms of system response time and has the greatest flexibility. In this case, system response time is largely determined by the operating speed of the µP and the software which is driving it since the concentration of information is done at the µP interface. With this setup, full advantage of the MT8952B's 19 byte FIFO buffers may be realized since messages may be sent and received without waiting for queued requests and go-aheads as required in a shared resource scheme. The D-channels may be operated in the Asynchronous Balanced mode (ABM) as defined by ISO HDLC. Further savings in speed are possible since response to incoming messages can be interrupt driven.

3.2 Shared HDLC Resource - Method #1

In this scheme a single HLDC Protocol Controller is time-shared between up to eight digital line circuits. Figure 10 illustrates a schematic representation of

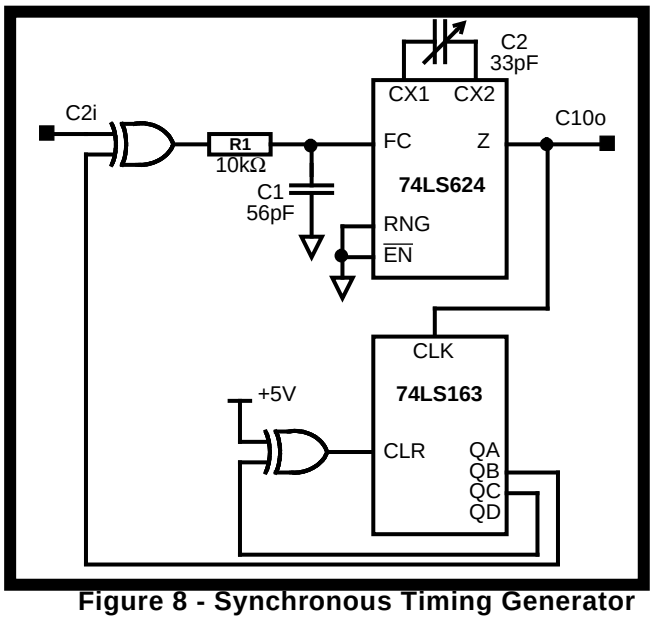

Figure 8 - Synchronous Timing Generator

this method. The time sharing is accomplished using the MT8981 Digital Crosspoint Switch (DX).

Under control of a µP, the MT8981 is used to connect the MT8952B, in succession, to each DNIC's D-channel at a predetermined regular interval. The B1 and B2 channels arrive at the line card at STi1 and terminate at DX link STi1 where they are routed to STo2. Figure 11 shows an arbitrary arrangement of the incoming STi1 stream in which the B1 and B2 channels for each of eight line circuits are packed into the first 16 ST-BUS channels. The D-channel information originating at the MT8952B arrives at DX link STi3 in channel 0. This is also routed to STo2 and into the channel corresponding to the line circuit selected to receive the packet. In Figure 11, the D-channel arriving at STi3 is shown arbitrarily switched to channel 8 which corresponds to line circuit #3. The C-channels used to control the DNICs can be accessed from the parallel port of the DX by putting channels 1, 5, 9, 13, 17, 21, 25, 29 of link STo2 into message mode (see MT8981 Data Sheet). This combines the C-channel information with the B1, B2

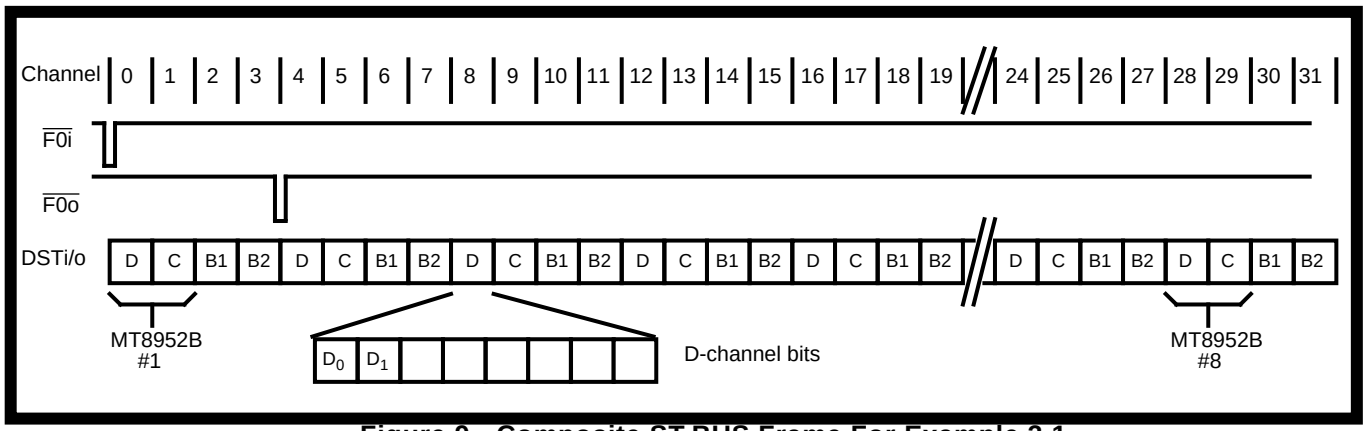

Figure 9 - Composite ST-BUS Frame For Example 3.1

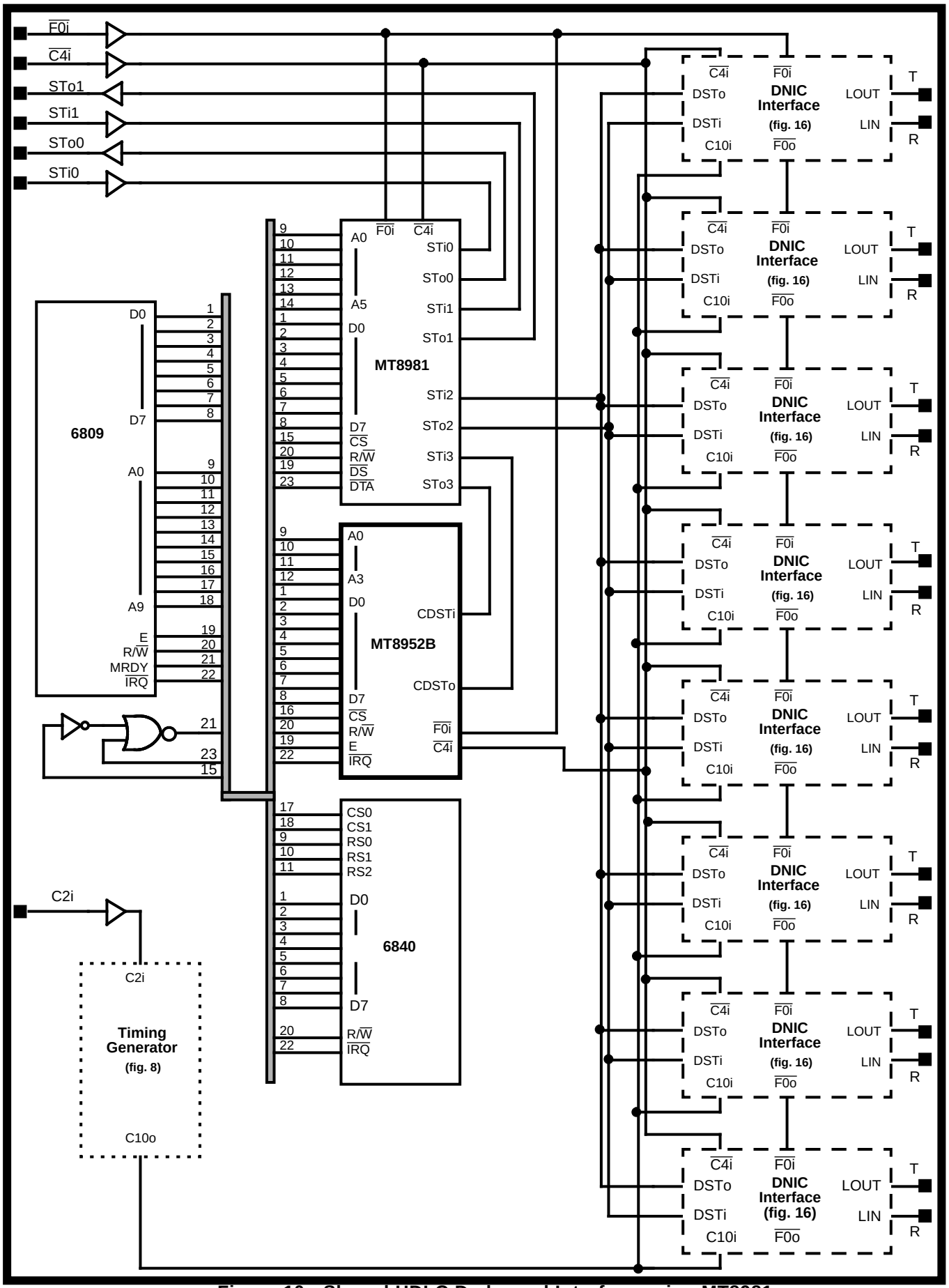

Figure 10 - Shared HDLC D-channel Interface using MT8981

and D-channels at the composite STo2 output link. When accessing the DNIC registers from the DX, however, the DNIC register bit assignments are reversed. This is due to the fact that the DX outputs the MSB first while the DNIC expects to receive the LSB first.

On the receive side, the B1 and B2 channels arriving at DX input link STi2 from the line circuits are routed to STo1 and leave the card edge at STo1. The D-channel from the selected receive line circuit is routed to channel 0 of STo3 so that the MT8952B may receive it. The DX's data memory can be used to read the C-channel status from STi2 channels 1, 5, 9, 13, 17, 21, 25, 29 .

As in the previous example of 3.1, the HDLC Protocol Controller is used in internal timing mode and the DNIC is used in single port, digital network mode. The MT8952B is programmed to output and accept D-channel information on ST-BUS channel 0 at a rate of 16 kbit/s or 2 bits/frame. Although the MT8952B, in this mode, has its C-channel active in timeslot 1 this is ignored since each DNIC C-channel must have a dedicated interface. As mentioned above, these are accessed through the DX.

Each DNIC D-channel is active in the first timeslot relative to its received frame pulse. As in example 3.1, DNICs are 'daisy-chained' together utilizing the $\overline{F0o}$ which, in single port, digital network mode, occurs after completion of channel 3. The composite ST-BUS stream, STo2, sent to all DNIC's is shown in Figure 11 with the D-channel active for DNIC #3. Notice that the 7 remaining inactive DNIC D-channels transmit an 'all-ones' pattern. This is recognized in HDLC as an idle channel state and can be accomplished by connecting the inactive Tx channels via the DX to an 'all ones' pattern originating elsewhere.

This method employs a polling scheme which makes use of the various link states defined in HDLC as well as the GO-AHEAD (GA) sequence incorporated into the MT8952B. Normally, incoming and outgoing D-channel links will be in an idle state. If the µP wishes to transmit a packet of information to a peripheral unit it simply connects channel 0 at DX STi3 to the channel at STo2 corresponding to the desired peripheral. The µP then loads it's message into the MT8952B transmit FIFO in the normal manner. When transmission is complete, the channel at STo2 is then returned to an 'all-ones' idle state.

The GA sequence and polling technique are used when receiving messages. Normally all peripheral units will be in idle state. The DX, under µP control, will sequentially connect the HDLC's receiver to each DNIC's incoming D-channel. The HDLC receiver will stay connected to this incoming channel for a specified time 'listening' for a GA sequence which is raised by a peripheral as a request-to-send. Since the GA sequence is nine bits long, including a shared 0 between sequences, the 'listening' time must be at least 16 bits long in order to detect the sequence in a bit oriented protocol. Since two bits are received per frame, this corresponds to eight frames or 1.0 msec which the HDLC must remain connected to the incoming D-channel before proceeding to the next incoming D-channel. This timeout function may be realized with a hardware timer such as the 6840 as shown in Figure 10.

When a peripheral sends a GA sequence and the HDLC Protocol Controller eventually detects this state, it raises the GA flag in the Interrupt Flag

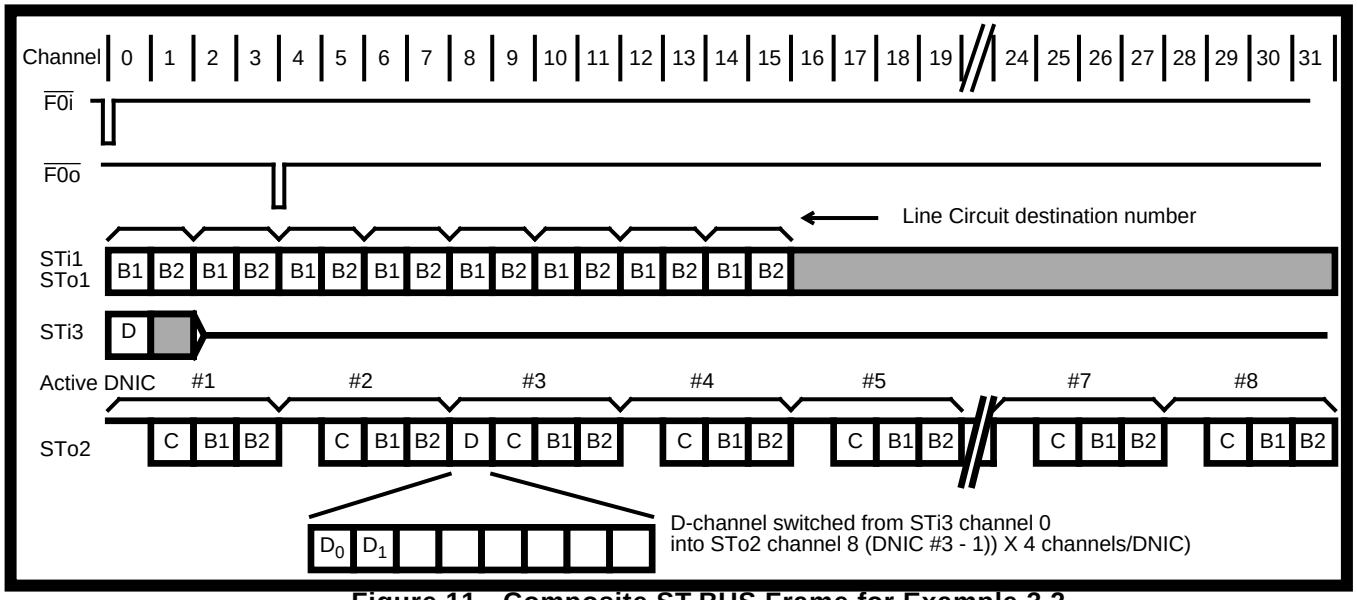

Figure 11 - Composite ST-BUS Frame for Example 3.2

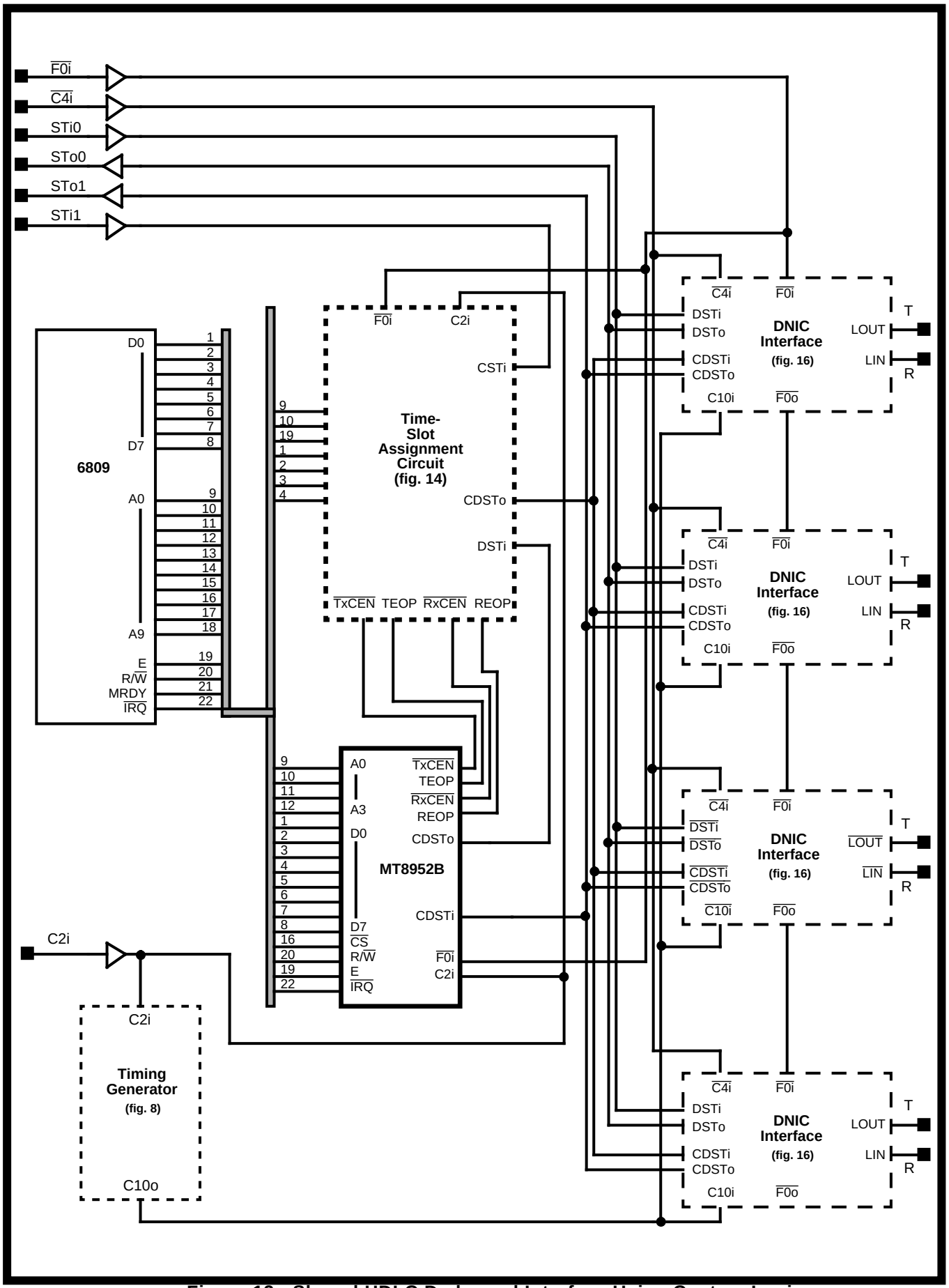

Figure 12 - Shared HDLC D-channel Interface Using Custom Logic

register. This may also trigger an interrupt. If this occurs the timeout function is suspended and the DX is programmed to connect the HDLC transmitter to the corresponding peripheral. The HDLC transmitter is then put into GA state signalling back to the peripheral that it may proceed with transmission of its packet. Once the entire packet has been received the timeout function would be enabled and the polling routine restarted.

This method is more software intensive than the other methods and is better suited to line cards of eight lines or less. System response time becomes primarily a function of the length of the messages and the number of line circuits (up to a max. of eight) the HDLC Protocol Controller must service. In this approach message packets should therefore be limited in size. For example, given eight line circuits and limiting messages to 16 bytes, the worst case system response time would be approximately 100 msec. (Worst case refers to every line requesting to send a maximum length message.) This takes into account the time required for polling, the GA response, the actual information transfer and the associated frame structure.

From a hardware standpoint this approach is a simple and relatively inexpensive implementation of the line card function. In cases where the size of the line card is small, the complexity of messages is not too great and/or the system response time is not overly critical this method will provide a suitable solution.

3.3 Shared HDLC Resource - Method #2

The significant differences between the previous Shared HDLC Resource method and this method are the operating modes of both the DNIC and the HDLC Protocol Controller and the way in which the timeslot assignment is accomplished. In this method the MT8952B is used in External Timing mode and the DNIC is used in dual-port, digital network mode. The multiplex timing for the HDLC channel is performed by custom circuitry represented by the block labelled 'Timeslot Assignment Circuit' in Figure 12.

The MT8952B transmit and receive sections, in External Timing mode, are independently controlled by the hardware pins $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$, respectively. To assist in multiplexing, the MT8952B outputs TEOP and REOP to indicate when it has finished transmitting or receiving a packet. These four signals make the multiplexing task performed by any custom circuitry relatively simple to implement.

The DNIC, as mentioned earlier, is used in dual-port mode. The B1 and B2 channels are input/output at DNIC port DSTi/DSTo in timeslots 0 (B1) and 16 (B2) relative to $\overline{\text{F0i}}$. The D and C information is input/output at port CDSTi/CDSTo on channels 0 (C) and 16 (D). In this application, as in the others presented here, the DNICs are 'daisy-chained' together using the delayed frame pulse output $\overline{\text{F0o}}$. In dual-port mode the signal $\overline{\text{F0o}}$ comes at the end of channel 0. Supplying this to the next DNIC in the chain skews its active channels by one channel time.

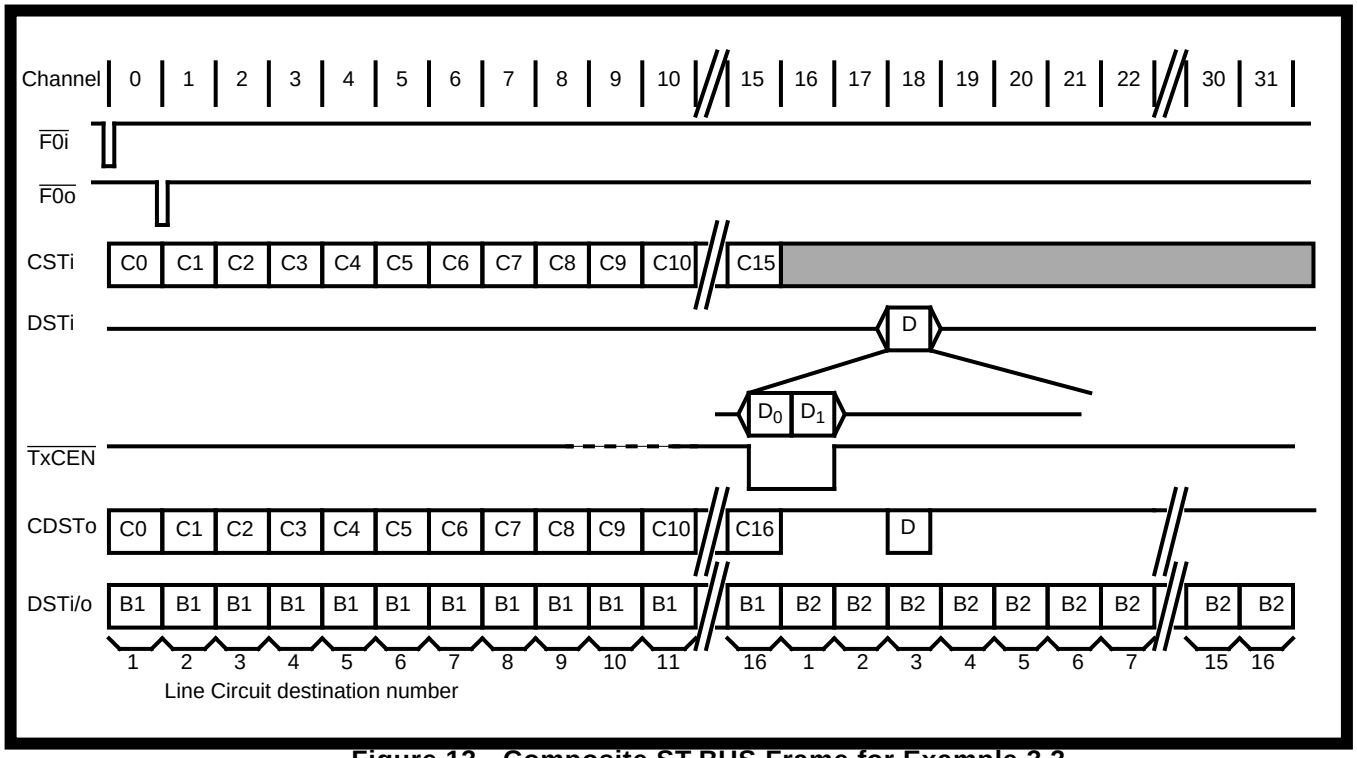

Figure 13 - Composite ST-BUS Frame for Example 3.3

Since two ST-BUS links are used to support these 'daisy-chained' DNICs, up to 16 line circuits may be served by one HDLC Protocol Controller with this configuration.

As pointed out previously, the block labelled 'Timeslot assignment circuit' multiplexes the D-channel, originating at the HDLC Protocol Controller, and the C-channels into a common output stream. Figure 14 shows a typical implementation of this circuit. At the microprocessor bus, transmit and receive addresses between 0 and 15 are latched indicating the line circuits to which the HDLC transmitter and receiver are to be connected to respectively. C2i and $\overline{F0i}$ are input to a series of counters which in turn supply a two-bit-wide bit count, an incrementing channel count and a half-frame signal used to divide the ST-BUS into two. When the channel count matches the latched Tx or Rx address the comparator output will go active. This signal, gated with the bit count and the half-frame count produces $\overline{TxCEN}$ or $\overline{RxCEN}$ to enable the HDLC transmitter or receiver for precisely two bit periods during the appropriate channel. C-channel and D-channel information destined for the line circuit are also fed through a simple multiplexer controlled by $\overline{TxCEN}$ and the half-frame count. This does the actual merging of the outgoing D and C channel information and can be designed in such a way as to produce a high ('all-ones') pattern on the unused D-channels.

Figure 13 shows the composition of the ST-BUS in the transmit direction. B1 and B2 channels for up to 16 line circuits arrive at the card edge (in Figure 12) at STi0 (and depart at STo0). All DNIC line circuits are connected in parallel to this bus and the channel assignments and line destination addresses are shown as DSTi/o in Figure 13. C-channels for up to 16 circuits originate off card and arrive at STi1. These are input to the timeslot assignment block at CSTi and are assigned to the first 16 channels of the ST-BUS. The D-channel from the MT8952B is input to the Timeslot assignment block at DSTi during the times enable by $\overline{TxCEN}$. These two inputs, CSTi and DSTi, are combined, as shown earlier in Figure 14, to produce CDSTo which is then routed to the DNICs. The composition of CDSTo is shown in Figure 13 with the D-channel enabled for line circuit 3 (channel 18).

In the opposite direction, C-channel information arriving from the line circuits leaves the card edge at STo1 in the first 16 channels. The MT8952B,

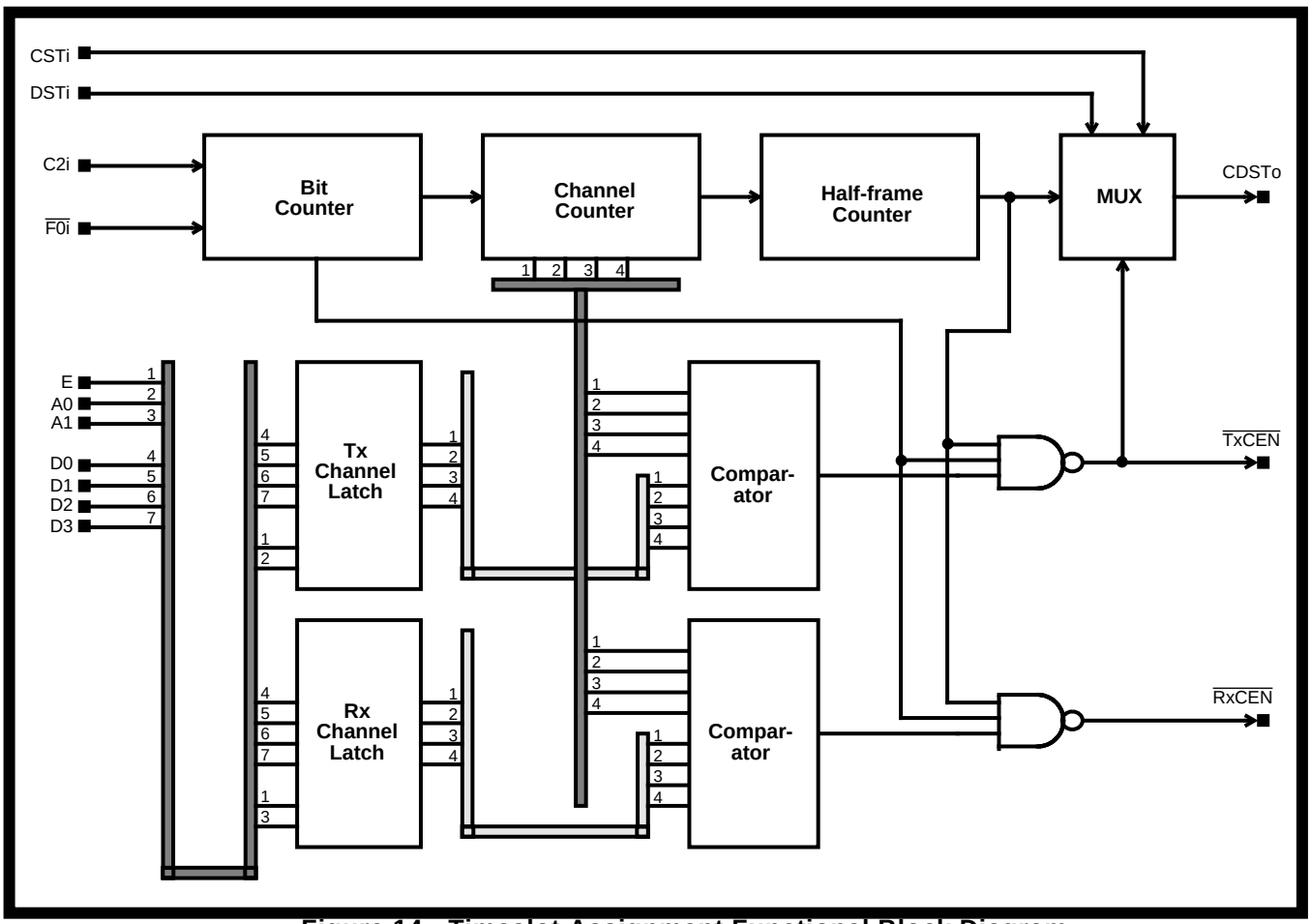

Figure 14 - Timeslot Assignment Functional Block Diagram

enabled by $\overline{\text{RxCEN}}$, receives the active incoming D-channel directly from the same bus.

The protocol used to exchange messages in this method is similar to that used in the previous example 3.2. For messages incoming from the peripheral line circuits the GA sequence and a polling routine are again made use of. If a peripheral requires sending a packet to the system it raises the GA sequence as a request-to-send. The HDLC receiver is switched sequentially among the line circuits listening for the GA sequence. This is done by updating the Rx address in the timeslot assignment circuit Rx latch. When the GA sequence is detected the HDLC transmitter is connected to the corresponding line circuit and acknowledges the request-to-send allowing normal exchange of packets. Outgoing messages, on the otherhand, are transmitted directly to the peripheral selected by latching the Tx address in the time-slot assignment circuit and loading the MT8952B Tx FIFO.

While this method appears very similar to the previous method, the advantage lies in the versatility of the custom designed circuit. Shown here is a simple implementation of some basic functions. However, this implementation could be expanded to include a number of timesaving features by further transferring functionality from software to hardware. Possible implementation could include: using a latch/counter to automatically increment the Rx address; independently generating GA acknowledgements in order to relieve the HDLC of this task and; latching the next receive channel address while looking ahead for other Request-To-Send sequences. These functions could easily be imple-mented using a combination of MSI devices or PALs.

In contrast to the previous example, 3.2, this method allows the designer to move some of the functions performed under software control to hardware which results in faster system response time and software reduction. This method still employs a polling technique and uses the GA sequence to request and acknowledge inbound packet transmission as in 3.2. However, this represents a compromise between ease of implementation, cost and system response time. It also allows larger groupings of line circuits on one line card and allows the designer greater flexibilty in designing in other cost/time saving features.

4.0 Digital Telephone/Terminal

This section is intended to briefly introduce the designer to some basic concepts in designing peripheral equipment for use at the far end of the digital link. This equipment may be special feature telephones with RS-232 data ports, terminals/workstations with integrated voice, etc.

The digital link may be terminated and interfaced at the far end using the same two components as are used at the line card. The HDLC Protocol Controller and the Digital Network Interface Circuit are ideal for use in such applications since they are fabricated in low-power CMOS permitting equipment, in many cases, to be line powered.

Figure 15 shows a simplified implementation of a smart telephone set with a data port configured to accept RS-232 type signals. Here the D-channel is used to signal and provide messages between the set and the system, the B1-channel is used to carry voice at 64 kbits/s and the B2-channel is used to carry the data. The RS-232 data port is interfaced to the ST-BUS using the MT8950 Data Codec while the voice is interfaced using the MT896x Voice Codec. The Data Codec uses Transition Encoded Modulation (TEM) to encode the signal transition relative to the ST-BUS $\overline{\text{F1}}$ signal and provides the 8 bit data on the ST-BUS in the particular channel to which the device is assigned. The Data Codec will encode signals up to 8 kbits/s, 9.6 and 19.2 kbits/s. The timing circuitry provides $\overline{\text{C2}}$ clock for the codecs and generates the appropriate frame pulses to assign the MT8950 to channel 3 and the MT896x to channel 2.

The DNIC is used in Digital Network, single port mode and configured as a slave device. In slave mode the DNIC extracts the timing from the line and provides all ST-BUS clocks to drive the set. The MT8952B, acting as the D-channel interface, is operated in Internal Timing mode. In this mode it transmits/receives its D-channel in timeslot 0 and its C-channel registers in timeslot 1. The DNIC, correspondingly, expects its D, C, B1 and B2 channels to be present/active during timeslots 0, 1, 2, 3 respectively.

In order for the set to transmit messages over the D-channel the µP would simply program the MT8952B into GA mode to signal a request-to-send to the DPABX. Upon recognition of the GA sequence the DPABX would reply with a GA sequence back to the set to indicate the system is ready to accept the message. The MT8952B would then be taken out of GA mode and the packet loaded to the FIFO would be sent. When the set transmitter is idle the MT8952B resides in idle fill state.

Incoming messages from the system arrive asynchronously on the D-channel. The MT8952B,

recognizing the frame structure, indicates to the set µP through an IRQ that an information packet has been received into the Rx FIFO.

As with the line card implementations, digital telephones and special feature terminals can be implemented very easily using the MT8952B HDLC Protocol Controller and the MT8972B/71B Digital Network Interface Circuit.

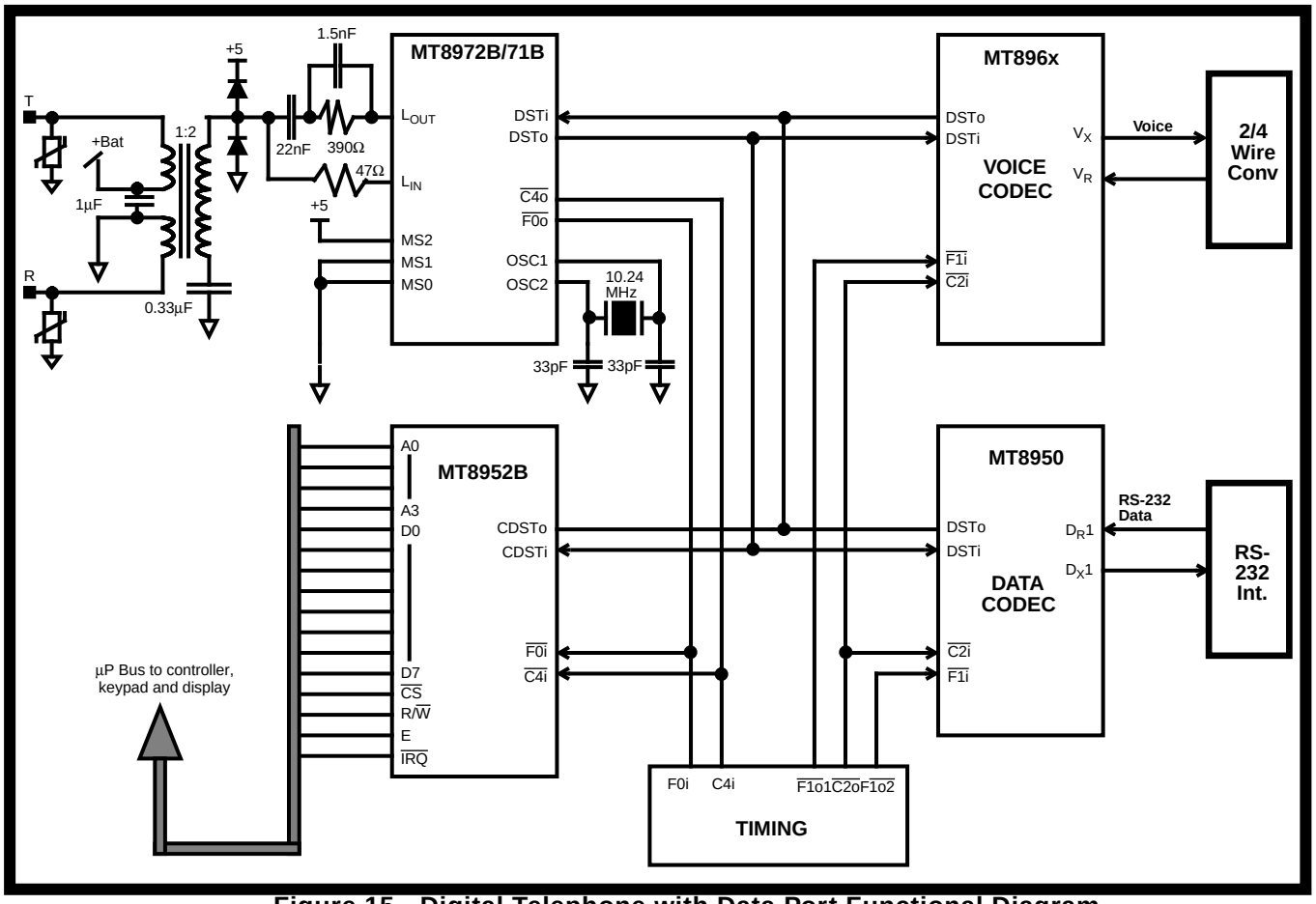

Figure 15 - Digital Telephone with Data Port Functional Diagram

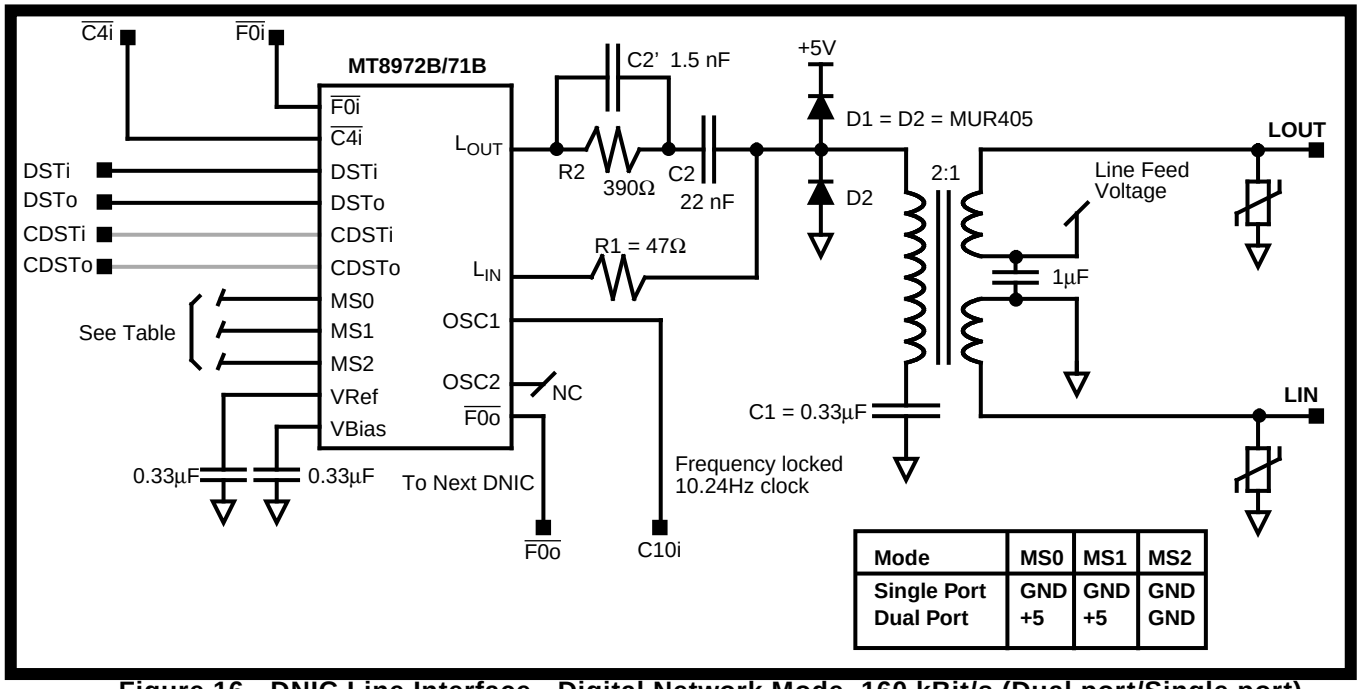

Figure 16 - DNIC Line Interface - Digital Network Mode, 160 kBit/s (Dual port/Single port)

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