ZARLINK SEMICONDUCTOR

Application Note MSAN-128
Implementing an ISDN Architecture Using the ST-BUS

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1.0 Introduction

The concept of the Integrated Services Digital Network (ISDN) originated from the desire to provide integrated services through better use of the bandwidth potential in existing tele-communications subscriber loops (loop plant). Advances in VLSI technology and digital signal processing have made high rate digital transmission to the subscriber's premises not only possible, but also economical. ISDN is the rationalization of the architecture of a telecommunications network to support and utilize this improved capability

One of the cornerstones of the ISDN concept is international compatibility. The CCITT has addressed this requirement by defining a rigid structure for subscriber access to an ISDN, at several reference points. A corresponding set of specifications has been generated facilitating the development of generic subscriber interfaces to ISDN's for all applications. The acceptance and timely implementation of ISDN's will be enhanced by the ubiquitous connectivity provided by such standardized interfaces. Further, the economics of scale and competition will reinforce this trend through reduced costs of implementation. Figure 1 shows the ISDN User Network Access Model.

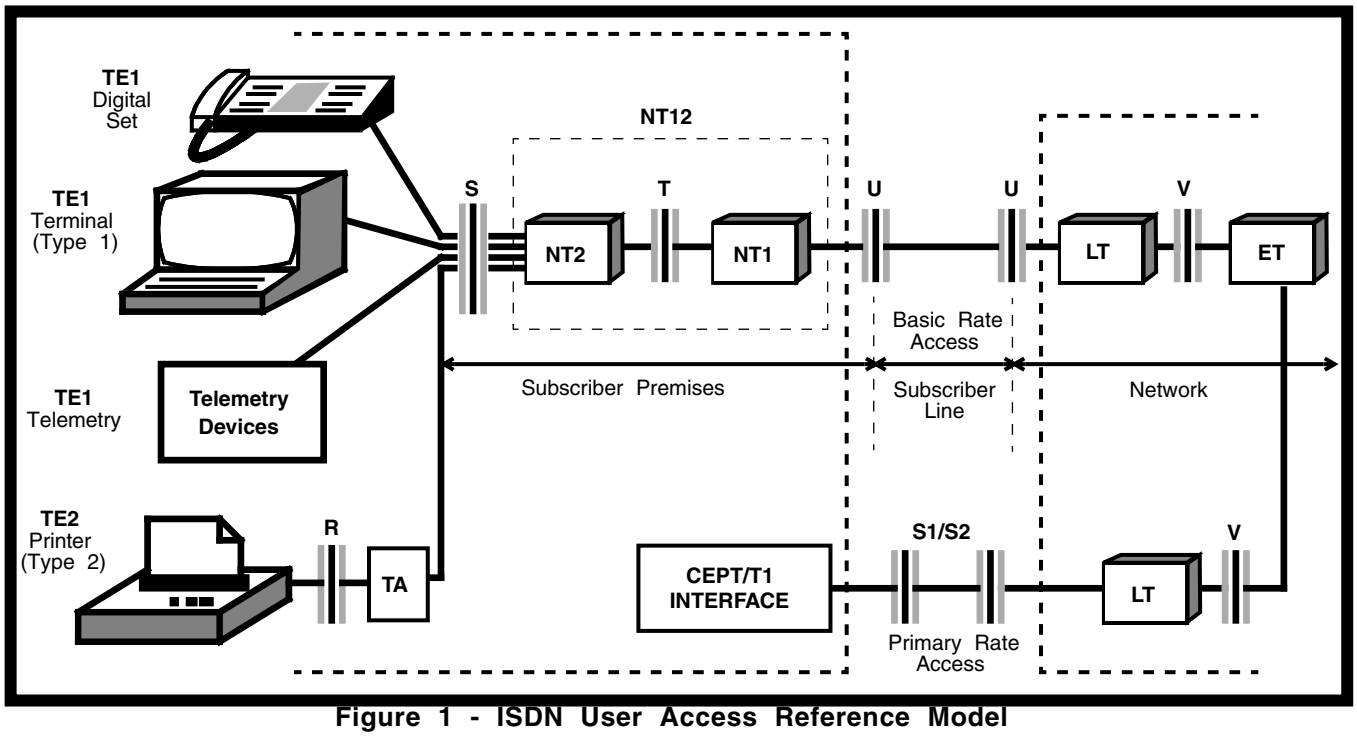

Figure 1 - ISDN User Access Reference Model

As can be seen from Figure 1, there are points in theend-to-end transmission of information through anISDN, where information must change from one typeof transmission scheme to another. These points areat the Terminal Equipment (TE), the NetworkTerminations (NT), the Loop Terminations (LT), theExchange Termination (ET) etc., shown in Figure 1.Rather than create a different interface componentfor each unique type of carrier-to-carrier transition, itis more practical to design an interface betweeneach type of transmission method and someintermediate format.

The intermediate format called for is a commonmechanism to transfer information between theinterface devices. The ST-BUS, developed by Zarlink Semiconductor, is a component interface designedspecifically for this purpose. This application notedescribes the ST-BUS structure as it applies to boththe ISDN model and the ISDN componentsdeveloped by Zarlink Semiconductor. The electricalspecification for the ST-BUS may be found in ZarlinkSemiconductor's data book.

2.0ISDN Information Channels

Information travels on ISDN transmission media inthe form of serial digital data streams. Eachinformation stream can support multiplecommunication channels through Time DivisionMultiplexing (TDM). The CCITT has defined several types of information channels, each with a defined bitrate.

Signalling information, telemetry information and lowspeed packet communications are carried on D-channels, which have a bit rate of 16 kbit/s (D(16))and a bit rate of 64 kbit/s (D(64)). Information thatwill be termed "user information" in this note, iscarried on B-channels, H0-channels, H11-channelsand H12-channels. This information can be circuitswitched data, packet switched data, audio,facsimile, telex or video information. The bit rates foruser information channels are as follows:

a) B-channel : 64 kbit/s
b) H0-channel : 384 kbit/s
c) H11-channel : 1536 kbit/s
d) H12-channel : 1920 kbit/s

The interface between ISDN components mustsupport all the different types of informationchannels. The component interface, therefore, mustuse TDM techniques, based on the 64 kbit/s channelrate common to all channel types. Multiple 64 kbit/schannels can be used to construct the higherbandwidth H0, H11 and H12-channels. At the 16kbit/s rate, the data fits into two bits of a 64 kbit/schannel.The maximum throughput supported by the currentrecommendations is 2048 kbit/s (32X64 kbit/s

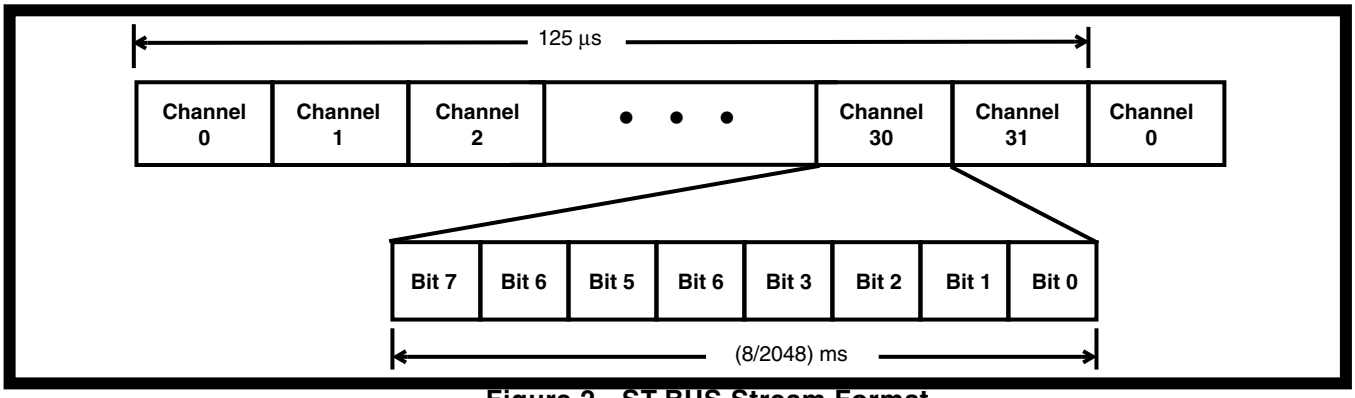

Figure 2 - ST-BUS Stream Format

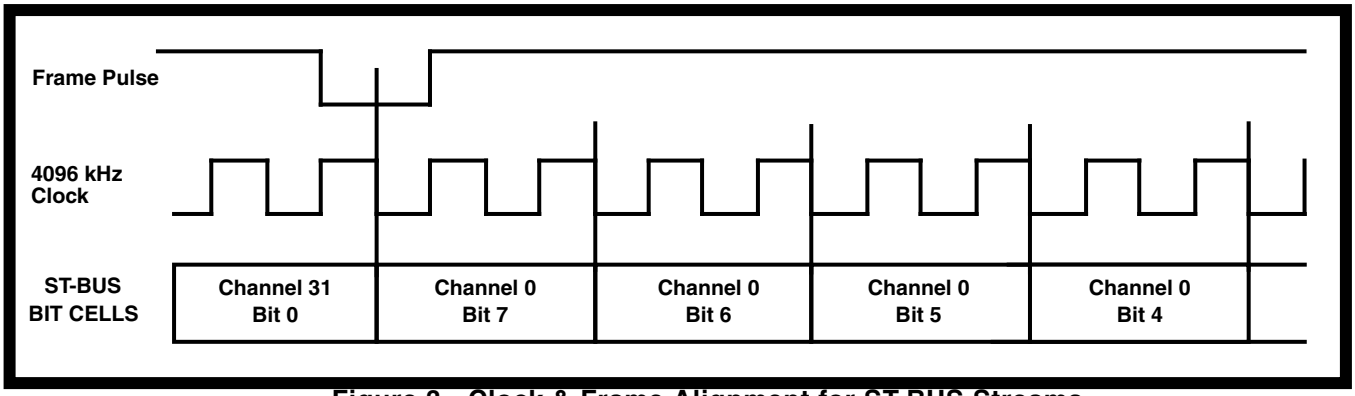

Figure 3 - Clock & Frame Alignment for ST-BUS Streams

channels), specified at the 2048 kbit/s S1 reference point (I series recommendation I.431). The capacity of the component interface should encompass the bandwidths required by all current reference point specifications, implying that the minimum number of 64 kbit/s channels supported by the component interface should be 32. This philosophy allows for maximum connectivity between all types of ISDN interface components.

3.0 ST-BUS Frame Structure and Nomenclature

The ST-BUS is a synchronous TDM serial bussing scheme, with data streams operating at 2048 kbit/s, configured as 32, 64 kbit/s channels (Figure 2). This rate and channel structure makes the ST-BUS compatible with all narrowband ISDN transmission bit rates. 64 kbit/s channels may be concatenated to form the higher rate channels.

Synchronization of the data transfer is provided by a frame pulse, which identifies the frame boundaries and repeats at an 8 kHz rate. Figure 3 shows how the frame pulse defines the ST-BUS frame boundaries. All data is clocked into the device on the appropriate edge of the clock signal.

ST-BUS nomenclature uses the device as the reference for information flow direction. ST-BUS streams input to a component are named STi (ST-BUS input). ST-BUS streams output from a component use the same conventions except that the “i” suffix is replaced by an “o” suffix eg. STo. If there is more than one input or output ST-BUS stream, there may be a number appended to the end of the input names eg. STi0, or STi1. If the type of information on an ST-BUS stream is important, the name of the input may be preceded by a D (for information to be processed eg., DSTi2) or a C (for component control information eg. CSTi0).

Component control is easily integrated into the ST-BUS architecture. The advantage of using ST-BUS streams for control/status information is that the same means for transporting user information through network equipment can be used for the control/status information. The same principles that make serial TDM information transportation beneficial in the ISDN (physical media savings, power consumption savings) apply to control/status information.

Primary rate interfaces such as the MH89760 Extended Super Frame T1 Digital Trunk Interface (1544 kbit/s, S2 reference point) and the MH89790 CEPT Digital Trunk Interface (2048 kbit/s, S1 interface) have entire streams dedicated to control and status. This is because control/status is required on a per channel basis. Basic rate interfaces have control/status information embedded in DST streams. Figures 4 and 5 show the correlation between data and basic rate device control/status channels on DST streams. Also note the frame pulse output by the devices for allocating channels to other devices in a daisy chain fashion. This will be discussed in later sections.

4.0 ST-BUS Family of ISDN Components

The implementation of an economical ISDN requires a number of principle interfacing and support functions to be performed by VLSI devices. These functions are:

a) Interfacing to the U reference point
b) Interfacing to the S0, S1 and S2 reference points
c) Interworking with non-ISDN (RS-232, X.21) formats at the R reference point
d) Voice coding/decoding
e) Link layer and network layer communication
f) Circuit switching
g) Time base generation

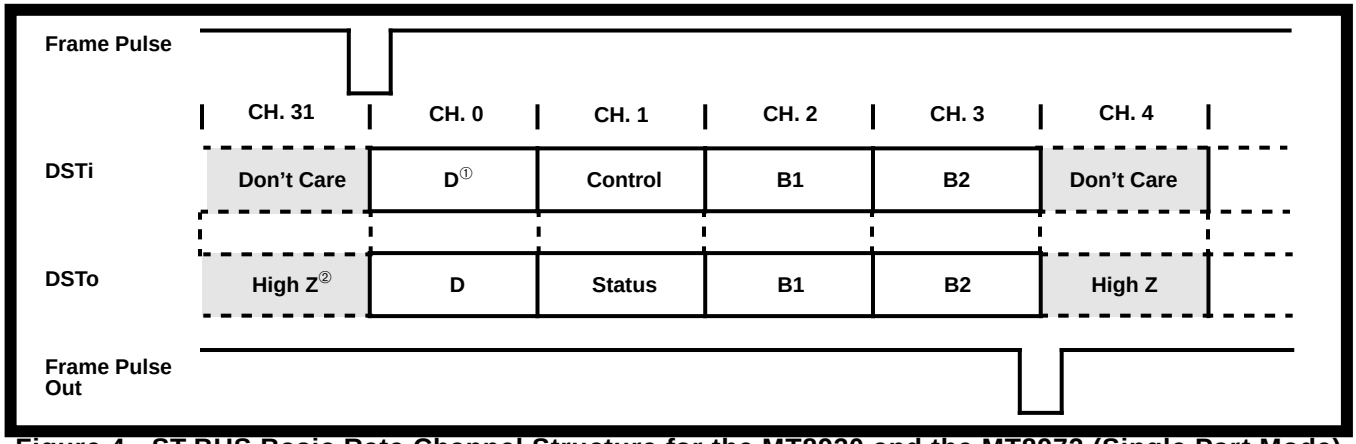

Figure 4 - ST-BUS Basic Rate Channel Structure for the MT8930 and the MT8972 (Single Port Mode)

① D Channel information, first two bits are used (16 kbit/s).
② High impedance state.

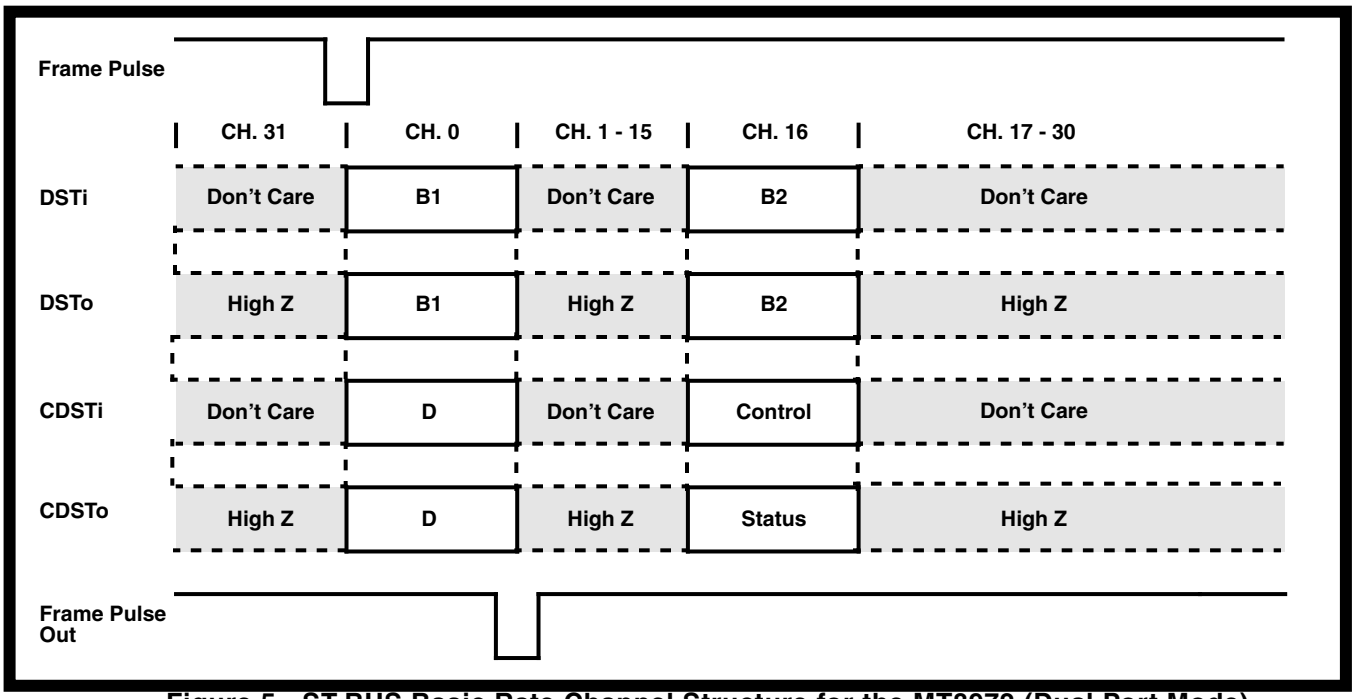

Figure 5 - ST-BUS Basic Rate Channel Structure for the MT8972 (Dual Port Mode)

To be considered complete, a family of ISDN components must support all of these ISDN functions. Zarlink Semiconductor provides components for each of these functions, all connected by the ST-BUS component interface. Table 1 correlates the ISDN function with the ST-BUS component that performs the function. Figures 6 and 7 show where ST-BUS ISDN devices fit into the ISDN User Access Model. Each device will be briefly described in the next few sections, emphasizing the ST-BUS aspect of the component. More detail may be found in the specific product's data sheet.

To continue this discussion, several blocks in Figure 1 require brief definition. TE1's are Terminal Equipment that are compatible with ISDN access requirements. TE2's are non-ISDN Terminal Equipment. TA's are Terminal Adaption circuits that adapt non-ISDN terminals to the ISDN. NT2's are Network Terminating equipment that perform some networking function, eg., a PBX, a LAN etc. NT1's perform a bridge function between the S0 reference point and the U reference point. Both the NT2 and the NT1 can be combined, omitting the S0 reference point. LT's are the subscriber Loop Terminations at the network side of the U reference point. ET's are the Exchange Terminations. The ET's and the LT's may be combined, just as the NT2's and the NT1's may be combined, omitting the V reference point.

ISDN FUNCTION	ST-BUS COMPONENT
U Interface	MT8972 (DNIC)
S0 Interface	MT8930 (SNIC)
S1 Interface	MT8978, MH89780 (CEPT 2048 kbit/s Trunk Interface) MT8979, MH89790 (CEPT 2048 kbit/s Trunk Interface Supporting CRC4)
S2 Interface	MT8976, MH89760 (ESF 1544 kbit/s Trunk Interface)
Non-ISDN Data Interface	MH89500 (Rate Adapter)
Voice Codecs and Digital Telephone	MT8964/65 (Voice Codecs) MT8994/5 (Digital Telephone)
Link Layer Support	MT8930 (On-Chip Protocoller) MT8952B (HDLC Protocol Controller)
Switching	MT8980/ 81 (Digital Crosspoints)
Time Base Generation	MT8940 (DPLL) MT8930, MT8972 (On-Chip PLL)

Table 1. ST-BUS ISDN Components

4.1 Interfacing to the U Reference Point

The U reference point specifies the transmission method for basic rate information transfer between an ISDN and the subscriber's premises (160 kbit/s). The specification is being developed by the T1D1.3 committee in the United States. The requirements are that the transmission media is a single twisted

wire pair, and the method for achieving full duplex transmission is adaptive echo cancellation. The 160 kbit/s rate is divided into two B-channels, one D-channel (D16), and 16 kbit/s OAM (Operations, Administration and Maintenance) information. The line code is the 2B1Q (2 Binary 1 Quaternary) line code. The format of the OAM information, which includes synchronization information, is still being determined.

The MT8972 Digital Network Interface Circuit complies with this still developing standard to a certain degree. Full duplex communication over a single twisted pair at a data transfer rate of 160 kbit/s is performed, adaptive echo cancellation is used and subscriber information is transferred on two B-channels and a D-channel (D16). The remaining requirements of the DNIC's transmission scheme differ from what the U reference point standard will be. The modulation technique incorporated by the MT8972 is differentially encoded biphase, and the 16 kbit/s of OAM information is divided into an 8 kbit/s synchronization signal and an 8 kbit/s "housekeeping" channel, available to the user.

The biphase line code and the associated synchronization technique were chosen as a tradeoff between cost of implementation and capability. As a result, the MT8972 is the best combination of price, capability and proven performance of the two wire, 2 B + D format transmission devices currently available. The device is a good intermediate solution until the standard is complete and provides a cost effective long term solution for private loops (behind a PBX). A device compatible with the final standard will be available from Zarlink, in keeping with the company's philosophy of complying with industry standards.

ST-BUS access to the MT8972 is provided in two ways. All information (2 B + D + one control/status byte) can be transported on one DSTi stream and DSTo stream (Figure 4 - Single Port Mode). Alternatively, if it is desirable to separate user information from control/status and D-channel information (sometimes desirable in a Private Branch Exchange, Multiplexer or other large system), two B-channels can be transported on the DSTi and DSTo pins, and the D-channel and control/status channel can be transferred on the CDSTi and CDSTo pins (Figure 5 - Dual Port Mode). The application in Figure 6 shows MT8972's in Dual Port Mode, in a network line card application.

The MT8972 can be configured to be used at either end of the subscriber loop. It can either have its 4096 kHz clock input to it (network side or master mode), or it can derive timing from the received line signal at the NT (slave mode). After the MT8972 receives its frame pulse, it is referenced to the channels it is allocated on the ST-BUS (in slave mode the MT8972 generates the frame pulse). When the MT8972's ST-BUS access period is finished, a frame pulse is output to furnish another MT8972 with a reference for ST-BUS access. This allows daisy chaining of frame pulses for use in line card applications.

4.2 Interfacing to the S0 Reference Point (Basic Rate)

The S0 reference point is defined by the CCITT to be the basic rate information transmission method between TE's and NT's, specified in recommendation I.430. The MT8930 Subscriber Network Interface Circuit is fully compatible with this standard. The user information, signalling information and control/maintenance information specified at the S0 reference point is all accessible through the MT8930. The MT8930 can transfer this information between its three ports: the S-Interface port, the microprocessor port and the ST-BUS port (see Figure 4 for ST-BUS format).

The MT8930 may be used in either TE's, TA's or NT's. At the NT, the MT8930 is synchronized to external clocks, and in the TE and TA applications the MT8930 synchronizes to the received line signal. In the latter case, the MT8930 generates the ST-BUS clock and frame pulse, just like the MT8972 did in subscriber side (NT) applications. The MT8930 also produces a frame pulse at the end of its allocated ST-BUS channels for daisy chaining in line card applications.

The microprocessor port is provided to access the MT8930 control and status registers. The MT8930 has a controllerless mode for applications where a microcontroller is not required. An on-chip Packet Assembler/Disassembler (PA/D) may also be accessed through the microprocessor port, to assist in formatting information on the D-channel in the LAPD format (Link Access Procedure on the D-channel). The B-channels are accessible from the microprocessor port, as is the ST-BUS port.

B-channel information is accessible through the ST-BUS port, for connection to other information processing components. Control and status information for the MT8930 and D-channel information can also be transferred via the ST-BUS port. This can be advantageous in a line card application, as it may be more desirable to use a multi-channel formatter as opposed to the individual formatters on each MT8930. An advantage of controlling the MT8930 through the ST-BUS interface

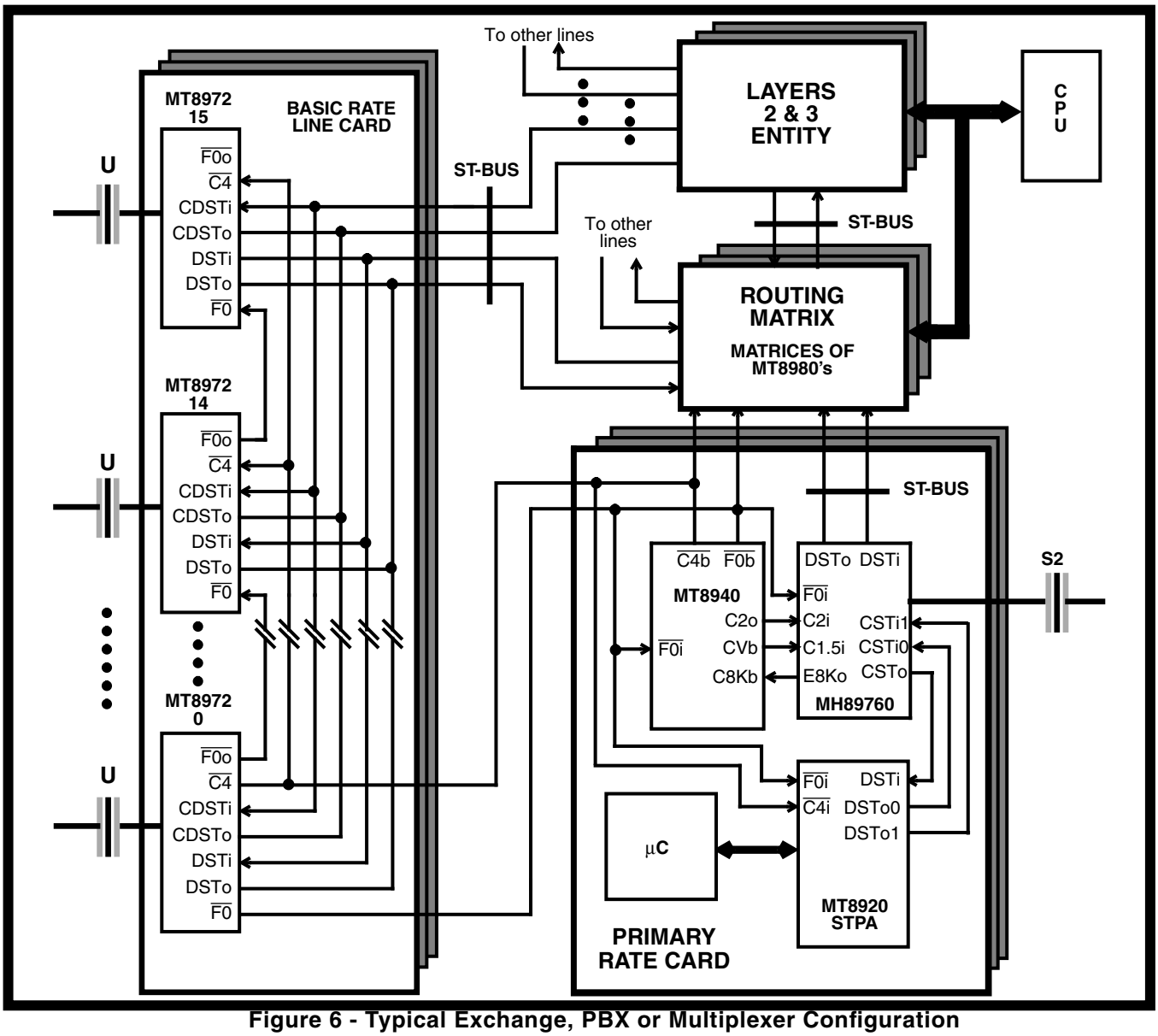

Figure 6 - Typical Exchange, PBX or Multiplexer Configuration

is that the interface looks exactly like an MT8972 interface to the rest of the system. This promotes interchangeability of the devices at backplane connections.

Figure 7 shows several applications of the MT8930 in the subscriber's premises.

4.3 Interfacing to the S1 and S2 Reference Points (Primary Rate)

The S1 and S2 reference points are specified in recommendation I.431. This recommendation is based on the digital trunk specifications of the CCITT G series. Zarlink components which can be used for the S1 and S2 reference points are:

a) The MT8976, MH89760 ESF Digital Trunk Interface for the 1544 kbit/s rate (S2).

b) The MT8978, MH89780, MT8979 and MH89790 Digital Trunk Interfaces for the 2048 kbit/s rate (S1).

All the digital trunk interfaces comply with the Frame formats specified in I.431, and support clear channel operation. For timing purposes, the trunk circuits extract clock information from the received signal. This information is used for clocking in the received information and for ST-BUS timing (in slave applications). A complementary device, the MT8940 Digital Phase Locked Loop, is provided to lock received timing to local timing if required (slave applications). This device is also a convenient tool for generating ST-BUS signals like clocks and frame pulse, in systems that don't require phase synchronization (master systems).

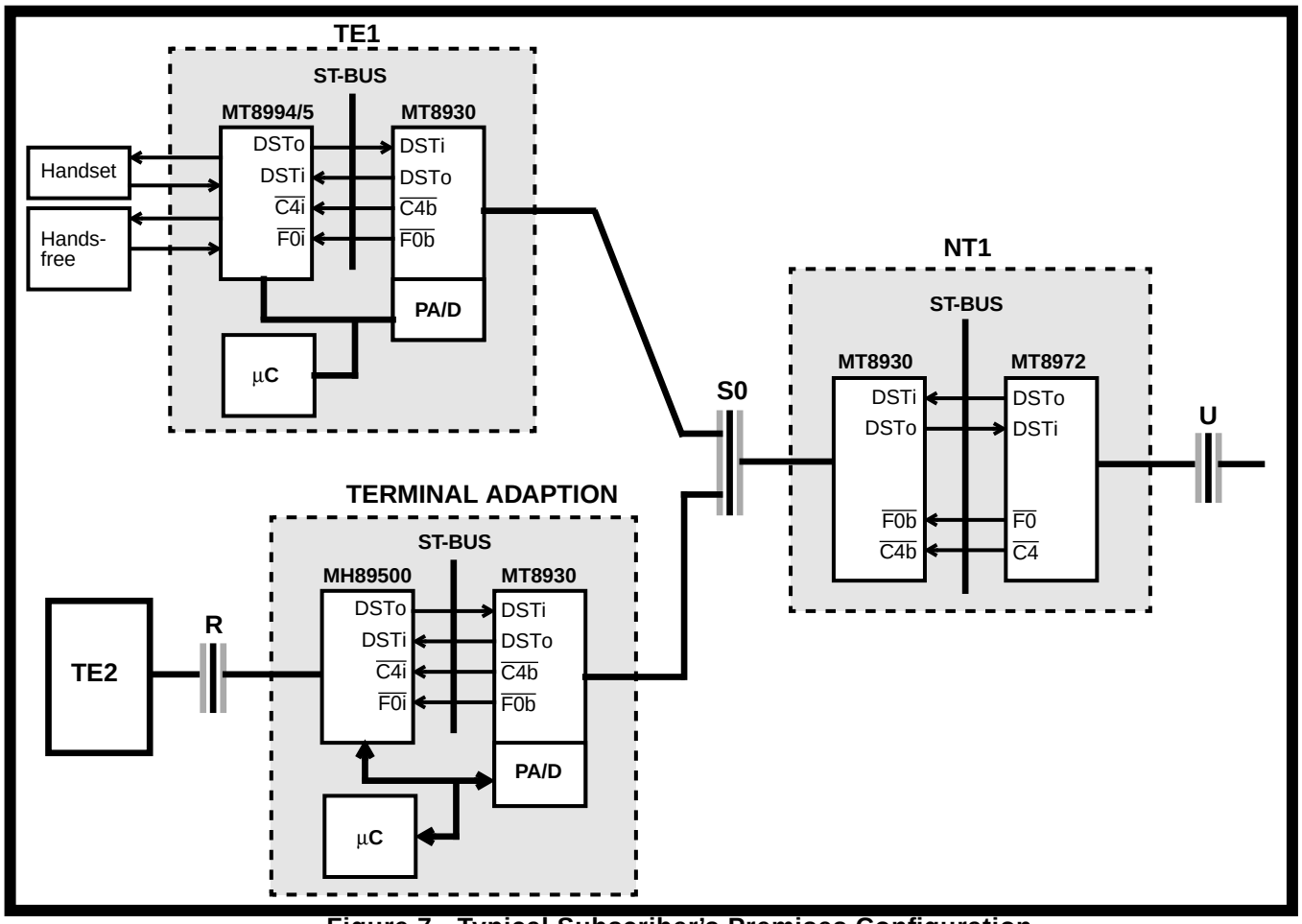

Figure 7 - Typical Subscriber's Premises Configuration

Communication to the trunk interfaces is via ST-BUS (transporting both information for processing, and control/status information). A frame pulse determines the start of a frame for each component. Bit timing is provided by a clock (2048 kHz clock) input, which is easily derived from the 4096 kHz clock used for the rest of the ST-BUS ISDN components.

Controlling the digital trunks requires flexible microprocessor access to the ST-BUS. The MT8920 STPA (ST-BUS Parallel Access) device provides fast microprocessor access to one incoming ST-BUS stream and two outgoing ST-BUS streams (directly corresponding to CSTo1, CSTi0 and CSTi1 needed by the digital trunk interfaces. See Figure 6). The ST-BUS timing is controlled by a frame pulse and a clock signal. Another method of accessing the ST-BUS with a microprocessor is the MT8980 Digital Crosspoint, or the MT8952 HDLC Controller, both of which will be discussed in a following section.

4.4 Non-ISDN Data to ISDN Interworking

The R reference point in the ISDN User Access Model (Figure 1) is the point where terminals with non-ISDN interfaces (TE2's) access the ISDN. Data terminals at this point may comply with the following pre-ISDN recommendations for interfacing to Data Communication Equipment: X.20, X.20 bis, X.21, X.21 bis, and some V-series recommendations. Recommendations I.460, I.461, I.462 and I.463 specify how these non-ISDN data interfaces may be synchronously rate adapted to comply with ISDN. The European Computer Manufacturers Association recommendation 102 (ECMA 102) additionally specifies asynchronous rate adaption.

The MH89500 performs rate adaption according to I.460, I.461, I.463 and ECMA 102. Rate adapted information is transferred to and from an ST-BUS environment, where the information is available to any other ST-BUS ISDN component. The MH89500 requires a 4096 kHz clock and a frame pulse, using ST-BUS channels 0, 2 or 3 (channels 2 and 3 are compatible with the B-channels of the MT8972 and MT8930).

I.460 specifies that multiple low speed channels (8 kbit/s, 16 kbit/s, and 32 kbit/s) may be multiplexed into one 64 kbit/s B-channel. Any bit rate below 8 kbit/s only needs one bit in an eight bit ST-BUS channel, 8 to 16 kbit/s bit rates need two bits, 16 to 32 kbit/s bit rates need four bits, and 32 to 64 kbit/s

bit rates need eight bits. The MH89500 (a one channel device) allows specification of which bits in the ST-BUS channel it uses. This capability allows up to eight MH89500's to be connected in parallel, submultiplexing information into a common channel.

Figure 7 shows an MH89500 connected to an MT8930 in the TA block of the ISDN User Access Model. Figure 8 shows multiple MH89500's connected in parallel for submultiplexing purposes, in a maximally integrated TA function (TA2). A TA2 allows call set up to be performed using the D-channel. Minimal integration (TA1) means that the ISDN has set up a semi-permanent or "hot-line" circuit between the terminal equipment and the packet network. The MH89500 gives its controlling microcontroller a communication path to the DTE through the MH89500 microprocessor port. This makes TA2 implementation much easier.

4.5 Voice Codecs

To traverse an ISDN, voice signals must be translated to digital information using Pulse Code Modulation (PCM) techniques and then placed into a B-channel. Zarlink Semiconductor makes several PCM components that interface voice signals to the ST-BUS and hence, ISDN.

The base product is the MT8964/65 Voice Codec, with programmable gain and attenuation on the I.C. The variants of the Codec determine the digital encoding algorithm: μlaw, true sign inverted amplitude or A-law, true sign inverted amplitude. The Voice Codec products can be used in both subscriber premises equipment and network equipment. These products are useful in inter-working non-ISDN analog equipment with an ISDN.

The ST-BUS interface to the Voice Codec consists of a framing pulse, a 2048 kHz clock signal, a DSTo/DSTi port and a CSTo/CSTi port. The DST streams carry PCM information, and the CST streams carry control/status information.

The MT8994/5 Digital Telephone (D-phone) is a fully integrated digital telephone I.C. designed for use in a TE1 (Figure 7). It incorporates an on-chip Codec (μ law or A-law), a tone ringer, a DTMF generator, speaker-phone algorithm, and an interface to standard telephony transducers. There is a microprocessor port for control/status requirements (tailored to Motorola and Intel microcontrollers) and an ST-BUS port for interfacing to either a U, or S0 interface device. The ST-BUS clock signals are a frame pulse and a 4096 kHz clock. PCM channel allocation is compatible with the MT8930 and the MT8972 B1 and B2 channels in single port mode.

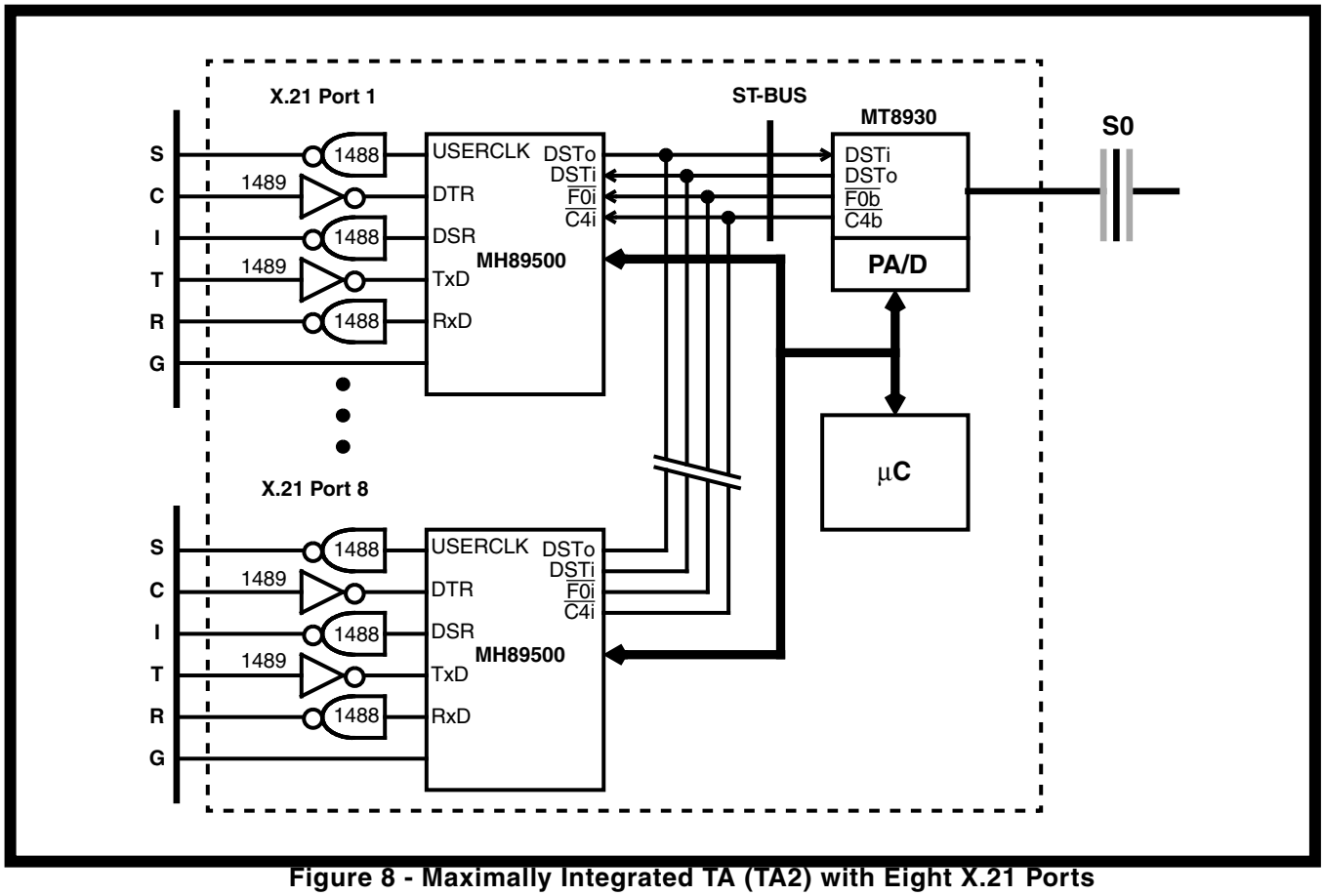

Figure 8 - Maximally Integrated TA (TA2) with Eight X.21 Ports

The ST-BUS control/status channel is visible from the microprocessor port, so that the control/status channel of either the MT8930 or the MT8972 may be accessed. The ST-BUS channel allocation of the MT8994/5 is programmable, so other ST-BUS ISDN components can share the B channels of the transmission device with the D-Phone.

A potential TE other than a TE1 could consist of an MT8994/5, MT8952B HDLC controller and an MT8972 (Figure 9). This would be equivalent to a TE1 incorporating the NT1 function. The MT8952B would provide protocolled control over the D-channel or over either B-channel (for interworking with packet networks), while the MT8994/5 provides voice communication over either B-channel.

4.6 Link Layer Support

Recommendation I.441 specifies the User/Network data link layer protocol for ISDN. The protocol specified in I.441 is called Link Access Procedure on the D-Channel (LAPD). All ISDN signalling information, as well as telemetry information and low rate packet communications, is transferred across the D-channel in LAPD formatted packets.

LAPD is very similar to the High Level Data-Link Control (HDLC) protocol and the LAPB protocol that is specified in CCITT recommendation X.25. Differences between these protocols are limited to procedural (or peer to peer) functions. PA/D functions, such as opening and closing flags, data transparency through bit stuffing and Frame Check Sequence calculation, are all common among protocols like HDLC, LAPD, and LAPB.

The fact that the PA/D function is common among many layer 2 protocols makes the MT8952B HDLC Controller (a PA/D device) useful in a variety of network functions. It can be used as a D-channel communication device, or it can be used for interworking with non-ISDN packet networks, such as an X.25 network, through a B-channel. It has a microprocessor port and and ST-BUS port, allowing it to be used with any combination of ST-BUS ISDN components, as shown in Figure 9.

The ST-BUS clock signals required by the MT8952B are a frame pulse and 4096 kHz clock (or optionally 2048 kHz). Information transfer rates supported are 8 kbit/s, 16 kbit/s, 48 kbit/s, 56 kbit/s, 64 kbit/s, 128 kbit/s and 192 kbit/s. Bit positions and channel positions are compatible with the D-channel and B-channel positions of the MT8972 and the MT8930. Transfer rates of 8, 16, and 48 kbit/s are only available through channel 0 (D channel compatibility). With a 64 kbit/s transfer rate, data is available on either channel 2, 3 or 4, where channels 2 and 3 are compatible with the B-channel. At the 128 kbit/s transfer rate, data is concatenated on channels 2 and 3 and at 192 kbit/s data is concatenated on channels 2, 3 and 4 (this last option is not useful for basic rate applications). ST-BUS channel 1 is dedicated to a special register in the MT8952B, meant to map directly into the control/ status channels of the basic rate components.

The MT8952B is designed for use with the MT8972 and as a component to be used as part of a larger, central signalling resource. Network applications favour a loosely coupled approach to signalling and control, separate from transmission facilities. On the other hand, TE applications favour a signalling resource tightly coupled to the transmission circuitry. The PA/D function is built into the MT8930 for TE applications.

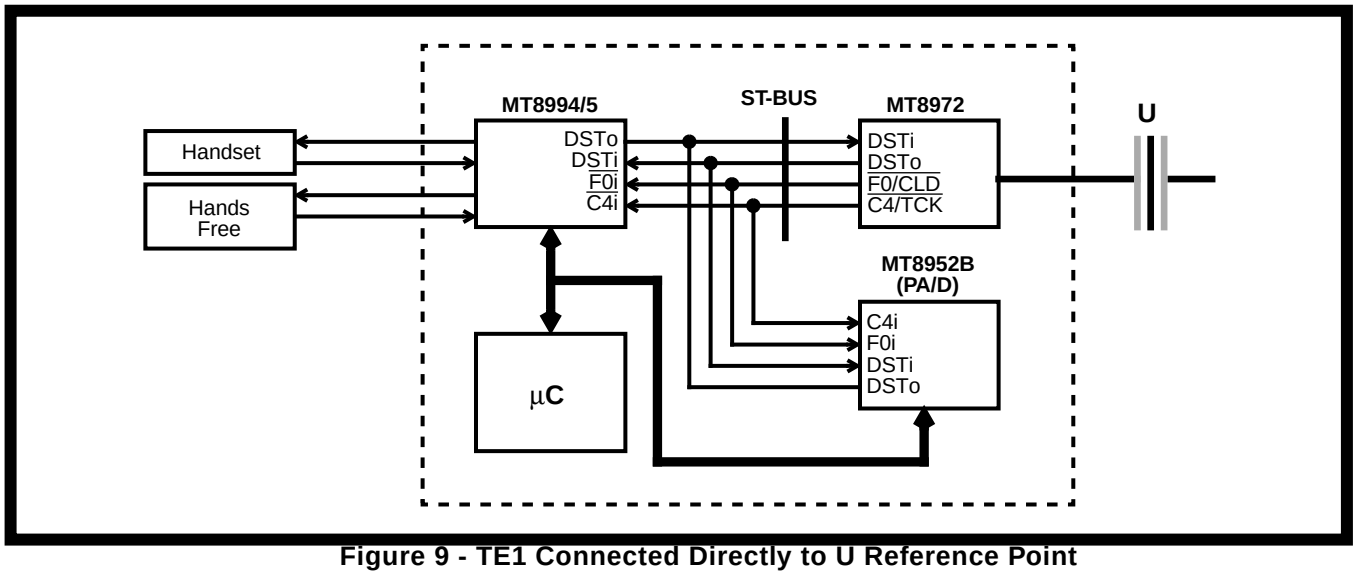

Figure 9 - TE1 Connected Directly to U Reference Point

The MT8972 does not have PA/D circuitry incorporated into it at present because the current definition of the ISDN Subscriber Access Model promotes the use of the S reference point in TE's, with the U reference point connected to Modem-like NT equipment and the network.

4.7 Switching

In larger ISDN systems, particularly network equipment, there is a requirement for having circuit switching capability. The MT8980 and the MT8981 are digital crosspoint switches, based on the ST-BUS architecture. The MT8980 is a 256 channel by 256 channel non-blocking switch (eight ST-BUS inputs to eight ST-BUS outputs). This is equivalent to 65536 crosspoints. The MT8981 is a 128 channel by 128 channel non-blocking switch (four ST-BUS inputs to four ST-BUS outputs, 16384 crosspoints).

The outputs have per channel high impedance capability, enabling large switching matrices to be constructed using multiple MT8980/81's. The ST-BUS ports are visible to the microprocessor interface, to allow control/status information to be placed on ST-BUS streams through these components. The ST-BUS clock signals required are a frame pulse and a 4096 kHz clock.

4.8 Time Base Generation

Every system needs a common time base as a timing reference. Digital communication systems must have synchronization between the time bases of communicating equipment to ensure information is sampled at the correct time. This synchronization is performed using phase locked loop techniques: a locally generated time base, close to the frequency of a received signal or some derivative of that frequency, is phase adjusted when the phase difference between the two signals becomes too great.

The MT8972 in master mode (Loop termination at network side) uses an external 10240 kHz clock source (frequency locked to the ST-BUS clock signals) to generate timing on the transmit side. Timing is extracted from the received line signal to clock in the received data, and the information is retimed to the ST-BUS timing. Frame pulse and the 4096 kHz clock are input to control the ST-BUS timing of the component.

In slave mode (Network termination at user side), the 10240 kHz time base is provided by an external crystal. The time base is phase locked to the received signal, and the phase locked timing is used to generated transmit timing, as well as ST-BUS timing (frame pulse and 4096 kHz clock) for the rest of the slave system that the MT8972 resides in.

The MT8930 operates in a very similar manner to the MT8972 in comparable applications (NT applications and TE applications), however, the 10240 kHz external time base of the MT8972 is replaced by an on-chip voltage controlled oscillator. The ST-BUS signals are provided externally in NT mode and sourced by the MT8930 in TE mode.

The thick film hybrid versions of the digital trunk interfaces (MH89760, MH89780, MH89790) incorporate tunable clock extractors that extract the data rate from the received data signal. This provides a clock for the line receiver circuit (2048 kHz or 1544 kHz). An 8 kHz signal (nominally the frequency is dependent on the extracted clock frequency) is also generated by the digital trunks.

The MT8940 T1/CEPT Digital Phase Locked Loop is specifically designed to generate an ST-BUS time base (frame pulse, 4096 kHz and 2048 kHz clock) and a 1544 kHz clock, using a 12355 kHz Oscillator input and a 16388 kHz oscillator input. To synchronize a system to the received signal, the MT8940 can be used to phase lock these timing signals to the 8 kHz signal extracted from the digital trunk interface.

5.0 Conclusion

The ST-BUS is a simple inter-component interface that allows complete connectivity between ISDN devices. An important aspect of the connectivity is that it is common to a complete set of ISDN functions. The flexibility of the ST-BUS architecture, coupled with the full complement of supporting components, permits the easy, economical design of any type of ISDN equipment.

ST-BUS components address the physical layer and the data link layer needs of ISDN. ST-BUS support of ISDN shall be extended beyond the current component family to encompass any new ISDN recommendations. This commitment to support, makes ST-BUS the preferred inter-component interface for ISDN.

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